PSPICE BASED REALISATION OF SINGLE-PHASE THIRTEEN LEVEL INVERTER USING SINGLE DC SOURCE

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Abstract—Multilevel inverter has emerged recently as a very important alternative in the area of high-power medium voltage energy control. This project presents the most important topologies like diode clamped inverter (neutral point clamped), capacitor clamped (flying capacitor) and cascaded multi cell with separate DC sources. The most relevant control and modulation methods developed for this family of converters include multi-level sinusoidal pulse width modulation, multi-level selective harmonic elimination and space vector modulation. Special attention is dedicated to the latest and more relevant applications of these converters such as laminators, conveyer belts and unified power flow controllers. The need of an active front-end at the input side for those inverters supplying regenerative load is also discussed and circuit topology options are also presented. The thirteen-level inverter was designed and results were also shown in the project. Finally the peripherally developing areas such as high voltage high power devices and optical senses and other opportunities for future development are addressed.

Index Terms—Multilevel Inverter, Total Harmonic distortion, Single-Phase.

I. INTRODUCTION

The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. As the number of levels reach infinity, the output total harmonic distortion approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. For single-phase multilevel inverters, the most common topologies are the cascaded, diode-clamped, and capacitor clamped types. There exist many other topologies. In general, multilevel inverter topologies can be classified into two types: Type I and Type II[1]. Type I uses multiple dc voltage sources and Type II uses multiple (split or clamping) dc voltage capacitors. Type I includes the traditional cascaded topologies. Type II includes the conventional diode-clamped and capacitor-clamped inverters. In terms of single phase multilevel inverters, the disadvantages of the two types are apparent. Type I suffers from the availability of the multiple dc voltage sources. In practice, bulky transformers either of low or medium frequency are required. This is a great challenge to when it comes to volume, weight, and cost minimization. The problem with Type II is mainly the balancing of the dc capacitor voltages. Recently thirteen level inverters using H-Bridge inverter have drawn some researcher’s interest. As for the single-phase thirteen level case for a typical diode-clamp inverter twenty four switches, eighteen diodes and single dc source are needed. The capacitor-clamped thirteen level inverter involves twenty four switches, thirty capacitors and single dc source. The cascaded thirteen level inverter has three asymmetrical separate dc sources and three H-Bridge inverters.

This paper presents a simplified H-Bridge multilevel inverter with reduced number of switches. Apart from power devices and circuit complexity reduction we need to take into account the technological tendency to lower the prize at which multilevel inverter can compete with standard configuration. As contribution to solve this twin problem (cumbersome power stage and complex firing control circuit) this work proposes a new converter topology, presented as in Fig.1. This
topology includes an H-Bridge stage with an auxiliary bidirectional switch, drastically reducing the power circuit complexity.

Fig.1. H-Bridge Inverter with Auxiliary Switches

Theoretical analyses and simulation results are presented to show the validity of the proposed inverter.

II. PROPOSED INVERTER

Fig. 1 shows the circuit diagram of the proposed single-phase thirteen level inverter. Obviously the topology is very simple and can be constructed by including an H-bridge stage with an auxiliary bidirectional switch, drastically reducing the power circuit complexity.

2.1 Main Power Switches:
The new topology achieves around 40% reduction in the number of main switches required, using only nine controlled power switches. The voltage and current rating of the auxiliary switches are lower than that required by the main controlled switches.

2.2 Auxiliary Devices:
The new configuration reduces the number of diodes and capacitors, when compared with the diode clamped and capacitor clamped configurations. Since the six capacitors are connected in parallel with the main dc power supply, no significant capacitor voltage swing is produced during normal operation, avoiding a problem that can limit operating range in other multi level configurations.

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2.3 Switching States for Thirteen Level Output Voltage
The switching states and voltage levels can be summarized in Table I. The proposed inverter can generate thirteen voltage levels at its output terminals. The switching frequency is low and hence the switching losses will be less.

\[
\text{Switching frequency} = 50 \text{ Hz} \\
\text{Total time period} = \frac{1}{f} = 20 \text{ ms} \\
\text{Switching time} = \frac{\text{total time period}}{\text{no. of switching patterns per cycle}} = \frac{20}{25} = 0.8 \text{ ms}
\]

2.3 Modes of Operation:
1. 0 Voltage level

Fig. 2. Mode of operation of the H-Bridge Thirteen Level Inverter to output 0 voltage level.
During this mode switches M3 and M4 are turned ON.
The following capacitors will be charging C1, C2, C3, C4, C5, and C6.
The Kirchhoff’s Voltage Law equation for this mode is as follows
\[ V_s + V_{m8} - V_r - V_{m9} = 0. \] (1)

2. Voltage Level = +Vdc/6

During this mode switches M4 and M9 are turned ON.
The Kirchhoff’s Voltage Law equation for this mode is as follows
\[ V_s + V_{m5} - V_r - V_{m9} = 0 \] (2)

3. Voltage Level = +2Vdc/6

During this mode switches M4 and M8 are turned ON.
The following capacitors C1, C2, C3, and C4 are charging.
The Kirchhoff’s Voltage Law equation for this mode is as follows
\[ V_s + V_{m6} - V_r - V_{m9} = 0 \] (3)

4. Voltage Level = +3Vdc/6

During this mode switches M4 and M7 are turned ON.
Capacitors C1, C2, and C3 are charging.
The Kirchhoff’s Voltage Law equation for this mode is as follows
\[ V_s + V_{m7} - V_r - V_{m9} = 0 \] (4)

5. Voltage Level = +4Vdc/6

During this mode switches M4 and M6 are turned ON whereas capacitors C1 and C2 are charging.
The Kirchhoff’s Voltage Law equation for this mode is as follows
\[ V_s + V_{m6} - V_r - V_{m9} = 0 \] (5)

6. Voltage Level = +5Vdc/6

During this mode switches M4 and M5 are turned ON.
Only C1 capacitor is charging during this mode and switches M4 and M5 are turned ON.
The Kirchhoff’s Voltage Law equation for this mode is as follows
\[ V_s + V_{m5} - V_r - V_{m9} = 0 \] (6)
During this mode switches M1 and M4 are turned ON. The Kirchhoff’s Voltage Law equation for this mode is as follows

8. Voltage Level = \(-\frac{V_{dc}}{6}\)

During this mode capacitors C2, C3, C4, C5 and C6 are charging. Switches M2 and M5 are turned ON. The Kirchhoff’s Voltage Law equation for this mode is as follows

9. Voltage Level = \(-2 \frac{V_{dc}}{6}\)

During this mode switches M2 and M6 are turned ON. And capacitors C3, C4, C5 and C6 are charging. The Kirchhoff’s Voltage Law equation for this mode is as follows

10. Voltage Level = \(-3\frac{V_{dc}}{6}\)

During this mode switches M2 and M7 are turned ON. Now capacitors C4, C5 and C6 are charging. The Kirchhoff’s Voltage Law equation for this mode is as follows

11. Voltage Level = \(-4\frac{V_{dc}}{6}\)

During this mode switches M2 and M8 are turned ON. And capacitors C5 and C6 are charging. The Kirchhoff’s Voltage Law equation for this mode is as follows

12. Voltage Level = \(-5\frac{V_{dc}}{6}\)
During this mode switches M2 and M9 are turned ON. Only the capacitor C6 is charging. The Kirchhoff’s Voltage Law equation for this mode is as follows

\[ V_s + V_{m5} - V_r - V_{m7} = 0 \]  

(12)

### III. RESULT ANALYSIS

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<th>Parameters of the Inverter for Simulation</th>
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### IV. CONCLUSION

A cost effective simplified H-bridge thirteen level inverter has been simulated using PSPICE. By using the 13 level H-bridge inverter with auxiliary switches we can achieve reduction of total harmonic distortion. Hence efficiency increases due to reduction in switching losses. Moreover we need less isolation and we can achieve balance voltage transfer by this proposed method. A further development of the simplified H-bridge multilevel inverter able to be
applied to any number of voltage levels within the power switches maximum voltage, is now under consideration.

REFERENCES


