Three-level full-bridge zero voltage and zero current switching DC-DC converter Topology

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***Abstract*— This project proposes a development of soft switching scheme for three level DC-DC converter is used to provide zero voltage switching condition for all the controlled switches. In this paper, the gate pulses are generating from PWM controller. This paper describes the main operational modes of the proposed converter as well as simulation results and also observes and compares the switching losses of the proposed converter with and without zero voltage switching scheme.**

***Index Terms*— Zero Voltage Switching (ZVS), Zero Current Switching (ZCS).**

I. INTRODUCTION

In ordinary converters there exists many problems like stress on switches, switching losses, EMI etc…. These problems can be eliminated by using ZVS and ZCS converters. In ZVS, the switches are turned on and off at zero voltages and in ZCS, the switches are turned on and off at zero currents. As a result power reduces almost to a least value, by which the stress on the switches can be reduced. To adopt ZVS and ZCS techniques to three level as well as five level full bridge converter. Switch-mode dc-to-ac inverters used in ac power supplies and ac motor drives where the objective is to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. Practically, we use an inverter in both single-phase and three phase ac.

II. PROPOSED THREE LEVEL ZERO VOLTAGE AND ZERO CURRENT SWITCHING FULL BRIDGE DC-DC CONVERTER TOPOLOGY

The goal of the design is to produce a dc–dc converter that achieves soft switching for all the main switches, reduces the voltage stresses across each main switch, and controls the voltage on the secondary as per an FB step-down converter. Fig.1 shows the circuit topology and the operational waveforms of the proposed converter. A proposed three level dc-dc converters is presented as shown in fig 1.

A. Operation Of The Zvzcs 3 Level DC-DC Converter Topology

The resistance R-load is the load equivalent resistance and might represent, for example, the inverter interfacing a distribution system. The intermediate voltage stages typically available in a 3L converter (i.e., ±*V*dc/2) allow a better approximation of a sinusoid thus resulting in a reduction in harmonic levels for the inverter case, but this feature is not applicable to the dc–dc converter here since the output voltage *V*out fixed at a constant dc level, is greater than the intermediate levels typical of dc–ac 3L converters. If the intermediate voltages were used, the voltage at the input of the diode-bridge rectifier would be less than *V*out and the rectifier would not conduct, so no power would be delivered to the load. Table 1 gives the proposed switching states and identifies the voltage levels *Vs* at the output of the transformer for each switching state. A "+" symbol indicates that the switch is ON during the switching state, while a "−" symbol indicates that the Switch is OFF. The switching frequency is fixed and each switch is ON for exactly half a switching cycle, but the timing of the turn-ON and turn-OFF of each switch is controlled so that the dc-bus voltage is applied to the transformer for the desired time as with phase-shifted PWM. Using Table 1 and recognizing that the rectifier causes the voltage at the output filter to be positive regardless of the polarity of the transformer voltage, it can be realized that the system has the same general operating modes as a buck converter.

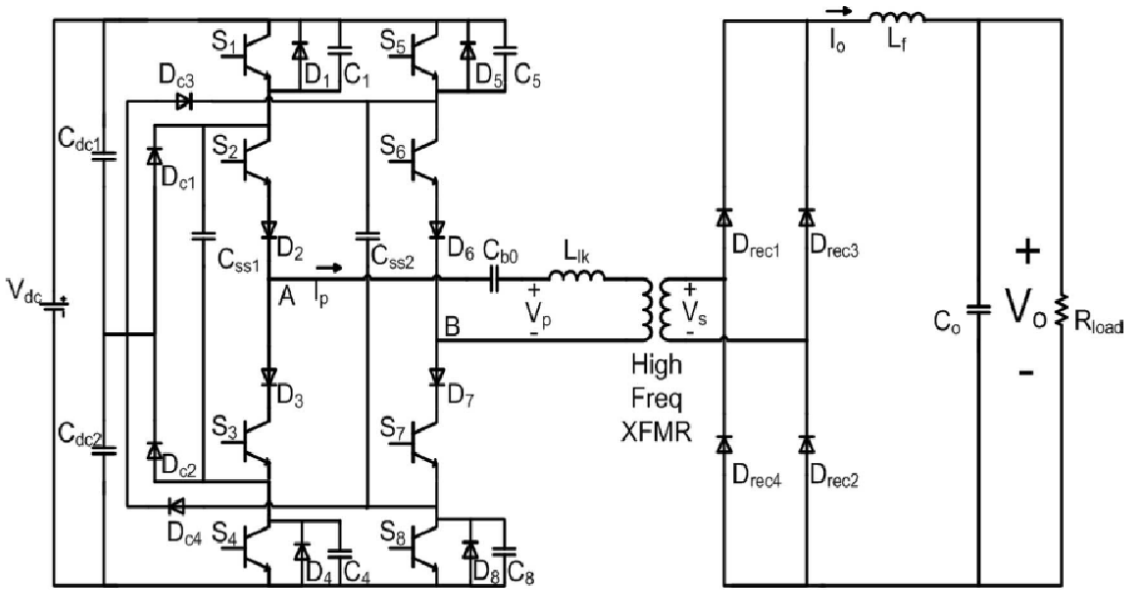

Fig.1. ZVZCS 3 Level control DC-DC converter

The switching scheme, though it does not allow the intermediate voltage levels, does achieve soft switching for all the main devices. Furthermore, the loss of intermediate switching states is consistent with other 3L soft-switched designs. The rectifier diodes *D*rec1–*D*rec4 change the transformer voltage so that a positive voltage is applied to the output filter regardless of the polarity of the transformer voltage; thus, the converter's operation can be defined in terms of half cycles with the voltage and current seen by the output filter *Lf –Co* being the same for each half cycle. If the converter is in state 1 for duration $D \times T\text{sw}/2$, where D represents the duty cycle and is a fraction between 0 and 1, then the average voltage at the rectifier will be

$$V_{out} = \frac{D * V_{dc}}{n} \qquad (1)$$

Where n is the turn's ratio of the transformer. This provides the desired dc voltage conversion and shows that the system operates as a transformer zed buck converter. This Chapter will show how the switching scheme achieves soft switching. Examining Table I and Fig.4.1 reveals that diagonal switches receive the same control signals. The switching scheme can be simplified by controlling the devices in pairs, so that each pair— *S*1 and *S*8, *S*2 and *S*7, *S*3 and *S*6, and *S*4 and *S*5—receives the same control signal. It can be further noted that the switching order and duration is identical to phase-shifted PWM for a two level FB, so existing phase-shifted PWM controllers can be used to control the converter. This is an advantage compared to other 3L FB soft-switching topologies which require complex switching control schemes, such as double-phase-shifted control.

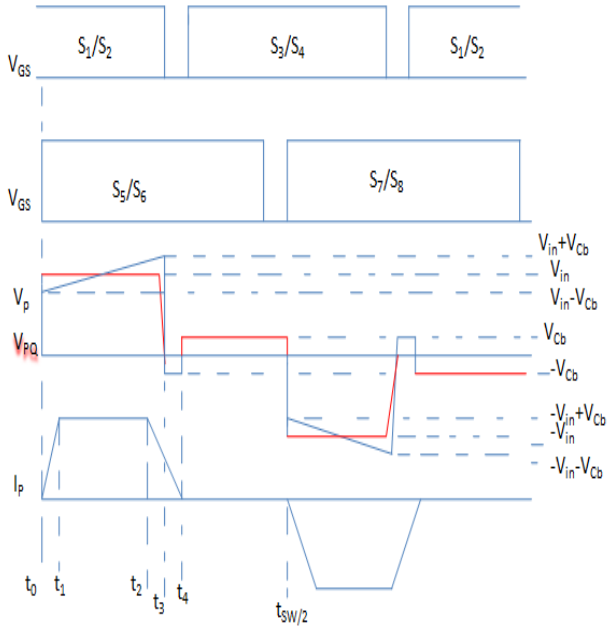

Fig 2.L FB ZVZCS converter. (a)Schematic. (b)Operational waveforms

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State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	V
1	+	+	-	-	-	-	+	+	V_{DC}/n
2	-	+	-	-	-	-	+	-	0
3	-	+	-	+	+	-	+	-	0
4	-	-	-	+	+	-	-	-	0
5	-	-	+	+	+	+	-	-	$-V_{DC}/n$
6	-	-	+	-	-	+	-	-	0
7	+	-	+	-	-	+	-	+	0
8	+	-	-	-	-	-	-	+	0

Table1.Switching table

B. Zvzcs DC-DC Converter Operation Modes

The figure 1.shows the equivalent circuit for the eight operational modes. The following analysis is assumes that the switching period, and the blocking capacitor is large enough to act as a constant voltage source while the current is being reset.

(a)Operational Mode 1: ($t_0 \leq t \leq t_1$)

Switches S_1 and S_8 have been ON for a (relatively) long time and Cb_0 is charged to $-v_{cb0.}$ At t = 0, switches S_2 and S_7 being conducting and ($V_{dc} - v_{cb0}$) is applied to the primary of the transformer. As a result the primary current rapidly rises from 0 to the reflected output current.

$$I_{p0} = \frac{I_0}{n} \qquad (2)$$

Where I_{P0} is the peak value of the primary side current going into the transformer, I_0 is the Current through L_f, and n is the turn's ratio of the transformer. The voltage applied to the transformer leakage inductor L_{lk} during this period is

$V_{dc} - (- V_{cb0}) = V_{dc} + V_{cb0,}$ and the duration of this period is

$$t_1 - 0 = t_1 = \frac{L_{lk} * I_{p0}}{V_{dc} + V_{cbo}} \qquad (3)$$

Since this period is so short, V_{cb0} is assumed to be constant throughout the period. The load current is not completely supplied by V_{dc} during this period, so the excess current freewheels through the secondary rectifier diodes $D_{rec1} - D_{rec4.}$

$$T_{reset} = t_4 - t_3 = L_{lk} * \frac{I_{p0}}{V_{cbop}} \qquad (7)$$

(b)Operational Mode 2 :($t_1 \leq t < t_2$)

The freewheeling mode ends when the primary current reaches I_{p0} at t_1 and diodes D_{rec3} and D_{rec4} stop conducting.

(b) Operational Mode 2 : $t_1 \leq t < t_2$

The freewheeling mode ends when the primary current reaches I_{p0} at t_1 and diodes D_{rec3} and D_{rec4} stop conducting. The output filter is connected in series with the leakage inductance of the transformer through D_{rec1} and D_{rec2}, and acts to keep the primary current constant at I_{p0}. The duration of this mode is related to the voltage conversion ratio by the duty cycle parameter D, which is given by

$$\frac{V_0}{V_{dc}} = \frac{D}{n} = \frac{\left((t_{ON})\middle|(T_{sw}/2)\right)}{n} = \frac{(t_2 - t_1)/(T_{sw}/2)}{n} \qquad (4)$$

Since interval t_1 is so short, $t_{ON}$is set equal to t_2 and

$$D = \frac{t_2}{T_{sw}/2} \qquad (5)$$

(c) Operation Mode 3: ($t_2 \leq t < t_3$)

Switches S_1 and S_2 are turn OFF at t_2, and then S_5, S2, S7, S4 are turn ON. This is still held constant at Ipo by the large output filter inductance. The primary current begins to circulate through devices S_2 and S_7 diodes D_{c1} and D_{c4}. Switches $S_4$and S_5 can be gated ON under complete at any time after $t_{3.}$ Since this mode is so short,V_{cb0} is assumed to remain constant atV_{cb}

$$t_3 - t_2 = c_r * \frac{V_{dc}}{I_{p0}} \qquad (6)$$

(d) Operation Mode 4: ($t_3 \leq t < t_4$)

As the primary current circulates through S4, S5, and the blocking capacitor voltage Vcb0p is applied to the transformer and the primary current begins to decrease. As soon as the primary current falls below I_{p0}, the output current begins to freewheel through the output rectifier diodes, disconnecting the primary side of the circuit from the load and short circuiting the transformer magnetizing inductance.

(e) Operational Mode 5: ($t_4 \leq t < t_5$)

Upon reaching zero, the current is prevented from flowing in the negative direction by the diodes D_2 and D_7. The output current continues to freewheel through the

output rectifier diodes. The voltage The voltage *Vcb*0*p* appears across the output terminals *AB*, so *S*1 and *S*8 have to block (*V*dc + *Vcb*0*p*)/2. At *T*sw/2, *S*2 and *S*7 turn OFF under ZCS, and shortly afterward, *S*3 and *S*6 turn ON under ZCS. Since *S*4 and *S*5 are already ON, *S*3 and *S*6 conduct, and (−*V*dc + *Vcb*0*p*) is applied to the primary of the transformer.

(f) Operational Mode 6:($t_5 \le t < t_6$)

Here the switches *S*3 and *S*6 being conducting, each of the parallel capacitors conducts $I_{p0}/2$ during this mode and has change of voltage of Vdc/2. Using the same value C_r for capacitors C1, C4, C5 and C_8 the duration of this mode is

$$c_r * \frac{V_{dc}}{I_{p0}} \qquad (8)$$

(g) Operational Mode 7:($t_6 \le t < t_7$)

Here the switches *S*1 and *S*6 being conducting. And the switches *S*3 and *S*8 are ON state. The output voltage is – **V_{dc}.** And here the rectifying diodes do not conduct.

(h) Operational Mode 8:($t_7 \le t < t_8$)

In this mode the switches *S*3 and *S*6 are off state, and the switchesS1, S8 are ON. The capacitor **C_{ss2}** conduct. The output current continues to freewheel through the output rectifier diodes. And the switches *S*3 and *S*6 are off under the ZCS condition.

C. Design Equations

The design of the converter involves determining values for *C*dc1, *C*dc2, *C*ss1, *C*ss2, *C*1, *C*4, *C*5, *C*8, The output filter should be large enough to maintain the load current for the entire switching period *T*sw, while the Fig. 2 shows that they conduct during mode 3 and its mirror, mode 8. These capacitors must maintain a near-constant voltage during the entire cycle; thus, they should be selected so that they do not experience more than a 5%voltage change during mode 3. Therefore, the capacitor value required for a 5%ripple is

$$C_{SS} = \frac{I_{P0} * (t_3 - t_2)}{0.05 * V_{dc}} \qquad (9)$$

This can be simplified using ,

$$t_3 - t_2 = \frac{V_{dc}}{I_{p0}} \qquad (10)$$

so that,

$$C_{SS} = \frac{C_r}{0.05} = 20 * C_r \qquad (11)$$

The size of the parallel capacitors, *Cr*, is determined by the minimum requirement to achieve ZVS during turn-OFF, which requires that the parallel capacitors must be large enough to hold the voltage close to zero during the current fall-time of the device t_{fi}, which can be determined from the data sheet. Once this parameter has been determined, *Cr* can be calculated as follows

$$C_r = \frac{t_{fi} * I_{p0}}{V_{dc}} \qquad (12)$$

The blocking capacitor will reach its largest value when the converter is transferring maximum rated power and I_p is at I_{p0max}. In order to meet the voltage restriction outlined earlier for these conditions, Cb0 should be chosen as

$$C_{b0} = \frac{5 * I_{P0.max} * D_{max}}{4 * f_{sw} * V_{dc}} \qquad (13)$$

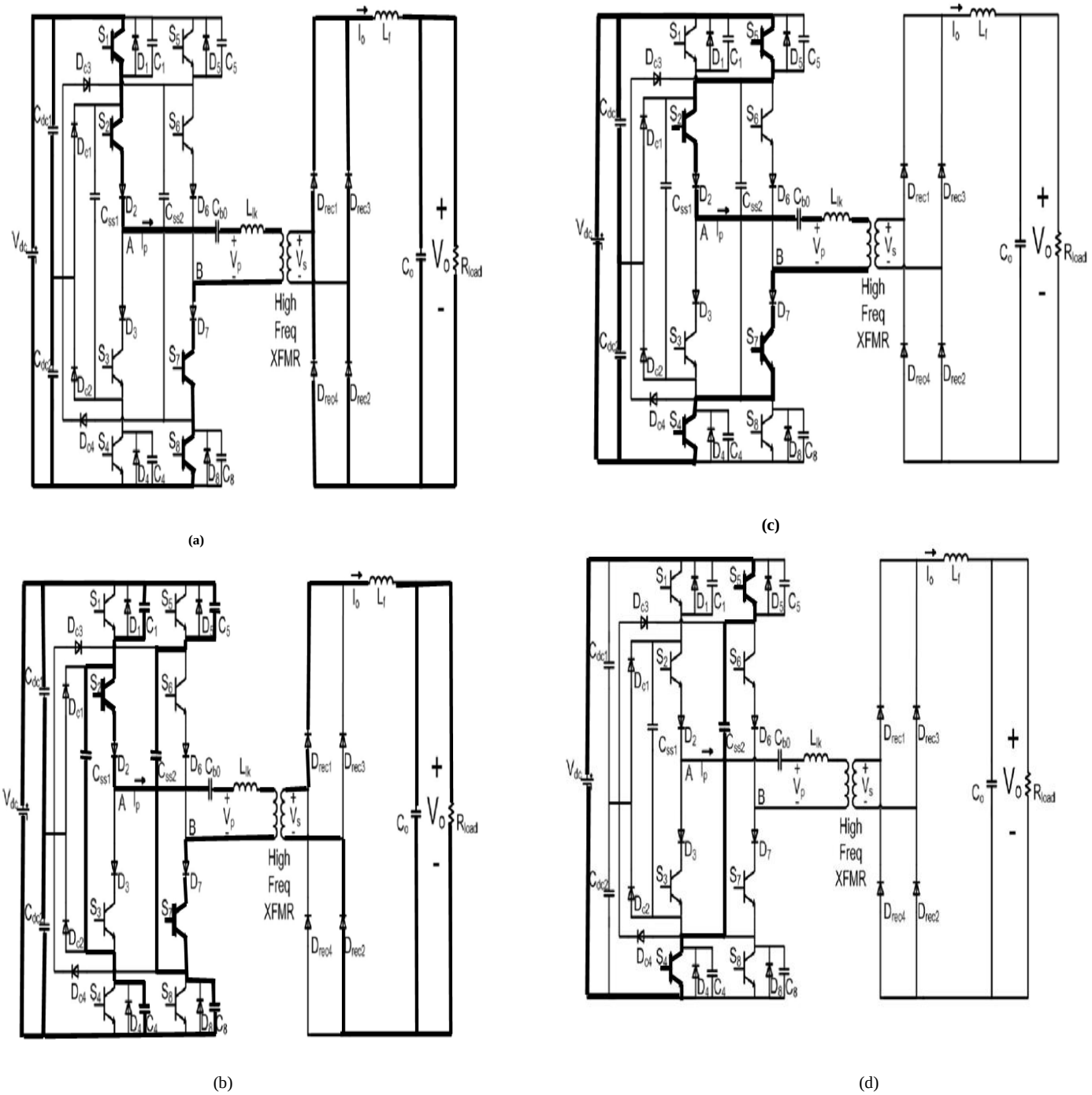
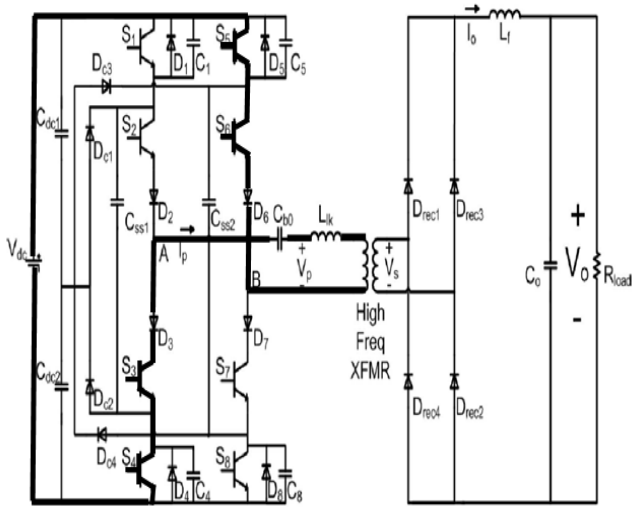
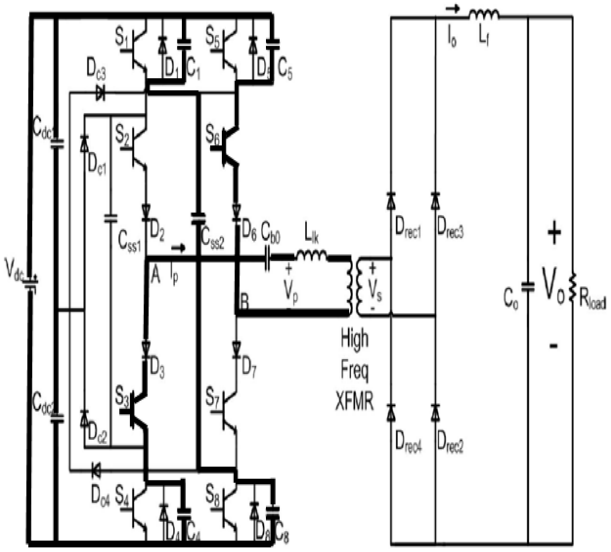


Fig 3. Operational modes of the ZVZCS 3L FB converter (a) $t_0 \leq t \leq t_1$ (b) $t_1 \leq t < t_2$ (c) $t_2 \leq t < t_3$ (d) $t_3 \leq t < t_4$



(e)



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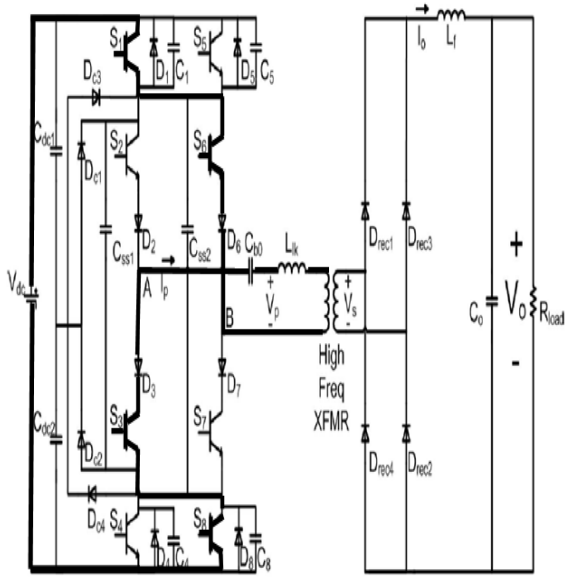

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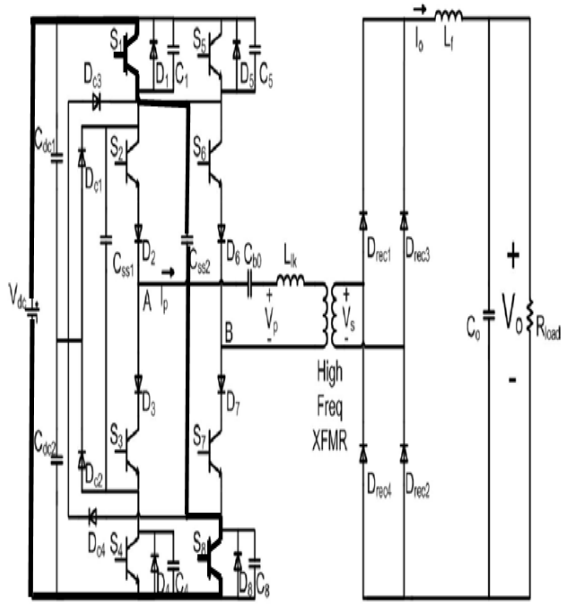

(h)

Fig 4 Operational modes of the ZVZCS 3L FB converter.(e) $t_4 \leq t < t_5$,(f)$t_5 \leq t < t_6$,(g) $t_6 \leq t < t_7$,(h)$t_7 \leq t < t_8$

D. Soft-Switching Range

ZVS is accomplished when I_{p0} discharges the parallel capacitors across the leading switches during mode 3. The length of mode 3, referred to as the dead time, limits the maximum duty cycle that can be commanded by the controller, which, in turn, limits the maximum voltage that can be achieved on the secondary and the maximum power that can be delivered to the load. Since ZVS, and hence the dead time, occurs twice per half cycle, the maximum duty cycle is

$$D_{max} = 1 - 2 * \frac{t_{dead}}{T_{sw}/2} \qquad (14)$$

Once the dead time is fixed, there is a minimum value of the load current under which ZVS no longer occurs since the leading switches will be switched before the parallel capacitors are completely discharged. This minimum load current is given by

$$I_{p0,min} = C_r * \frac{V_{dc}}{t_{dead}} \qquad (15)$$

ZCS is accomplished when the blocking capacitor voltage drives the primary current to zero before the state change that occurs at $T_{sw}/2$. The current begins to be reset at $t_2 = D \times T_{sw}/2$, so the total time available to reset the current is

$$T_{reset,max} = (1 - D) * \frac{T_{sw}}{2} \qquad (16)$$

ZCS will be achieved if the reset period from (6) is less than *T* reset, max, and using the value for $_{Vcb0p}$from (12)

$$\frac{4 * f_{sw} * C_{b0} * L_{lk}}{D} \leq (1 - D) * \frac{T_{sw}}{2} \qquad (17)$$

It can be seen from this equation that achieving ZCS is independent of the load current, though the voltage across *Cb*0 may become very large if the primary current exceeds the maximum load current used in (10) to calculate the value of the blocking capacitor. There is a limit on the range of duty cycles for which ZCS occurs, given by

$$\frac{1 - \sqrt{1 - 32 * f_{sw}^2 * C_{b0} * L_{lk}}}{2} \leq D \leq \frac{1 + \sqrt{1 - 32 * f_{sw}^2 * C_{b0} * L_{lk}}}{2} \qquad (18)$$

III. Simulation Results For ZVS Three Level DC-DC Converter

In the fig.5 Simulink model, a 100V/20V DC-DC converter has been proposed. In the proposed converter there are totally eight switches. In the positive half cycle diagonal four switches (S1, S2, S7 and S8) will operate and input voltage is applied to primary of the transformer. Similarly in the negative half cycle other diagonal four switches (S3, S4, S5 and S6) will operate and negative voltage is applied to the primary of the transformer. During the switching transitions all the switches operate under soft switching technique. In the proposed model the four outer switches (S1, S4, S5 and S8) operate under ZVS condition and the remaining inner four switches (S2, S3, S6 andS7) operate under ZCS condition. During the switching transitions all the switches operate under soft switching technique.

$$I_{p0,min} = C_r * \frac{V_{dc}}{t_{dead}} \qquad (19)$$

Fig 7(a) shows the voltage across switches S4/S5. When the pulse is given the voltage across the switch is zero and when pulse is removed the voltage across the switch is $V_{dc}/2$. Fig 7(b) shows ZVS turn-OFF condition of switches S4/S5 and Fig 7(c) shows ZVS turn-ON condition of switches S4/S5.

Fig 8(a) shows the current through switch. When the pulse is given to switch current starts flowing through it.before removing pulse to switch current coming zero. Fig 8(b) shows ZCS turn-ON condition of switches S3/S6 and Fig 8(c) shows ZCS turn-OFF condition of switches S3/S6.

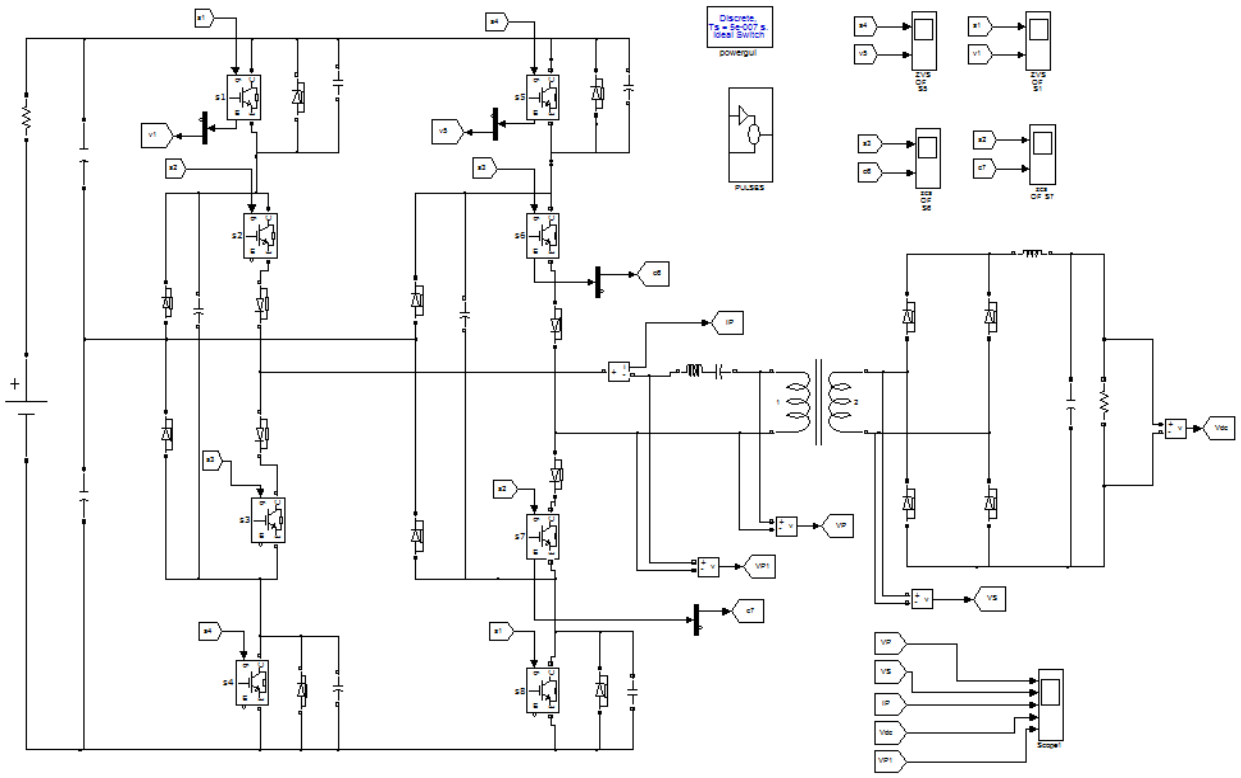

Figure.5.Simulink diagram of Three-Level ZVZCS DC-DC converter

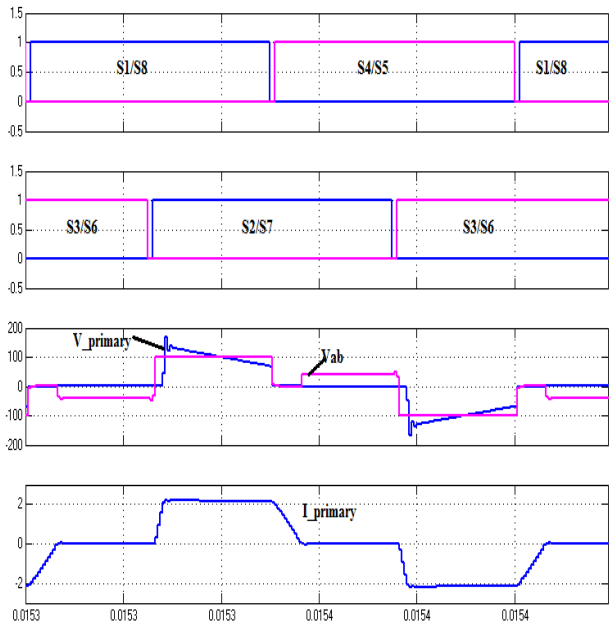

Figure.6.Operational waveforms of proposed converter

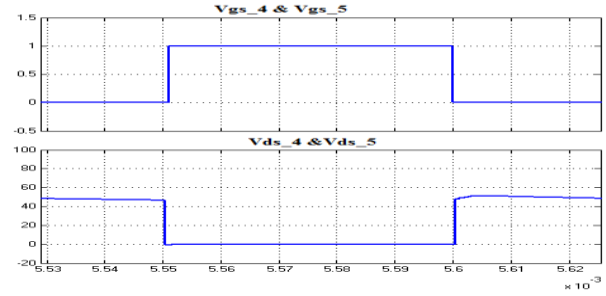

Fig.7(a)

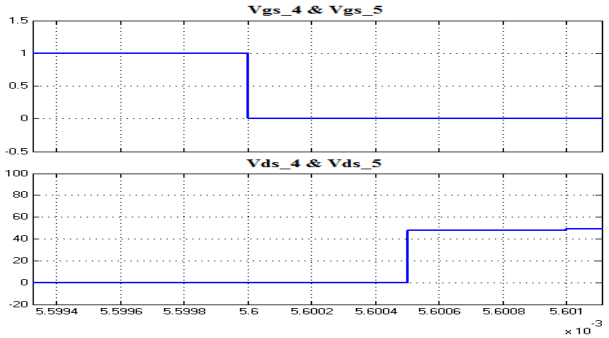

Fig.7(b)

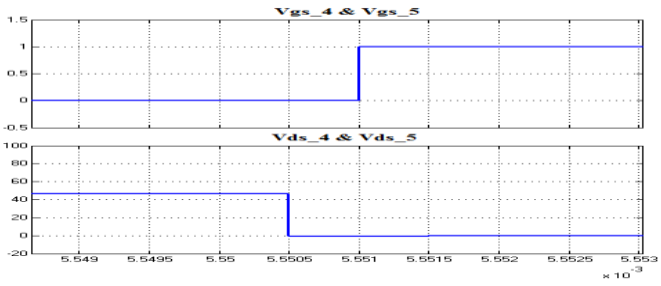

Fig.7(c)

Figure.7 simulation (a) voltage across switches S4/S5 (b) ZVS S4/S5 turn-ON (c) ZVS S4/S5 turn-OFF

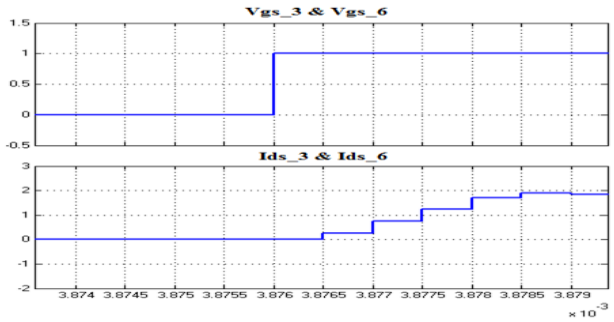

Fig8(a)

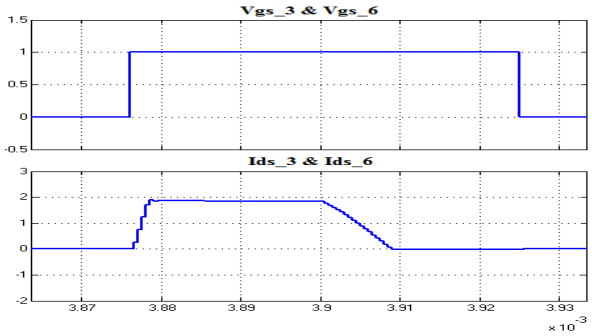

Fig8(b)

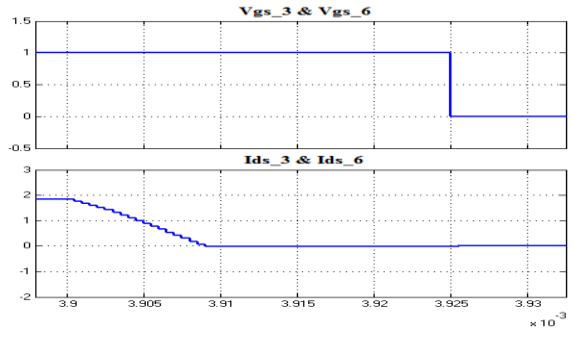

Fig8(c)

Figure.8.simulation (a) current through switch (b) ZCS S3/S6 turn-ON (c) ZCS S3/S6 turn-OFF

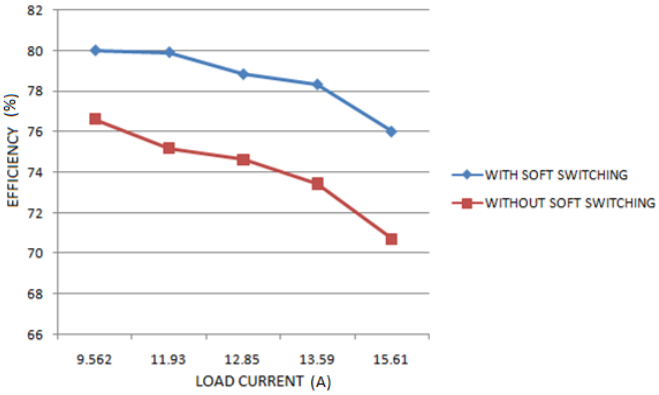

Fig 9. Efficiency for different load currents

Efficiency for various load currents for three level dc-dc converters with and without zero voltage switching scheme. For the same current (9.562A) flow in the converter circuit, the efficiency (75.63%) is less by applying without ZVS and efficiency is more (80.1%) in case of by applying ZVS.

IV. CONCLUSION

Resonant converter topologies can be used to increase circuit switching speeds, allowing the cost of circuit magnetic to be reduced, while still keeping switching losses to a minimum. Capacitive switching losses when turning on with a high drain-source voltage means that MOSFETs are more suitable for Zero -Voltage than Zero-Current switches, while it spoor turn-off characteristics mean that the IGBT is more suited to Zero-Current topologies. The transient response can be very fast compared to conventional designs, and the converter is especially well suited to on-off control.
Soft switching scheme is achieved in each and every switch. Voltage stress across each switch was reduced. By increasing the voltage levels the size of the filter elements may also reduced. The switching losses in the proposed converter are reduced. The proposed converter has the advantage of applying full dc bus voltage for the entire operating range.

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