MULTICONVERTER – UNIFIED POWER QUALITY CONDITIONING SYSTEM (MC-UPQC)

Tirupathi Rao B[1], Sri. P.K.S. Sarvesh[2]
[1]*M. Tech scholar, Lakireddy Balireddy College of Engineering, Vijayawada, India*
[2]*M. Tech, Assistance Professor, Lakireddy Balireddy College of Engineering, Vijayawada, India*

***Abstract*- In this paper, a new configuration of a UPQC called the multi converter unified power-quality conditioner (MC-UPQC) is presented. The system is extended by adding a series-VSC in an adjacent feeder. The proposed topology can be used for simultaneous compensation of voltage and current imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. The system is also capable of compensating for interruptions without the need for a battery storage system and consequently without storage capacity limitations. The results were obtained by using matlab/simulink.**

***Index Terms*- Power quality (PQ), unified power-quality conditioner(UPQC),voltage-source converter (VSC).**

I. INTRODUCTION

In order to meet PQ standard limits, it may be necessary to include some sort of compensation. Modern solutions can be found in the form of active rectification or active filtering. A shunt active power filter is suitable for the suppression of negative load influence on the supply network, but if there are supply voltage imperfections, a series active power filter may be needed to provide full compensation. In recent years, solutions based on flexible ac transmission systems (FACTS) have appeared.

Recently, multi converter FACTS devices, such as an interline power-flow controller (IPFC) and the generalized unified power-flow controller (GUPFC) are introduced. The aim of these devices is to control the power flow of multiline or a sub network rather than control the power flow of a single line by, for instance, a UPFC. When the power flows of two lines starting in one substation need to be controlled, an interline power flow controller (IPFC) can be used. An IPFC consists of two series VSCs whose dc capacitors are coupled. This allows active power to circulate between the VSCs. With this configuration, two lines can be controlled simultaneously to optimize the network utilization. The GUPFC combines three or more shunt and series converters. It extends the concept of voltage and power-flow control beyond what is achievable with the known two-converter UPFC. The simplest GUPFC consists of three converters one connected in shunt and the other two in series with two transmission lines in a substation.

In this paper, a new configuration of a UPQC called the multi converter unified power-quality conditioner (MC-UPQC) is presented. The system is extended by adding a series-VSC in an adjacent feeder. The proposed topology can be used for simultaneous compensation of voltage and current imperfections in both feeders by sharing power compensation capabilities between two adjacent feeders which are not connected. The system is also capable of compensating for interruptions without the need for a battery storage system and consequently without storage capacity limitations.

II. PROPOSED MC-UPQC SYSTEM

A. Circuit Configuration

The single-line diagram of a distribution system with an MC-UPQC is shown in Fig.2.1

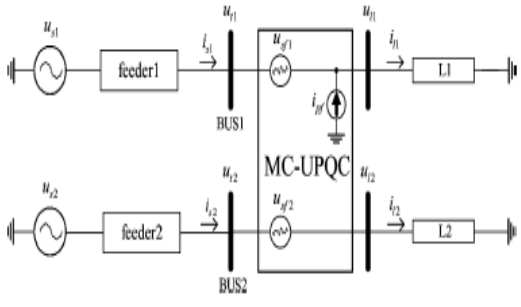

Fig.2.1 Single-line diagram of a distribution system with an MC-UPQC.

As shown in this figure 2.1, two feeders connected to two different substations supply the loads L1 and L2. The MC-UPQC is connected to two buses BUS1 and BUS2 with voltages of $u_{t1}$and u_{t2}, respectively. The shunt part of the MC-UPQC is also connected to load L1 with a current of u_{l1}. Supply voltages are denoted by $u_{s1}\, and\, u_{s2}$while load voltages are $u_{l1}\, and\, u_{l2}$. Finally, feeder currents are denoted by $i_{s1}\, and\, i_{s2}$ and load currents are $i_{l1}\, and\, i_{l2}$,

B. MC–UPQC Structure

The internal structure of the MC–UPQC is shown in Fig.2.2. It consists of three VSCs (VSC1, VSC2, and VSC3) which are connected back to back through a common dc-link capacitor. In the proposed configuration, VSC1 is connected in series with BUS1 and VSC2 is connected in parallel with load L1 at the end of Feeder1. VSC3 is connected in series with BUS2 at the Feeder2 end. Each of the three VSCs in Fig.2.2 is realized by a three-phase converter with a commutation reactor and high-pass output filter as shown in Fig.2.3

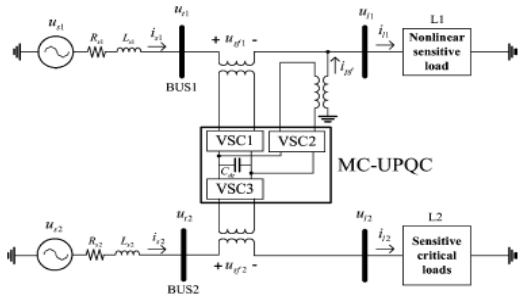

Fig.2.2 Typical MC-UPQC used in a distribution system.

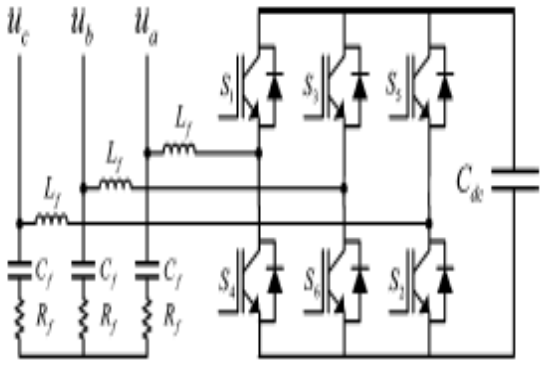

Fig.2.3 Schematic structure of a VSC.

The commutation reactor (L_f) and high- pass output filter $(R_f, C_f)$are connected to prevent the flow of switching harmonics into the power supply. As shown in Fig.1.2, all converters are supplied from a common dc-link capacitor and connected to the distribution system through a transformer. Secondary (distribution) sides of the series-connected transformers are directly connected in series with BUS1 and BUS2, and the secondary (distribution)side of the shunt-connected transformer is connected in parallel with load L1. The aims of the MC-UPQC shown in Fig.1.2 are:

1) to regulate the load voltage (u_{l1}) against sag/swell and disturbances in the system to protect the nonlinear/sensitive load L1;

2) to regulate the load voltage (u_{l2}) against sag/swell, interruption, and disturbances in the system to protect the sensitive/ critical load L2; to compensate for the reactive and harmonic components of nonlinear load current(i_{l1}). In order to achieve these goals, series VSCs (i.e., VSC1 and VSC3) operate as voltage controllers while the shunt VSC (i.e., VSC2) operates as a current controller.

C. Control Strategy

As shown in Fig.2.2, the MC-UPQC consists of two series VSCs and one shunt VSC which are controlled independently. The switching control strategy for series VSCs and the shunt VSC are selected to be sinusoidal pulse width-modulation (SPWM) voltage control and hysteresis current control, respectively. Details of the control algorithm, which are based on the d–q method,

(a) Shunt-VSC:

Functions of the shunt-VSC are:

1) to compensate for the reactive component of load L1 current;

2) to compensate for the harmonic components of load L1 current;

3) to regulate the voltage of the common dc-link capacitor.

The measured load current $i_{l_{abc}}$ is transformed into the synchronous dq0 reference frame by using

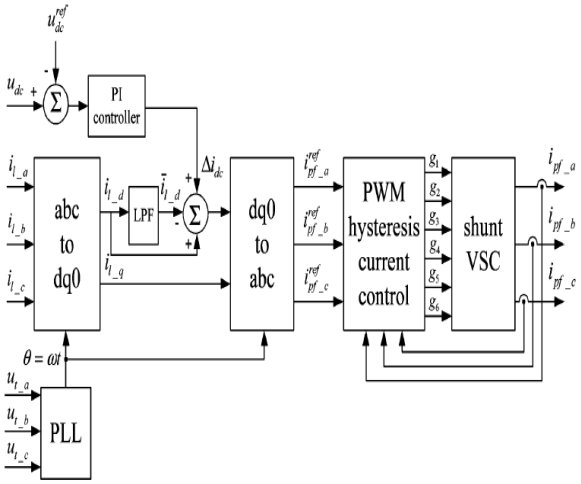

Fig.2.4 control block diagram for the shunt VSC.

$$i_{l\_dq0} = T_{abc}^{dq0} i_{l\_abc} \tag{2.1}$$

$$T_{abc}^{dqo} = \frac{2}{3}\begin{bmatrix} \cos(wt) & \cos(wt-120^0) & \cos(wt+120^0) \\ -\sin(wt) & -\sin(wt-120^0) & -\sin(wt+120^0) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.2}$$

where the transformation matrix is shown in (2.2),.By this transform, the fundamental positive-sequence component, which is transformed into dc quantities in the d and q axes, can be easily extracted by low-pass filters (LPFs). Also, all harmonic components are transformed into ac quantities with a fundamental frequency shift

$$i_{l\_d} = \bar{i}_{l\_d} + i_{l\_d} \tag{2.3}$$

$$i_{l\_q} = \bar{i}_{l\_q} + i_{l\_q} \tag{2.4}$$

Where, i_{l_d}, i_{l_q} are d-q components of load current, $\bar{i}_{l\_d}$, $\bar{i}_{l\_q}$ are dc components, and $\tilde{i}_{l\_d}$, $\tilde{i}_{l\_q}$ are the ac components of $\bar{i}_{l\_d}$, $\bar{i}_{l\_q}$. If i_s is the feeder current and i_{pf} is the shunt VSC current and knowing , $i_s = i_l - i_{pf}$,then d–q components of the shunt VSC reference current are defined as follows:

$$i_{pf\_d}^{ref} = i_{l_d} \tag{2.5}$$

$$i_{pf\_q}^{ref} = i_{l\_q} \tag{2.6}$$

Consequently, the d–q components of the feeder current are

$$i_{s\_d} = \tilde{i}_{l\_d} \tag{2.7}$$

$$i_{s\_q} = 0 \tag{2.8}$$

This means that there are no harmonic and reactive components in the feeder current. Switching losses cause the dc-link capacitor voltage to decrease. Other disturbances, such as the sudden variation of load, can also affect the dc link. In order to regulate the dc-link capacitor voltage, a proportional–integral (PI) controller is used as shown in Fig.2.4. The input of the PI controller is the error between the actual capacitor voltage (U_{dc}) and its reference- value.u_{dc}^{ref} .The output of the PI controller i.e.,$(\Delta i_{dc})$is added to the d component of the shunt-VSC reference current to form a new reference current as follows:

$$\begin{cases} i_{pf\_d}^{ref} = i_{l\_d} = \Delta i_{dc} \\ i_{pf\_q}^{ref} = i_{l\_q} \end{cases} \tag{2.9}$$

As shown in Fig.2.4, the reference current in (2.9) is then transformed back into the abc reference frame. By using PWM hysteresis current control, the output-compensating currents in each phase are obtained

$$i_{pf\_abc}^{ref} = T_{dq0}^{abc} i_{pf\_dq0}^{ref} \; ; \; \left(T_{dq0}^{abc} = T_{abc}^{dq0\_1}\right) \tag{2.10}$$

(b) Series-VSC:

Functions of the series VSCs in each feeder are:
1) to mitigate voltage sag and swell,
2) to compensate for voltage distortions, such as harmonics, and
3) to compensate for interruptions (in Feeder2 only).

The control block diagram of each series VSC is shown in Fig.2.5. The bus voltage u_{t_abc} is detected and then transformed into the synchronous dq0 reference frame using

$$u_{t\_dq0} = T_{abc}^{dq0} u_{t\_abc} = u_{t1p} + u_{t1n} + u_{t10} + u_{t1h} \tag{2.11}$$

Where,

$$\begin{cases} u_{t1p} = [u_{t1p\_d} \quad u_{t1p\_q} \quad 0]^T \\ u_{t1n} = [u_{t1n\_d} \quad u_{t1n\_q} \quad 0]^T \\ u_{t10} = [0 \quad 0 \quad u_{00}]^T \\ u_{th} = [u_{th\_d} \quad u_{th\_q} \quad u_{th\_0}]^T \end{cases} \tag{2.12}$$

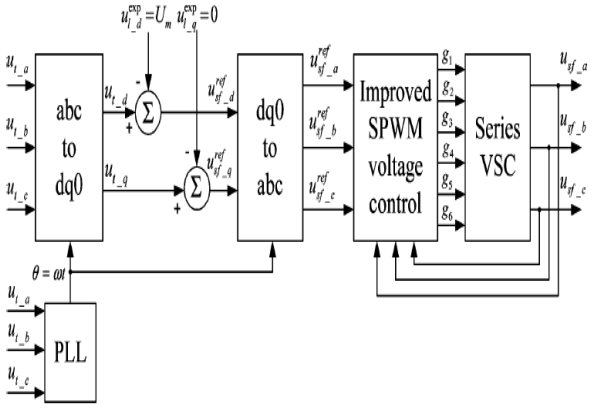

Fig.2.5 control block diagram for the shunt VSC.

$u_{t1p}, u_{t1n}, u_{t10}$ are fundamental frequency positive-, negative-, and zero-sequence components, respectively, and u_{tl} is the harmonic component of the bus voltage. According to control objectives of the MC-UPQC, the load voltage should be kept sinusoidal with a constant amplitude even if the bus voltage is disturbed. Therefore, the expected load voltage in the synchronous dq0 reference frame $\left(u_{t\_dq0}^{exp}\right)$ only has one value.

$$u_{l\_dq0}^{exp} = T_{abc}^{dq0} u_{t\_abc}^{exp} = \begin{bmatrix} U_m \\ 0 \\ 0 \end{bmatrix} \qquad (2.13)$$

where the load voltage in the abc reference frame $\left(u_{t\_abc}^{exp}\right)$ is

$$u_{l\_abc}^{exp} = \begin{bmatrix} U_m \cos(wt) \\ U_m \cos(wt - 120^0) \\ U_m \cos(wt + 120^0) \end{bmatrix} \qquad (2.14)$$

The compensating reference voltage in the synchronous dq0 reference frame $\left(u_{sf\_dq0}^{ref}\right)$ is defined as

$$u_{sf\_dq0}^{ref} = u_{t\_dq0} - u_{l\_dq0}^{exp} \qquad (2.15)$$

This means u_{t1p_d} in (2.12) should be maintained at $U_m$while all other unwanted components must be eliminated. The compensating reference voltage is then transformed back into the abc reference frame. By using an improved SPWM voltage control technique (sine PWM control with minor loop feedback), the output compensation voltage of the series VSC can be obtained.

III. POWER-RATING ANALYSIS OF THE MC-UPQC

The power rating of the MC-UPQC is an important factor in terms of cost. Before calculation of the power rating of each VSC in the MC UPQC structure, two models of a UPQC are analyzed and the best model which requires the minimum power rating is considered. All voltage and current phasors used in this section are phase quantities at the fundamental frequency. There are two models for a UPQC- quadrature compensation (UPQC-Q) and inphase compensation (UPQC-P). In the quadrature compensation scheme, the injected voltage by the series- VSC maintains a quadrature advance relationship with the supply current so that no real power is consumed by the series VSC at steady state. This is a significant advantage when UPQC mitigates sag conditions. The series VSC also shares the volt ampere reactive (VAR) of the load along with the shunt-VSC, reducing the power rating of the shunt-VSC.

Fig.3.1 shows the phasor diagram of this scheme under a typical load power factor condition with and without a voltage sag.

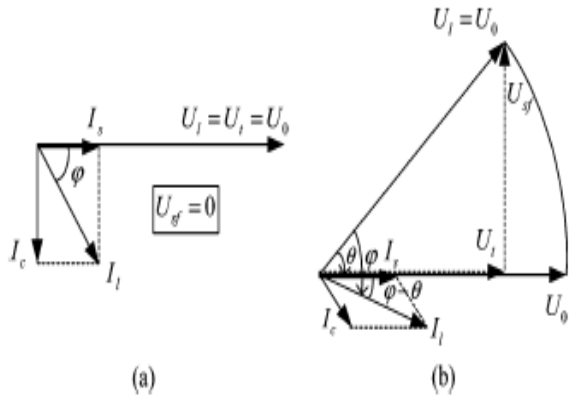

Fig.3.1 Phasor diagram of quadrature compensation. (a) Without voltage sag. (b) With voltage sag.

When the bus voltage is at the desired value , $U_l = U_t = U_0$ the series-injected voltage U_{sf} is zero [Fig.3.1(a)]. The shunt VSC injects the reactive component of load current I_c, resulting in unity input-power factor. Furthermore, the shunt VSC compensates for not only the reactive component, but also the harmonic components of the load current I_c. For sag compensation in this model, the quadrature series voltage injection is needed as shown in Fig.

3.1(b). The shunt VSC injects I_c in such a way that the active power requirement of the load is only drawn from the utility which results in a unity input-power factor. In an inphase compensation scheme, the injected voltage is inphase with the supply voltage when the supply is balanced. By virtue of inphase injection, series VSC will mitigate the voltage sag condition by minimum injected voltage. The phasor diagram of Fig.3.2 explains the operation of this scheme in case of a voltage sag.

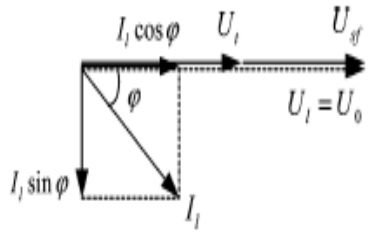

Fig.3.2 Phasor diagram of inphase compensation (supply voltage sag).

A comparison between in phase (UPQC-P) and quadrature (UPQC-Q) models is made for different sag conditions and load power factors. It is shown that the power rating of the shunt-VSC in the UPQC-Q model is lower than that of the UPQC-P, and the power rating of the series-VSC in the UPQC-P model is lower than that of the UPQC-Q for a power factor of less than or equal to 0.9. Also, it is shown that the total power rating of UPQC-Q is lower than that of UPQC-P where the VAR demand of the load is high.

The power needed for interruption compensation in Feeder2 must be supplied through the shunt VSC in Feeder1 and the series VSC in Feeder2. This implies that power ratings of these VSCs are greater than that of the series one in Feeder1. If quadrature compensation in Feeder1 and inphase compensation in Feeder2 are selected, then the power rating of the shunt VSC and the series VSC (in Feeder2) will be reduced. This is an important criterion for practical applications.

The load power factors in Feeder1 and Feeder2 are assumed to be $\cos\varphi_1$ *and* $\cos\varphi_2$ and the per-unit sags, which must be compensated in Feeder1 and Feeder2, are supposed to be x1 and x2, respectively.

If the MC-UPQC is lossless, the active power demand supplied by Feeder1 consists of two parts:

1) the active power demand of load in Feeder1;

2) the active power demand for sag and interruption compensation in Feeder2.

Thus, Feeder1 current I_{01} can be found as

$$U_{t1}I_{s1} = U_{l1}I_{l1}\cos\varphi_1 + U_{sf2}I_{l2}\cos\varphi_2 \qquad (3.1)$$

$$I_{s1} = \frac{I_{01}\cos\varphi_1}{(1-\mathcal{X}_1)} + \frac{\mathcal{X}_2 I_{02}\cos\varphi_2}{(1-\mathcal{X}_1)} \qquad (3.2)$$

From Fig., the voltage injected by the series VSC in Feeder1 and thus the power rating of this converter (S_{VSC1}) can be calculated as

$$S_{VSC1} = 3U_{sf1}I_{s1} = 3U_0(1-\mathcal{X}_1)\tan\theta \times \left(\frac{I_{01}\cos\varphi_1}{1-\mathcal{X}_1} + \frac{\mathcal{X}_2 I_{02}\cos\varphi_2}{1-\mathcal{X}_1}\right) \qquad (3.3)$$

The shunt VSC current is divided into two parts.

1) The first part (i.e.,I_{cl}) compensates for the reactive component (and harmonic components) of Feeder1 current and can be calculated from Fig. as

$$I_{c1} = \sqrt{I_{l1}^2 + I_{s1}^2 - 2I_{l1}I_{s1}\cos(\varphi_1-\theta)}$$
$$= \sqrt{I_{01}^2 + I_{s1}^2 - 2I_{01}I_{s1}\cos(\varphi_1-\theta)} \qquad (3.4)$$

Where, I_{s1} is calculated. This part of the shunt VSC current only exchanges reactive power (Q) with the system.

2) The second part provides the real power (P), which is needed for a sag or interruption compensation in Feeder2. Therefore, the power rating of the shunt VSC can be calculated as

$$S_{VSC2} = 3U_{l1}I_{pf} = 3\sqrt{Q^2+P^2}$$
$$= 3\sqrt{(U_{l1}I_{C1})^2 + (U_{sf2}I_{l2}\cos\varphi_2)^2}$$
$$= 3U_0\sqrt{I_{c1}^2 + \mathcal{X}_2 I_{02}\cos\varphi_2)^2} \qquad (3.5)$$

Where, I_{C1} is calculated. Finally, the power rating of the series-VSC in Feeder2 can be calculated. For the worst-case scenario (i.e., interruption compensation), one must consider $\mathcal{X}_2 = 1$. Therefore

$$S_{VSC3} = 3U_{sf2}I_{l2} = 3\mathcal{X}_2 U_0 I_{02} \qquad (3.6)$$

IV. SIMULATION RESULTS

The proposed MC-UPQC and its control schemes have been tested through extensive case study simulations using matlab⁄simulation. In this section, simulation results are presented, and the performance of the proposed MC-UPQC system is shown.

A. Distortion and Sag/Swell on the Bus Voltage

Let us consider that the power system in Fig. 3.2 consists of two three-phase three-wire 380(v) (rms, L-L), 50-Hz utilities. The BUS1 voltage (U_{t1}) contains the seventh-order harmonic with a value of 22%, and the BUS2 voltage (U_{t2}) contains the fifth order harmonic with a value of 35%. The BUS1 voltage contains 25% sag between $0.1s < t < 0.2s$ and 20% swell between $0.2s < t < 0.3s$. The BUS2 voltage contains 35% sag between $0.15s < t < 0.25s$ and 30% swell between$0.25s < t < 0.3s$. The nonlinear/sensitive load L1 is a three-phase rectifier-load which supplies an RC load of 10Ω and 30 F. Finally, the critical load L2 contains a balanced RL load of 10Ω and 100mH. The MC–UPQC is switched on at t=0.02 s.

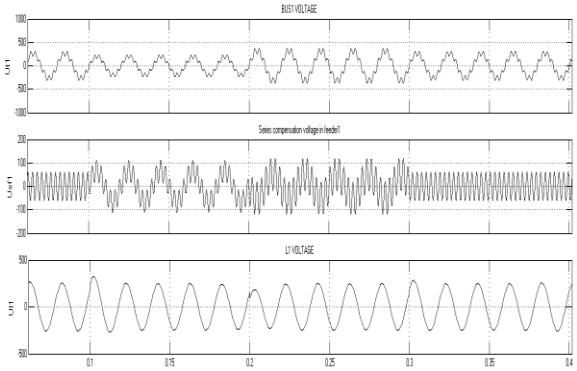

Fig.4.1 BUS1 voltage, series compensating voltage, and load voltage in Feeder1.

In all figures, only the phase a waveform is shown for simplicity. Similarly, the BUS2 voltage, the corresponding compensation voltage injected by VSC3, and finally, the load L2 voltage are shown in Fig.4.2

As shown in these figures 4.1 and 4.2, distorted voltages of BUS1 and BUS2 are satisfactorily compensated for across the loads L1 and L2 with very good dynamic response. The nonlinear load current, its corresponding compensation current injected by VSC2, compensated Feeder1 current, and, finally, the dc-link capacitor voltage are shown inFig.

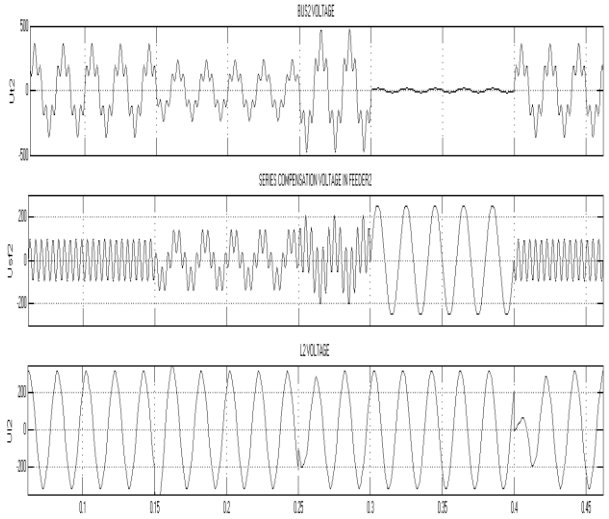

Fig.4.2 BUS2 voltage, series compensating voltage, and load voltage in Feeder2.

The distorted nonlinear load current is compensated very well, and the total harmonic distortion (THD) of the feeder current is reduced from 28.5% to less than 5%. Also, the dc voltage regulation loop has functioned properly under all disturbances, such as sag/swell in both feeders.

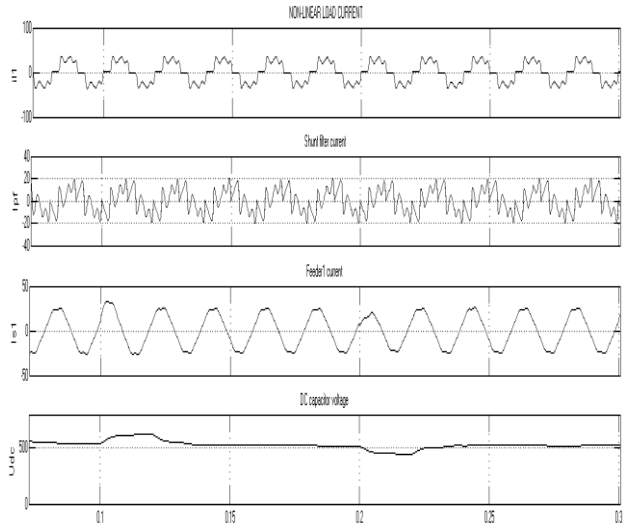

Fig.4.3 Nonlinear load current, compensating current, Feeder1 current, and capacitor voltage.

B. Upstream Fault on Feeder2

When a fault occurs in Feeder2 (in any form of L-G, L-L-G, and L-L-L-G faults), the voltage

across the sensitive/critical load L2 is involved in sag/swell or interruption. This voltage imperfection can be compensated for by VSC2. In this case, the power required by load L2 is supplied through VSC2 and VSC3. This implies that the power semiconductor switches of VSC2 and VSC3 must be rated such that total power transfer is possible. This may increase the cost of the device, but the benefit that may be obtained can offset the expense. In the proposed configuration, the sensitive/critical load on Feeder2 is fully protected against distortion, sag/swell, and interruption. Furthermore, the regulated voltage across the sensitive load on Feeder1 can supply several customers who are also protected against distortion, sag/swell, and momentary interruption. Therefore, the cost of the MC-UPQC must be balanced against the cost of interruption, based on reliability indices, such as the customer average interruption duration index (CAIDI) and customer average interruption frequency index (CAIFI). It is expected that the MC-UPQC cost can be recovered in a few years by charging higher tariffs for the protected lines. The performance of the MC-UPQC under a fault condition on Feeder2 is tested by applying a three-phase fault to ground on Feeder2 between 0.3s<t<0.4 s. Simulation results are shown in Fig.4.4

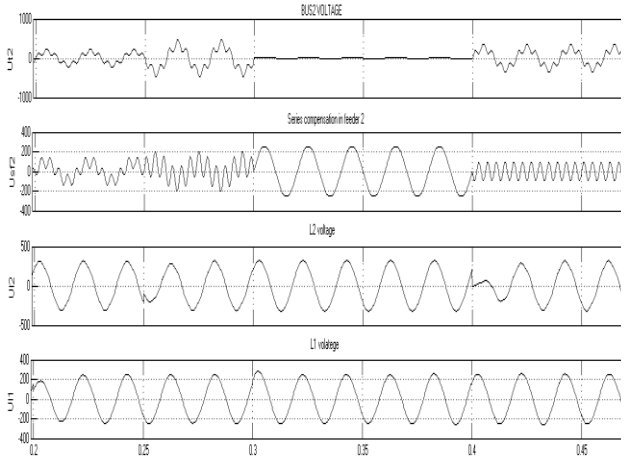

Fig.8.4 An upstream fault on Feeder2: BUS2 voltage, compensating voltage, and loads L1 and L2 voltages.

C. Load Change

To evaluate the system behaviour during a load change, the nonlinear load L1 is doubled by reducing its resistance to half at t=0.5s. The other load, however, is kept unchanged. The system response is shown in Fig.4.5

It can be seen that as load L1 changes, the load voltages u_{l1} *and* u_{l2} remain undisturbed, the dc bus voltage is regulated, and the nonlinear load current is compensated.

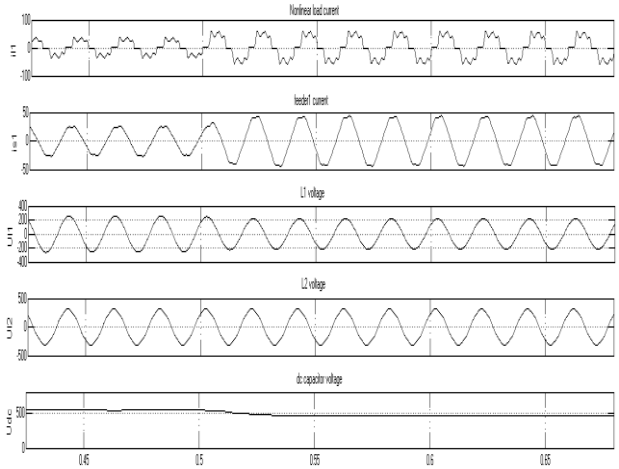

Fig.4.5 Load change: nonlinear load current, Feeder1 current, load L1 voltage, load L2 voltage, and dc-link capacitor voltage.

D. Unbalance Voltage

The control strategies for shunt and series VSCs , are based on the d–q method. They are capable of compensating for the unbalanced source voltage and unbalanced load current. To evaluate the control system capability for unbalanced voltage compensation, a new simulation is performed. In this new simulation, the BUS2 voltage and the harmonic components of BUS1 voltage are similar to those given in. However, the fundamental component of the BUS1 voltage ($U_{t1,fundamental}$) is an unbalanced three-phase voltage with an unbalance factor U_-/U_+ of 40%. This unbalance voltage is given by

$$\left(U_{t1,fundamental}\right) = \begin{bmatrix} 0.31\cos(wt + 46^0) \\ 0.31\cos(wt - 106^0) \\ 0.155\cos(wt - 210^0) \end{bmatrix} \quad (4.1)$$

The simulation results for the three-phase BUS1 voltage series compensation voltage, and load voltage in feeder 1 are shown in Fig.4.6

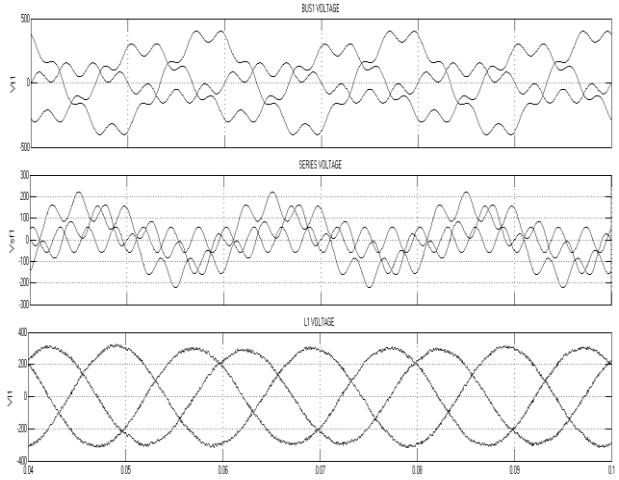

Fig.4.6 BUS1 voltage, series compensating voltage, and load voltage in Feeder1 under unbalanced source voltage.

The simulation results show that the harmonic components and unbalance of BUS1 voltage are compensated for by injecting the proper series voltage. In this figure 4.6, the load voltage is a three-phase sinusoidal balance voltage with regulated amplitude.

V. CONCLUSION

In this paper, a new configuration for simultaneous compensation of voltage and current in adjacent feeders has been proposed. The new configuration is named multi-converter unified power-quality conditioner (MC-UPQC). Compared to a conventional UPQC, the proposed topology is capable of fully protecting critical and sensitive loads against distortions, sags/swell, and interruption in two-feeder systems. The idea can be theoretically extended to multibus/multifeeder systems by adding more series VSCs. The performance of the MC-UPQC is evaluated under various disturbance conditions and it is shown that the proposed MC-UPQC offers the following advantages:

1) power transfer between two adjacent feeders for sag/swell and interruption compensation;

2) compensation for interruptions without the need for a battery storage system and, consequently, without storage capacity limitation;

3) sharing power compensation capabilities between two adjacent feeders which are not connected.

REFERENCES

[1] H. Fujita and H. Akagi, "The unified power quality conditioner: The integration of series and shunt active filters," IEEE Trans. Power Electron., vol. 13, no. 2, pp. 315–322, Mar. 1998.

[2] A. Ghosh and G. Ledwich, "A unified power quality conditioner (UPQC) for simultaneous voltage and current compensation," Elect. Power Syst. Res., pp. 55–63, 2001.

[3] M. Aredes, K. Heumann, and E. H. Watanabe, "An universal active power line conditioner," IEEE Trans. Power Del., vol. 13, no. 2, pp. 545–551, Apr. 1998.

[4] L. Gyugyi, K. K. Sen , and C. D. Schauder, "Interline power flow controller concept: A new approach to power flow management in transmission systems," IEEE Trans. Power Del., vol. 14, no. 3, pp. 1115–1123, Jul. 1999.

[5] B. Fardanesh, B. Shperling, E. Uzunovic, and S. Zelingher, "Multi-converter FACTS Devices: The generalized unified power flow controller (GUPFC)," in Proc. IEEE Power Eng. Soc. Summer Meeting, 2000, vol. 4, pp. 2511–2517.