© 2014 IJIRT | Volume 1 Issue 6 | ISSN : 2349-6002

Analog to Digital Converter in Wireless LAN

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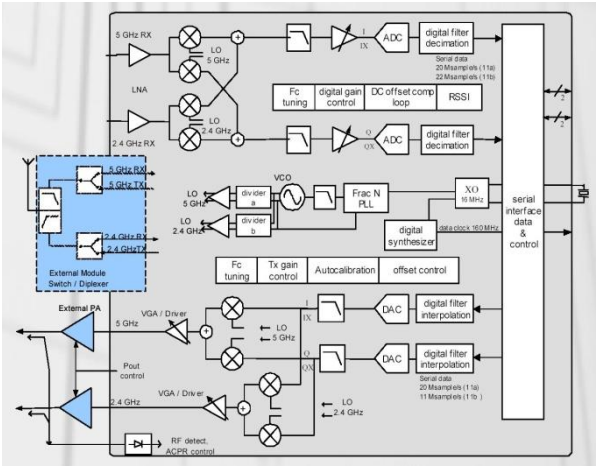
Abstract- **Most wireless broadband communications systems make use of a zero-IF (intermediate frequency) demodulation scheme for down conversion of the radio frequency signal into baseband frequencies. The outputs of the down-conversion are quadrature (I&Q) modulated analog baseband signals that can be digitized using a dual channel ADC in order to be more effectively processed in the digital baseband processor. Typical ADC resolution for these applications is in the 10 to 12-bit range. The "over-the-air", radio frequency channel bandwidth for broadband communication protocols, such as WiFi 802.11abg, LTE and WiMAX, can reach 20 MHz. The corresponding down-converted, quadrature modulated signals have, each, a bandwidth of up to 10 MHz. The IEEE 802.11a standard is the wireless local area network (WLAN) standard for tomorrow's high imposition communication world. However, battery life of the device is a major problem for today's user because everyone wants to avoid the need of frequently recharging the battery of the device, i.e. laptops. As a result, power consumption of the device has to be low while maintaining required or equal performance. Analog to digital converters (ADCs) are important power consumers in any device. Interpolation/averaging ADC aims toward a higher performance application, i.e. digitization of data before I and Q data separation; since interpolation ADC usually has higher power consumption but faster conversion rate. These two ADC architectures are in active research today as better trade off between power consumption and performance is demanded by the future.**

Index Terms- **WLAN, IEEE 802.11, ADC, Analog.**

I. INTRODUCTION

A **wireless network** is any type of computer network that uses wireless data connections for connecting network nodes. Wireless networking is a method by which homes, telecommunications networks and enterprise (business) installations avoid the costly process of introducing cables into a building, or as a connection between various equipment location. Wireless telecommunications networks are generally implemented and administered using radio communication. This implementation takes place at the physical level (layer) of the OSI model network structureIEEE 802.11a is a standard that was approved by the IEEE committee back in 1999. It is a standard based on coded orthogonal frequency-division multiplexing (OFDM) modulation and it provides two to five times the data rate and as much as ten times the system capacity than its predecessor, IEEE 802.11b. The IEEE 802.11a WLAN standard operates in the 5GHz frequency band with a channel bandwidth of 20MHz and a variable data rate between 6 – 54*Mbit/sec* . In any wireless application, power consumption of the device is as important as its performance. A typical transceiver chip for the 802.11a standard consumed about 800*mW* of power when operating in full speed and of that 800*mW* of power consumption, nearly 25% is taken by the ADCs [9]. Clearly, more power efficient ADCs with adequate performance should be used in order to extend the battery life of the device. For the IEEE 802.11a standard, the ADCs usually require 8-10 bits of resolution while running at 40MHz for Nyquist rate ADC and even higher sampling rate for oversampled ADC. The number bits depends on the overall system architecture. If digitization is done before the in-phase (I) and quadrate (Q) data separation, the ADC is required to be high speed; otherwise, a slower but higher resolution ADC can be used. figure shows a typical system architecture for the WLAN 802.11a. This transceiver can be used with all the 802.11 standard, claimed in the role of the ADC is to perform digitization of the received data so that the data can be decoded



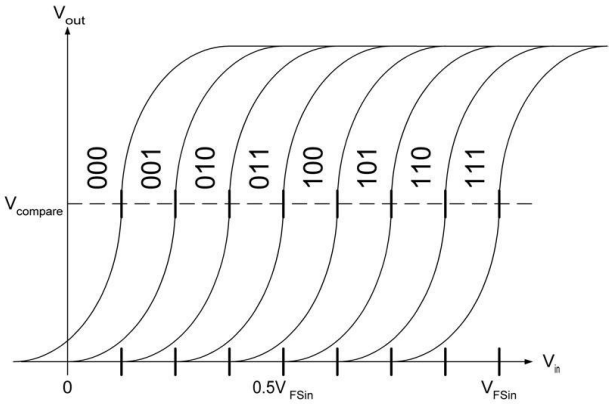
digitally by the baseband processor.

II. INTERPOLATING AND AVERAGING ADC

The interpolating and averaging ADC is based on the architecture of the flash ADC, which is the fastest of all ADC architectures. It tries to overcome the high power consumption disadvantage of the flash ADC by using analog preprocessing like pre-amplifying, interpolating, folding and averaging techniques [4]. As a result, lower input capacitance is seen by the input signal because the

comparators are placed after the analog preprocessing. By making sure that the interpolation network does not load the preamplifiers, power can be saved.

The basic idea of an interpolating and averaging ADC is that the sampled input analog signal will go through a number of pre-amplification stages before the comparison and digitization actually take place.



In between the pre-amplification stages, interpolation will be done to get the required resolution of the digital output. Averaging at the output of the interpolation network with the help of passive elements can improve the accuracy of the digitization.

The above figure illustrates the transfer function of the interpolation ADCs. This example is for a 3-bit resolution but the idea applies equally to higher resolution interpolation ADC. As seen, the input full-scale voltage (VFSin) is divided into 8 equal parts by using differential amplifier type circuit. The sampled input voltage will be compared to all eight transfer functions simultaneously at every intersection points of the dotted line and the transfer functions, i.e. comparing to eight 1-bit flash ADC each with different input-output relationship. The result will be encoded into a 3-bit digital output.

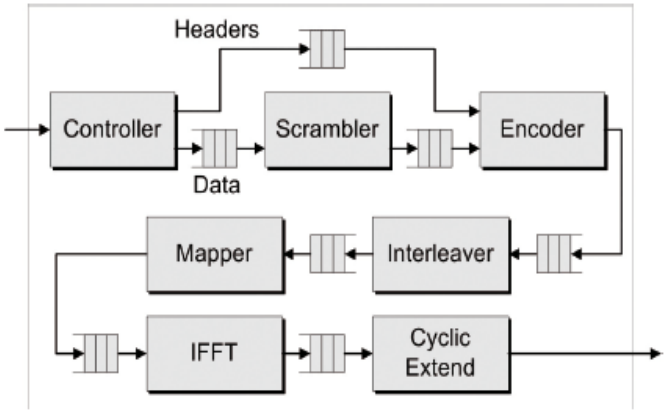
The block diagram and operation of the interpolating and averaging ADC is shown in Figure 3-2. The sampled input analog voltage is fed into two pre-amplifiers and their outputs are interpolated eight times (interpolation factor = 4). The interpolated outputs are averaged with resistors to lower the non-linear characteristics of the interpolation networks.

The averaged and interpolated outputs are compared with the sampled input voltage in regenerative comparators. The eight results will be encoded into a 3-bit digital word for the output.

J. Vandenbussche et. al. makes use of the interpolation and averaging architecture to propose a high-speed and high-accuracy ADC for WLAN application like IEEE 802.11a. It has 8-bit of resolution and capable of running at an input frequency of 30MHz. The resistive ladder on the left sets the reference voltages for the rest of the ADC stages. The rest of the stages are just as described previously. The ADC is fabricated in 0.35μm CMOS process and it consumes about 300mW when operating at full speed of 200MS/s. The interpolating and averaging ADC is able to achieve a SNR ratio of 43dB. The power consumption is relatively high for today's requirement. However, by using technology scaling, i.e. 0.13um process, the power consumption can be significantly deceased without changing of the circuit topology.

III. COMPARISONS

This chip, fabricated in a 0.25/spl mu/m 5M1P CMOS process with 3.7M transistors, implements a fully-compliant IEEE 802.11a PHY modem. The IEEE 802.11a standard provides for wireless local area networks (WLANs) with a physical layer based on coded orthogonal frequency domain multiplexing



(COFDM) modulation, delivering data rates up to 54Mb/s, operating in the 5GHz UNII frequency bands. The article outlines the role of a physical layer (PHY) modem in such a WLAN system. The PHY modem lies between a medium access controller (MAC) and a 5GHz radio transceiver, and is responsible for demodulating and modulating a baseband analog signal with data from the MAC. In 802.11a the baseband signal is a 64 subcarrier COFDM signal with BPSK, QPSK, QAM16 or QAM64 modulated subcarriers.v. From recent researches and technology advancement, interpolation/averaging ADC and pipelined ADC promise to deliver adequate performance according to the IEEE 802.11a WLAN standard with low power consumption.

Pipelined ADC is more suitable for high speed and high resolution requirement. For medium resolution, 8-10 bit and even faster conversion rate, an interpolation/averaging ADC should be used. The power consumption of the two ADCs reported above is not a fair comparison because they fabricated using different processes with different supply voltages. The conclusion drawn here assumes that the same speed and

process are used.

The advantage of digitizing earlier in the system architecture with a faster and higher power ADC is that the received data can be in digital form earlier. Processing the received data in digital form eliminates the linearity problem with analog component. Also, by enlarging the digital

circuit boundary in the system, one can save chip area since digital components have a higher integration. This is a tradeoff between power consumption with the chip area and signal integrity. Usually, interpolation/averaging ADC is used when digitization is done earlier since they have a faster conversion rate. Pipelined architecture is used when digitization is done after the I and Q data separation to save power.

IV. CONCLUSIONS AND FUTURE DIRECTIONS

Recent research shows that by using redundant signed-digit (RSD) cyclic implementation, a variable resolution ADC can be designed . Although this architecture only generates one bit per clock cycle and might not be suitable in today's wideband communication standard, the same idea can be applied in designing pipelined ADC. Circuitry can be designed to sense the channel condition and use the information to control the resolution of digitization. For example, if the channel requires less resolution, a few pipeline stages can be shut down for power conservation.

In conclusion, depending on the system architecture, designer should choose an ADC architecture that will give them the best trade off between power consumption and performance. For digitization before the I and Q data separation, an interpolation/averaging ADC should be used since they give a faster conversion rate. If I and Q data separation is done with SAW devices, a pipelined ADC can be used since they give similar speed and slightly lower power consumption.

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