© 2014 IJIRT | Volume 1 Issue 6 | ISSN : 2349-6002

MULTIPLEXER BASED FULL ADDER

Amit Kumar, Adnan Sherwani, Akash Singh
Student, ECE, DCE, Gurgaon

***Abstract*- Full adder could be a basic building block of the many application specific integrated circuits. The paper evaluates and compares the performance of varied full adder circuits that square measure designed victimization techniques such as XOR, transmission gates, multiplexers etc. conjointly a full adder circuit designed victimization electronic device is planned. The performance of those circuits relies on 180nm method model at provide voltage of two.5V. The TSPICE simulation results show that the planned circuit's performance is healthier as compare to the circuits that square measure found in literature whose performance is evaluated.**

***Index Terms*- XOR, Power, Full Adder, Transmission gate, Multiplexer.**

I. INTRODUCTION

Most of the VLSI applications, like digital-signal process, processing system and microprocessors use arithmetic operations extensively. The arithmetic unit is so, heart of all the point systems. Addition, subtraction, multiplication, and multiply and accumulate (MAC) area unit samples of the foremost usually used operations of the arithmetic circuit. Binary addition is consider this function the foremost crucial half of the arithmetic unit as a result of all different arithmetic operations typically involve addition [1, 2]. It is conjointly a terribly important operation as a result of it involves a carry propagation step. The analysis time of addition depends on the length of the operands.

Thus, the full adder that is the basic building block of all digital VLSI circuits ought to have been undergoes a substantial improvement, being driven by 3 basic style goals, viz. minimizing the transistor count, minimizing the ability consumption and increasing the speed. the expansion of moveable devices like PDAs, cell phones, etc. demand high speed process capabilities that additionally consume less power.The1-bit full adder is that the building block of those operation modules. Thus, enhancing its performance is important for enhancing the overall module performance. In this paper, we have a tendency to reviewed totally different 1-bit full adder cells and additionally gift a 1-bit full-adder cell victimization XOR gate with minimum junction transistor count and multiplex circuit that provides quicker operation, and consumes less power than the alternative planned full-adder cell found in the literature.

The rest of the paper is organized as follows: In section II, some normal implementations of the complete adder circuits are mentioned. In section III, the projected style of 1-bit full adder based mostly on the XOR-multiplexer circuit is conferred. In section IV, simulation results for projected and existing styles full adder circuits are given and comparisons are administrated with graph.

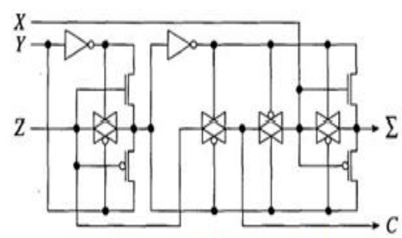

Fig. 1: 16-Transistor full adder circuit

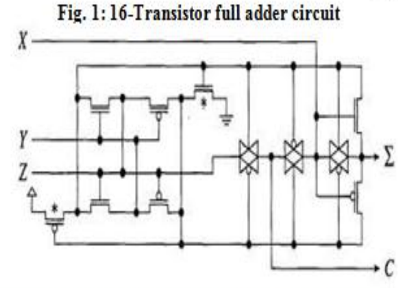

Fig. 2: 14-Transistor full adder circuit

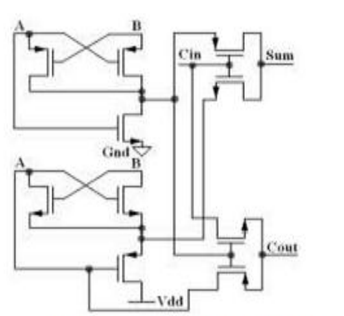

Fig. 3: 10-Transistor full adder circuit

II. PROPOSED FULL ADDER

The general mathematical equations for the "sum" and "carry" are given below in equations (1) and (2).

$$SUM = A \oplus B \oplus Cin \quad (1)$$
$$Cout = (A \oplus B)Cin + AB \quad (2)$$

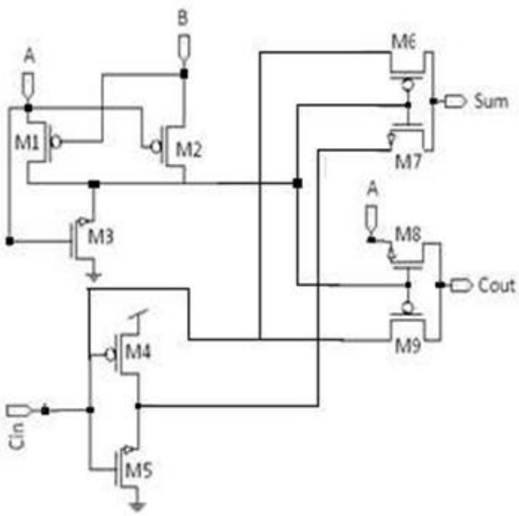

Fig. 4: Proposed full adder circuit

In the proposed circuit the transistor M1, M2 and M3 formed a XOR gate; M6 & M7 and M8 & M9 forms the multiplexers. The feature size of NMOS and PMOS in the XOR gate is used in such a way that it will give the correct output for all logic combinations. The operation of the circuit for different inputs is shown in the table1.

Table 1: The operation of the circuit for different inputs

INPUT			ON/OFF TRANSISTOR									OUTPUT	
A	B	C	M1	M2	M3	M4	M5	M6	M7	M8	M9	SUM	Co
0	0	0	ON	ON	OFF	ON	OFF	ON	OFF	OFF	ON	0	0
0	0	1	ON	ON	OFF	ON	OFF	OFF	ON	OFF	ON	1	0
0	1	0	OFF	ON	OFF	OFF	ON	ON	OFF	ON	OFF	1	0
0	1	1	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	0	1
1	0	0	ON	OFF	ON	OFF	ON	ON	OFF	ON	OFF	1	0
1	0	1	ON	OFF	ON	OFF	ON	OFF	0N	ON	OFF	0	1
1	1	0	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	ON	0	1
1	1	1	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	ON	1	1

III. SIMPULATION RESULTS

All the simulations are done on TSPICE and all the schematics area unit designed on 180nm technology and simulation is completed exploitation power provide of two.5V. The circuit area unit compared in terms of delay, power consumption and power delay product. The below given table two and three severally offers the simulation results of various adder cells given in literature also the projected adder cell.

Table2: Rise, fall time, power and power delay product of SUM

Full Adder	Raising Time*	Falling Time*	Propagation delay*	Power*	PDP&
16T	20.18	30.19	25.18	55.41	1395.22
14T	20.22	29.88	25.05	55.57	1392.02
10T	27.82	19.50	23.66	45.80	1083.62
9T	0.008	0.014	0.011	42.32	.4655
Units- *=ns,&=ns x ns					

Table 3: Rise, fall time, power and power delay product of CARRY

Full Adder	Raising Time*	Falling Time*	Propagation delay*	Power*	PDP
16T	60.35	40.05	50.20	55.21	1664.58
14T	60.15	39.73	49.94	55.57	2775.16
10T	66.52	40.03	53.27	45.80	2439.99
9T	.3116	.3228	.3172	42.32	13.42
Units- *=ns,&=ns x ns					

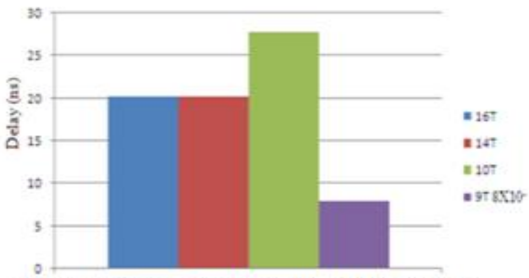

Fig. 5: Comparison of delay Rising Time for Sum

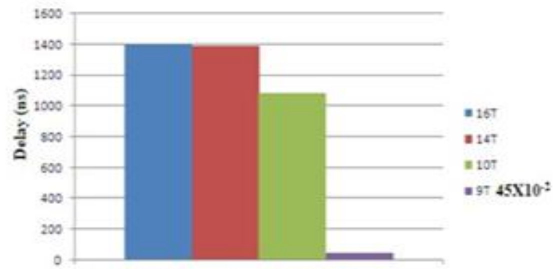

Figure.9. Comparison of PDP for Sum

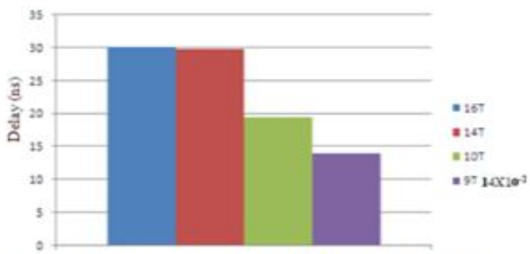

Fig. 6: Comparison of delay Falling Time for Sum

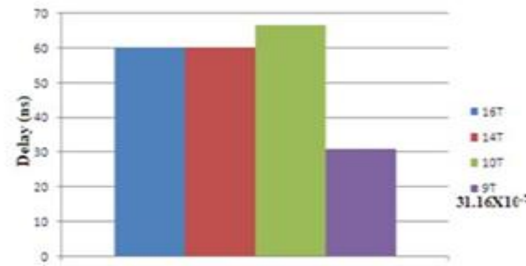

Figure.10. Comparison of delay Rising Time for Carry

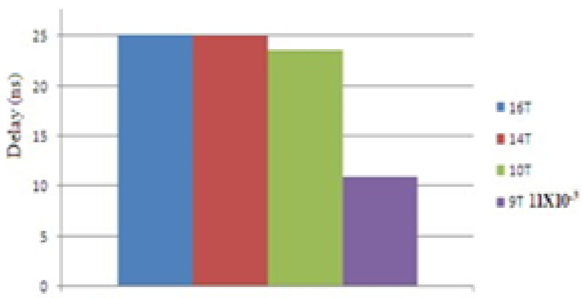

Fig. 7: Comparison of Propagation Delay for Sum

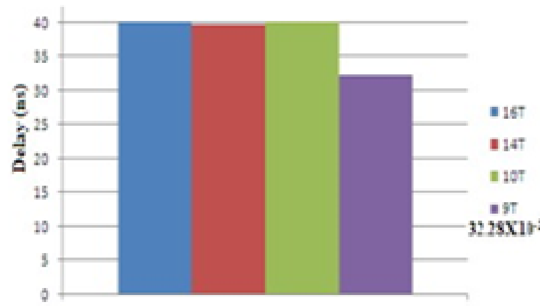

Figure.11. Comparison of delay Falling Time for Carry

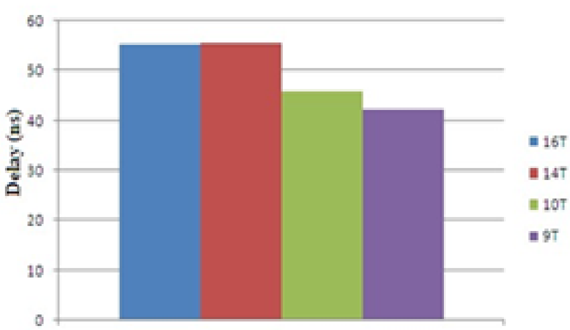

Figure.8. Comparison of Power Consumption for Sum & Carry

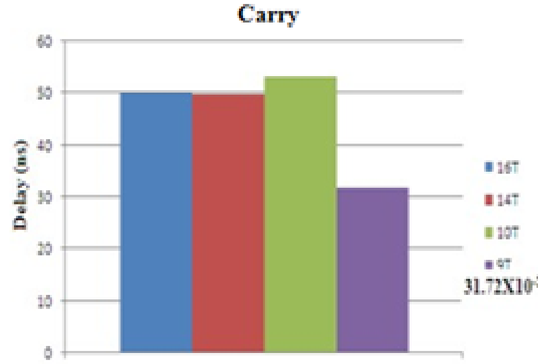

Figure.12. Comparison of Propagation Delay for Carry

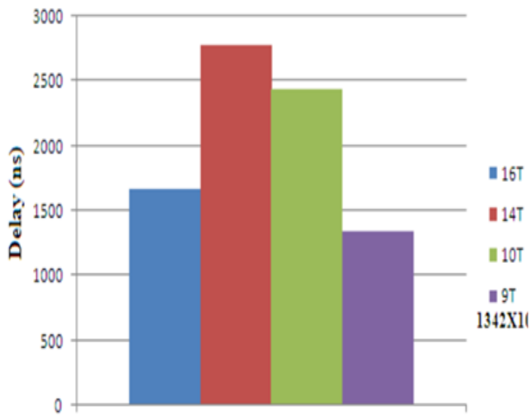

Figure.13. Comparison of PDP for Carry

IV. CONCLUSION

In this paper, performance of 3 adder cells is compared by the projected adder cell that is intended by exploitation XOR and electronic device. The simulation results show that the projected adder is economical in terms of delay, power consumption and power delay product.

REFERENCES

[1] Weste N, Eshragian K; Principles of CMOS VLSI Design-A systems Perspective.

[2] http://en.wikipedia.org/wiki/Fulladder.

[3] www.**slideshare**.net**.**