© 2014 IJIRT | Volume 1 Issue 6 | ISSN : 2349-6002

NEXT GENERATION MULTIPURPOSE MICROPROCESSOR

Shubham Gupta, Vishal Sharma, Parveen Suhag
ECE dept. Dronacharya college of Engg., Gurgaon, India

***Abstract-* The Next Generation Multipurpose Microprocessor (NGMP) is a SPARC V8(E) based multi-core architecture that provides a significant performance increase compared to earlier generations of European space processors. The NGMP is currently in development at Aeroflex Gaisler in Göteborg, Sweden, in an activity initiated by the European Space Agency (ESA). This paper describes the baseline architecture, points out key choices that have been made and emphasises design decisions that are still open. The software tools and operating systems that will be available for the NGMP, together with a general overview of the new LEON4FT microprocessor, are also described.**

I. ARCHITECTURAL OVERVIEW

It should be noted that this paper describes the current state of the NGMP. The specification has been frozen and the activity is currently in its architectural design phase. The development work is scheduled to be finished by the 1st of December 2010.

Fig. 1 depicts an overview of the NGMP architecture. The system will consist of five AHB buses; one 128-bit Processor bus, one 128-bit Memory bus, two 32-bit I/O buses and one 32-bit Debug bus. The Processor bus houses four LEON4FT cores connected to a shared L2 cache. The Memory bus is located between the L2 cache and the main external memory interfaces, DDR2 SDRAM and SDR SDRAM interfaces on shared pins, and it will include a memory scrubber and possibly on-chip memory. As an alternative to a large on-chip memory, part of the L2 cache could be turned into on-chip memory by cache-way disabling.

The two separate I/O buses house all the peripheral cores. All slave interfaces have been placed on one bus (Slave I/O bus), and all master/DMA interfaces have been placed on the other bus (Master I/O bus). The Master I/O bus connects to the Processor bus via an AHB bridge that provides access restriction and address translation (IOMMU) functionality. The two I/O buses include all peripheral units such as timers, interrupt controllers, UARTs, general purpose I/O port, PCI master/target, High-Speed Serial Link, Ethernet MAC, and SpaceWire interfaces.

The fifth bus, a dedicated 32-bit Debug bus, connects a debug support unit (DSU), PCI and AHB trace buffers and several debug communication links. The Debug bus allows for non-intrusive debugging through the DSU and direct access to the complete system, as the Debug bus is not placed behind an AHB bridge with access restriction functionality.

The target frequency NGMP design is 400 MHz, but depends ultimately on the ASIC technology The list below summarizes the specification for the NGMP system:

•128-bit Processor AHB bus
◦4x LEON4FT
▪16 + 16 KB write-through cache with LRU replacement
▪SPARC Reference MMU
▪Physical snooping
▪32-bit MUL/DIV
▪GRFPU with 4-word instruction FIFO shared between pairs of LEON4FT
◦1x256 KB Shared L2 write-back cache with memory access protection (fence registers), BCH ECC and cache-way locking
◦1x 128-bit to 32-bit unidirectional AHB to AHB bridge (from Debug bus to Processor bus)
◦1x 128-bit to 32-bit unidirectional AHB to AHB bridge (from Processor bus to slave I/O bus)
◦1x 32-bit to 128-bit unidirectional AHB to AHB bridge with IOMMU (from master I/O bus to Processor bus)
•128-bit Memory AHB bus
◦1x 64-bit data DDR2-800 memory interface with Reed-Solomon ECC (16 or 32 check bits)
◦1x 64-bit data SDRAM PC133 memory inter-face with Reed-Solomon ECC (16 or 32 check bits)
◦1x Memory scrubber
◦1x On-chip SDRAM (if available on the target technology)
•32-bit Master I/O AHB bus.

II. MAIN MEMORY INTERFACE

The baseline decision for the main memory interface is to support 96-bit (64 data bits and up to 32 check bits) DDR2 and SDR SDRAM on shared pins. However the selection between DDR2 and DDR1 should be regarded as open. The flight models of the NGMP are scheduled 4 to 5 years into the future. At that time there may be additional information available regarding memory device availability. Availability of I/O standards on the target technology may also impact the final decision.

The width of the SDR SDRAM data interface could potentially be made soft configurable between 32 and 64 data bits (plus check bits), allowing for NGMP systems with a reduced width of the memory interface to support packages with low pin count. This is not considered technically feasible for DDR/DDR2.

To further improve resilience against permanent memory errors, a scheme with a spare device column could be envisaged. If a permanent error occurred in one memory device, the spare column would replace the faulty one. This could potentially cause a timing problem since the Reed-Solomon codes are slow to generate, and the multiplexer tree would follow the codec directly. The decision on using column sparing has been deferred until the final technology and package has been selected.

The target is to use DDR2-800 and SDRAM PC100 memories. The SDR SDRAM interface will be able to run at the same or one fourth of the system frequency. The DDR2 interface will be run at the same or twice the system frequency. The clock scaling factor between the memory interfaces and the rest of the chip is selectable via an external signal.

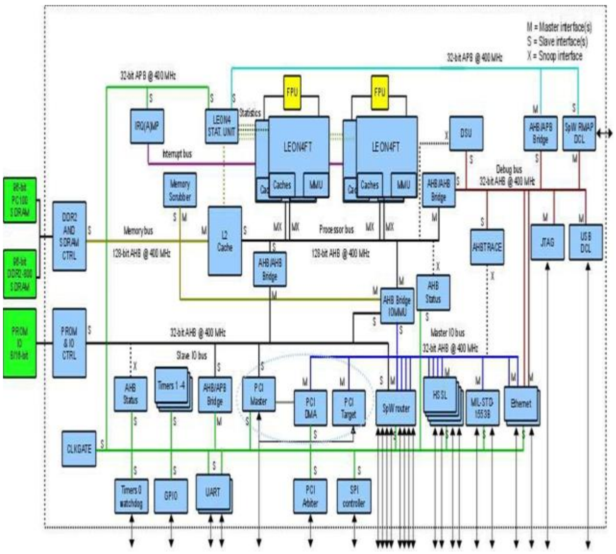
Preliminary calculations that take memory controller latencies into account indicate that the memory interface will have the characteristics listed in tab. 1. The table also includes values for typical DDR-400 memories as this memory type could be a candidate for NGMP. It should be noted that these results are based on memories with characteristics that are deemed to be common for a wide range of SDR/DDR/DDR2 memory devices. The calculations are also based on the behaviour and latencies, with simplifications, of Aeroflex Gaisler memory controllers.

III. I/O INTERFACE

An early design decision was to only include high-speed I/O interfaces on-chip, while legacy low-speed inter-faces can be placed in a companion chip (FPGA/ASIC). The reason for this decision is that low-speed interfaces such as CAN, I2C, 1553, UARTs etcetera do not generate enough data rates to require DMA capabilities, and can easily be implemented off-chip and connected to the NGMP using one of the high-speed interfaces. However, a set of standard peripherals required for operating sys-tem support is included on-chip. These include support for simple memory mapped I/O devices, two basic con-sole UARTs, and one 16-bit I/O port for external interrupts and simple control. The high-speed interfaces that are intended to be used in flight are four SpaceWire links, two 1000/100/10 Mbit Ethernet links, four high-speed serial links, and one 32-bit PCI 2.3 66 MHz master/target interface.

IV. SPACEWIRE LINKS

Considering the wide adoption of SpaceWire links, the NGMP system will implement four SpaceWire link interfaces directly on-chip. The links will be based on the GRSPW2 core from Aeroflex Gaisler's IP Library GRLIB, and include support for the Remote Memory Access Protocol (RMAP). The maximum link bit rate will be at least 200 Mbit/s. The GRSPW2 core will have its redundant link capability enabled, with two link drivers per core for redundancy.



V. DEBUG COMMUNICATION LINKS

The NGMP has a wide range of debug links; JTAG, SpaceWire RMAP, USB and Ethernet. The

controllers for the first three links are located on the Debug bus and will gated off in flight. The controllers for the two Ethernet debug links are embedded in the system's Ethernet cores.
The two Ethernet debug links use Aeroflex Gaisler's Ethernet Debug Communication Link (EDCL) protocol that is integrated in the GRETH_GBIT Ethernet cores. An extension to the GRETH_GBIT core allows users to connect each Ethernet debug link either to the Debug bus or to the Master I/O bus. The Ethernet cores' normal function is preserved even if the debug links are active. The debug traffic is intercepted and converted to DMA at hardware level. The selected buffer size for debug traffic in the NGMP gives a Ethernet debug link band-width of 100 Mbit/s.

VI. IMPROVED SUPPORT FOR PERFORMANCE AND DEBUGGING

The NGMP will include new and improved debug and profiling facilities compared to the LEON2FT and LEON3FT. The selection of available debug links has previously been discussed, additional debug support features of NGMP include:
•AHB bus trace buffer with filtering and counters for statistics
•Processor instruction trace buffers with filtering
•Performance counters capable of taking measurements in each processor core
•Dedicated debug communication links that al-low non-intrusive accesses to the processors' debug support unit
•Hardware break- and watchpoints
•Monitoring of data areas
•Interrupt time-stamping in order to measure interrupt handling latency
•PCI trace buffer
All performance counters and trace buffers are accessible via the Debug bus. The processors can also access the performance counters via the slave I/O bus.The rich set of debugging features gives users the ability to quickly diagnose problems when developing systems that include the NGMP. Some features, such as the PCI trace buffer could easily be replaced by external units or by performing measurements in simulation. However, experience among Aeroflex Gaisler engineers has shown that on-chip debugging resources that are readily available, and supported by a debug monitor, can significantly shorten the time required to diagnose and re-solve a problem.

VII. TARGET TECHNOLOGY

Baseline is the European ST 65 nm space technology. Possible backup options for target technology include UMC 90 nm with the DARE library and Tower (130 nm) with a library from Ramon Chips.
Power consumption of the NGMP ASIC core (without IOs) under worst case operating conditions and maxim-um software load is required to not exceed 6 W. Maxim-um power consumption in idle mode (no software activity, but conservation of status and SEE protection) is required to not exceed 100 mW.

VIII. EXPECTED PERFORMANCE

During the activity's definition phase a prototype system was developed based on existing components from Aeroflex Gaisler's GRLIB IP library. The prototype sys-tem was built on a Xilinx ML510 development board that has a Xilinx XC5VFX130T FPGA. To fit a proto-type system on this FPGA, a reduced configuration of the system described in the NGMP specification was implemented.For validation and performance measurements the SPEC CPU2000 and PARSEC 2.1 benchmark suites have been executed on a Linux Kernel (2.6.21.1) with Debian GNU/Linux 4.0 mounted using NFS over Ether-net.
To achieve a suitable execution time for each bench-mark the SPEC CPU2000 benchmark suite was used with the TRAIN input set and the SIMSMALL (Facessim), SIMMEDIUM (X264), and SIMLARGE (Blackscholes, Ferret, and Fluidanimate) input sets were used for the PARSEC benchmark suite. With these input sets the benchmarks finish their execution within 2 to 40 minutes (depending on benchmark and number of cores). This gives a reasonable long execution time to sample benchmark statistics (MIPS, L2 cache hit-rate, and bus utilization are sampled every 5 seconds).

IX. CONCLUSION

The NGMP will be a SPARC V8(E) based multi-core architecture that provides a significant performance in-crease compared to earlier generations of European space processors, with high-speed interfaces such as SpaceWire and Gigabit Ethernet on-chip. The platform will have improved support for profiling and debugging and will have a rich set of software immediately avail-able due to backward compatibility with existing

SPARC V8 software and LEON3 board support pack-ages. NGMP includes also specific support for AMP configurations and Time-Space Partitioning.

The NGMP is part of the ESA roadmap for standard mi-croprocessor components. It is developed under ESA contract, and it will be commercialised under fair and equal conditions to all users in the ESA member states. The NGMP is also fully developed with manpower loc-ated in Europe, and it only relies on European IP sources. It will therefore not be affected by US export regulations.

REFERENCES

1. www.google.co.in
2. www.wikipedia.com
3. microprocessors text book – G Gupta
4. microprocessor/onbored computer.
5. microprocessors and its interface – U S shah