BiCMOS

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***Abstract*- BiCMOS technology significantly enhances speed performances while incurring a negligible power or area penalty. BiCMOS can therefore provide applications with CMOS power and densities at speed which were previously the exclusive domain of bipolar. This has been demonstrated in applications ranging from static RAMs to gate arrays to microprocessors. Thus the concept of a system on a chip becomes a reality with BiCMOS. The main disadvantage of BiCMOS is greater process complexity, which results in a 1.1-1.3xpackaged chip cost. BiCMOS is currently being demonstrated at 0.5µm. This will extend the conventional 5V TTL (transistor-transistor logic) and ECL (emitter-coupled logic) interfaces to the next level of technology. The BiCMOS challenge has shifted from process and technology to circuits and systems.**

I. INTRODUCTION

BiCMOS is an evolved semiconductor technology that integrates two formerly separate semiconductor technologies - those of the bipolar junction transistor and the CMOS transistor - in a single integrated circuit device.

Bipolar junction transistors offer high speed, high gain, and low output resistance, which are excellent properties for high-frequency analog amplifiers, whereas CMOS technology offers high input resistance and is excellent for constructing simple, low-power logic gates. For as long as the two types of transistors have existed in production, designers of circuits utilizing discrete components have realized the advantages of integrating the two technologies; however, lacking implementation in integrated circuits, the application of this free-form design was restricted to fairly simple circuits. Discrete circuits of hundreds or thousands of transistors quickly expand to occupy hundreds or thousands of square centimeters of circuit board area, and for very high-speed circuits such as those used in modern digital computers, the distance between transistors (and the minimum capacitance of the connections between them) also makes the desired speeds grossly unattainable, so that if these designs cannot be built as integrated circuits, then they simply cannot be built.

In the 1990s, modern integrated circuit fabrication technologies began to make BiCMOS a reality. This technology rapidly found application in amplifiers and analog power management circuits, and has some advantages in digital logic. BiCMOS circuits use the characteristics of each type of transistor most appropriately. Generally this means that high current circuits use metal–oxide–semiconductor field-effect transistor (MOSFETs) for efficient control, and portions of specialized very high performance circuits use bipolar devices. Examples of this include radio frequency (RF) oscillators, bandgap-based references and low-noise circuits.
The Pentium, Pentium Pro, and SuperSPARC microprocessors also used BiCMOS.

HISTORY

- Until recently, integrating bipolar and MOS transistors into a single device proved difficult and uneconomical. For this reason, until now most integrated circuits have used one or the other, according to design criteria of the application. Particularly, bipolar transistors offer high speed, high gain, and low output resistance, whereas CMOS technology offers high input resistance, which translates to simple, low-power logic gates. For years designers of circuits utilizing discrete components have realized the advantages of integrating the two technologies; however, lacking implementation in integrated circuits, application was restricted to fairly simple designs. In the late 1990s, modern IC fabrication technologies began to make BiCMOS a reality. This technology rapidly found application in amplifiers, and appears to have some advantages in digital logic. At this time, the large level of integration allowed by the CMOS circuits is still not possible in BiCMOS technology. This is not a serious concern for amplifiers. It did, however, until a a few years

ago, restrict BiCMOS to small to medium scale integration in digital logic circuits. Nowadays BiCMOS circuits are scalable to VLSI dimensions.

II. THE SIMPLIFIED BiCMOS INVERTER

Two bipolar transistors (T3 and T4), one nMOS and one pMOS transistor (both enhancement-type devices, OFF at Vin=0V)
The MOS switches perform the logic function & bipolar transistors drive output loads

Vin = 0 :
T1 is off. Therefore T3 is non-conducting
T2 ON - supplies current to base of T4
T4 base voltage set to Vdd.
T4 conducts & acts as current source to charge load CL towards Vdd.
Vout rises to Vdd - Vbe (of T4)
Note : Vbe (of T4) is base-emitter voltage of T4.
(pullup bipolar transistor turns off as the output approaches
5V - Vbe (of T4))
Vin = Vdd :
T2 is off. Therefore T4 is non-conducting.
T1 is on and supplies current to the base of T3
T3 conducts & acts as a current sink to discharge load CL towards 0V.
Vout falls to 0V+ VCEsat (of T3)
Note : VCEsat (of T3) is saturation V from T3 collector to emitter
• T3 & T4 present low impedances when turned on into saturation & load CL will be
charged or discharged rapidly
• Output logic levels will be good & will be close to rail voltages since VCEsat is quite
small & VBE » 0.7V. Therefore, inverter has high noise margins
• Inverter has high input impedance, i.e., MOS gate input
• Inverter has low output impedance
• Inverter has high drive capability but occupies a relatively small area
• However, this is not a good arrangement to implement since no discharge path
exists for current from the base of either bipolar transistor when it is being turned
Off, i.e.,
• when Vin=Vdd, T2 is off and no
conducting path to the base of T4 exists
• When Vin=0, T1 is off and
no conducting path to the base of T3 exists
This will slow down the action of the circuit

III. THE CONVENTIONAL BiCMOS INVERTER

Two additional enhancement-type nMOS devices have been added (T5 and T6).
These transistors provide discharge paths for transistor base currents during turn-off.
Without T5, the output low voltage cannot fall below the base to emitter voltage VBE of T3.
Vin = 0 :
T1 is off. Therefore T3 is non-conducting
T2 ON - supplies current to base of T4
T4 base voltage set to Vdd.
T5 is turned on & clamps base of T3 to GND. T3 is turned off.
T4 conducts & acts as current source to charge load CL towards Vdd.
Vout rises to Vdd - Vbe (of T4) · Vin = Vd :
T2 is off
T1 is on and supplies current to the base of T3
T6 is turned on and clamps the base of T4 to GND. T4 is turned off.
T3 conducts & acts as a current sink to discharge load CL towards 0V
Vout falls to 0V+ VCEsat (of T3)

Again, this BiCMOS gate does not swing rail to rail. Hence some finite power is dissipated when driving another CMOS or BiCMOS gate. The leakage component of power dissipation can be reduced by varying the BiCMOS device parameters.

IV. BiCMOS STRUCTURES

Various types of BiCMOS gates have been devised to overcome the shortcomings of the conventional BiCMOS gate
BiCMOS devices are available which provide the full Vdd -> GND voltage swing
There is a common theme underlying all BiCMOS gates:
All have a common basic structure of a MOSFET (p or n) driving a bipolar
transistor (npn or pnp) which drives the output

BiCMOS can provide applications with CMOS power & densities at speeds which were previously the exclusive domain of bipolar. This has been demonstrated in applications ranging from static RAMs to gate arrays to u-processors.

BiCMOS fills the market niche between
• very high speed, but power hungry bipolar ECL (Emitter Coupled Logic)
and
• Very high density, medium speed CMOS.

V. ADVANTAGES OF BiCMOS

- It follows that BiCMOS technology goes some way towards combining the virtues of both CMOS and Bipolar technologies.
- Design uses CMOS gates along with bipolar totem-pole stage where driving of high capacitance loads is required.
- Resulting benefits of BiCMOS technology over solely CMOS or solely bipolar :
- Improved speed over purely-CMOS technology
- Lower power dissipation than purely-bipolar technology (simplifying packaging and board requirements)
- Flexible I/Os (i.e., TTL, CMOS or ECL) –

BiCMOS technology is well suited for I/O intensive applications.

ECL, TTL and CMOS input and output levels can easily be generated with no speed or tracking consequences.

- High performance analogue
- Latchup immunity (Discussed later in course)

VI. DISADVANTAGES OF BiCMOS

- Main disadvantage: greater process complexity compared to CMOS

Results in a 1.25 -> 1.4 times increase in die costs over conventional CMOS.

Taking into account packaging costs, the total manufacturing costs of supplying a BiCMOS chip ranges from 1.1-> 1.3 times that of CMOS.

- However, as CMOS complexity has increased, the percentage difference between CMOS and BiCMOS mask steps has decreased.

Therefore, just as power dissipation constraints motivated the switch from nMOS to CMOS in the late ‘70s, performance requirements motivated a switch from CMOS to BiCMOS in the late ‘80s for VLSI products requiring the highest speed levels.

- Capital costs of investing in continually smaller (<1um) CMOS technology rises exponentially, while the requirement of low power supplies for sub-0.5um CMOS results in degradation of performance.

Since BiCMOS does not have to be scaled as aggressively as CMOS, existing fabs can be utilised resulting in lower capital costs. Extra costs incurred in developing a BiCMOS technology is more than offset by the fact that the enhanced chip performance obtained extends the usefulness of manufacturing equipment & clean rooms by at least one technology generation.

VII. CONCLUSION

- BiCMOS is a manufacturing process for semiconductor devices that combines bipolar and CMOS to give the best balance between available output current and power consumption.
- Polysilicon emitters are universally used in BiCMOS technologies as part of the silicon bipolar transistors or SiGe heterojunction bipolar transistors because improved gain, scalability to deep sub-micron geometries, can be used in self-aligned fabrication schemes that minimize parasitic capacitance and resistance and compatibility with CMOS.
- The simplified BiCMOS Inverter is Two bipolar transistors (T3 and T4), one nMOS and one pMOS transistor (both enhancement-type devices, OFF at Vin=0V).
- The MOS switches perform the logic function & bipolar transistors drive output loads.
- The conventional BiCMOS Inverter is two additional enhancement-type nMOS devices have been added (T5 and T6).
- These transistors provide discharge paths for transistor base currents during turn-off.
- Without T5, the output low voltage cannot fall below the base to emitter voltage VBE of T3.
- BiCMOS can provide applications with CMOS power & densities at speeds which were previously the exclusive domain of bipolar. This has been demonstrated in applications ranging from static RAMs to gate arrays to u-processors.

- In general, BiCMOS devices offer many advantages where high load current sinking and sourcing is required. The high current gain of the NPN transistor greatly improves the output drive capability of a conventional CMOS device.

WEB SITES

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