Design of ring VCO based PLL using 0.25 µm CMOS technology

Ritika Tiwari, Vijay Sharma, Megha Soni
SVCE Indore

***Abstract*— A low power ring VCO based PLL using injection locking is realized by adopting 0.25µm CMOS technology at 2.5V. We have achieved a shift in the bias level by using pMOS active resistive load. The PLL output frequency is 104.4 MHz, at 5 MHz reference frequency by using injection locking based VCO and active resistive load managed to achieve low power dissipation of 4.98mW at 2.5 V.**

***Index Terms*- Phase Locked Loop, Injection Locking, Ring VCO, Shift Bias Level.**

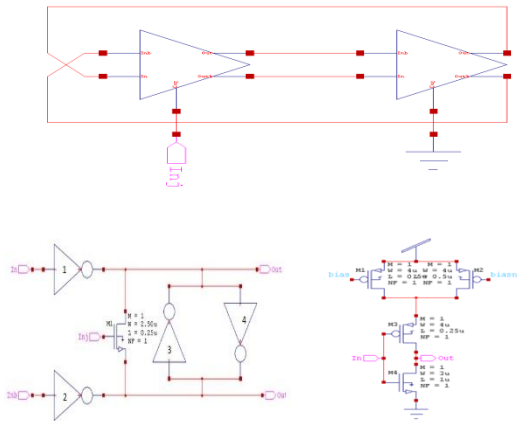
I. INTRODUCTION

PLL is very important building block used in communication, computers and other digital systems. Many digital devices such as Mobile phone, Notebooks operates at very high frequencies for which PLL are used for frequency synthesis, all these devices works on batteries so it becomes very important to design systems which consumes less power. The objective of this dissertation is to design a low power CMOS PLL at 2.5 V using 0.25 μm. In this paper we are designing a VCO using the MOS capacitance and active load resistance which are scalable, consumes less power and occupies less area. Also we are using Injection locking VCO to reduce the phase noise. This paper is organized as follows. Section 2 describes the design of differential injection locked ring VCO and all the necessary building blocks. Section 3 contains the comparison of the work done in this paper. The results are discussed in Section 4 along with the conclusion.

We have used injection locking as there are no stability issues and it also increases the loop bandwidth. The output phase noise tracks injection signal phase noise over wide bandwidth and it is very easy to implement. Injection locking can be used at very high frequencies.

II. DESIGN OF THE DIFFERENTIAL INJECTION-LOCKED RING-VCO

Usually tuning exhibits nonlinearity i.e. K_{VCO} is not constant. Such nonlinearity degrades the settling behavior of PLLs and leads to high sensitivity for some frequency region. To avoid this we need to minimize the variation of K_{VCO} across the whole tuning range. The linearity of the frequency tuning of a VCO is easily seen from its functional dependence of K_{VCO} on the control voltage. The closed loop transfer function of a PLL, H(s) is proportional to $K_{VCO.}$ The loop bandwidth is given as:



$$\omega_n = \sqrt{\frac{K_{VCO} I_P}{2\pi N C_f}}$$

where Ip is the charge pump current, N is the division ratio of the feedback loop, and C_f is the filter capacitance. So we can see that the loop bandwidth can be changed by varying the K_{VCO} [11]

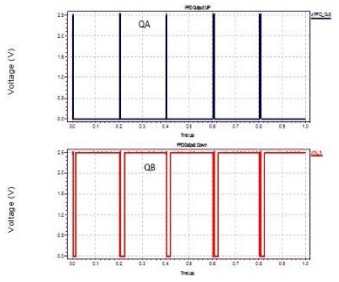


Fig. 1.Proposed differential delay cell[1]

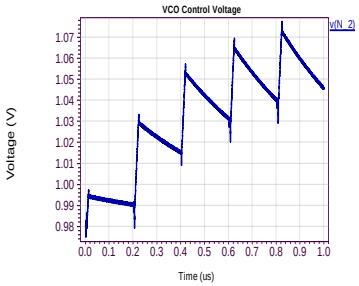


Fig. 2. Schematic and transfer characteristics of bias level shifter [1]

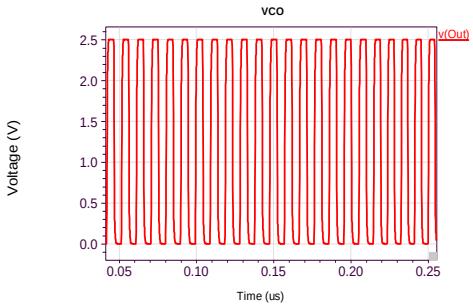


Fig. 3.Two stage differential ring VCO with injection locking [1]

Control voltage for VCO is generated by charge pump which passes through the RC filter the transient response of control voltage to VCO is shown above. This response shows that VCO control voltage varies linearly with time.

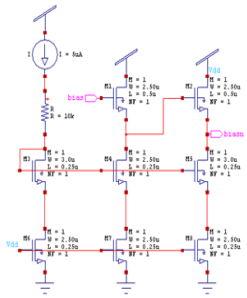


Fig. 4.Transient response of voltage control voltage for VCO

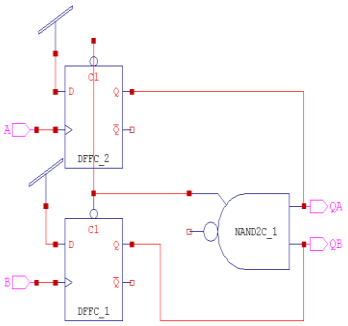


Fig.5.Transient response of VCO with T = 9.63 ns and f=104.4 MHz

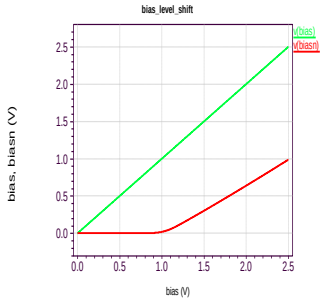


Fig. 6.Schematic of PFD

PFD compares the phase of two input signals one is the clock frequency or reference signal and other is the feedback signal from VCO to frequency divider and to PFD. PFD output is fed to the charge pump circuit. It has two inputs A and B which is applied to the clock terminal of the D flip flop.

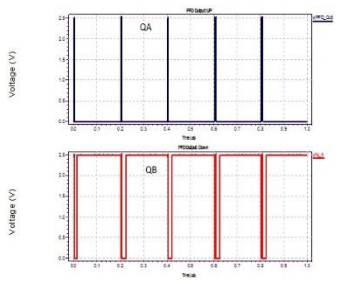


Fig. 7.Transient response of PFD

Charge pump circuits are capable of high efficiencies, (90–95%) while being electrically simple circuits.

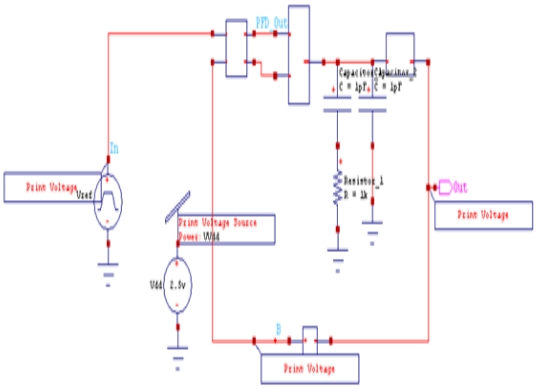


Fig. 8.Schematic of CMOS charge pump based on the current mirror technique

A divide by two circuit commonly called DTC is widely used to produce quadrature outputs.

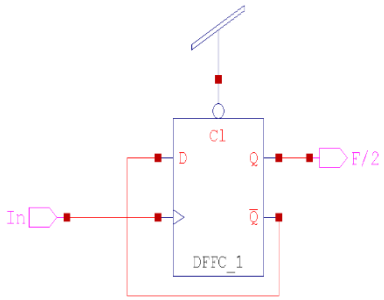


Fig. 9.Schematic of frequency divider

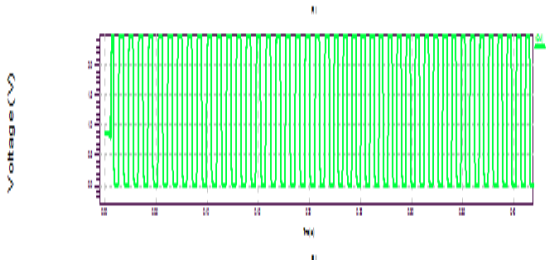


Fig. 10.Transient response of frequency divider

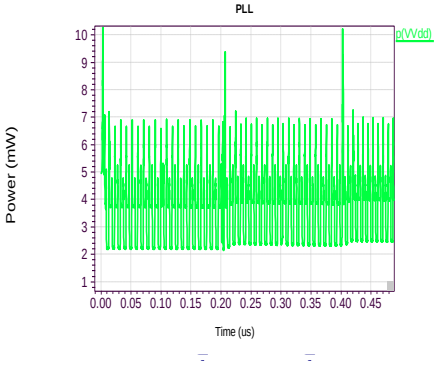


Fig. 11.Simulation setup of PLL with reference frequency of 5 MHz [1]

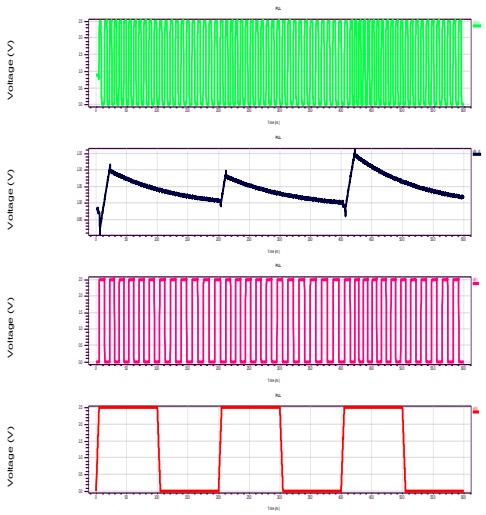


Fig.12. (a) Output response of PLL 104.4 MHz (b) Control voltage for VCO (c) Output response of

frequency divider (d) Reference input signal of 5 MHz

The transient response of the PLL is shown in the figure 6.4 which involves reference signal, VCO output frequency, VCO control voltage, and f/2 output signal which is fed to the PFD.

Fig. 13.Magnified transient response of PLL tested at 4 MHz input reference frequency

In this test setup PLL consumes 4.98 mW at 2.5 V power supply. Its transient power consumption curve is shown below

Fig. 13.Transient power consumption cure of PLL (4.98 mW) at 2.5 V power supply

III. PERFORMANCE SUMMARY OF PLL

TABLE 1
Performance summary of PLL

Technology	0.25 µm CMOS process
Supply Voltage	2.5 V
PLL output frequency	104.4 MHz at 5 MHz reference input frequency
Power dissipation	4.98 mW

IV. CONCLUSION

The design proposed in this dissertation is tested at 5 MHz reference signal but this design can support wide range of reference signal. The purpose of this dissertation is to demonstrate the design at 2.5 V at 0.25 µm CMOS technology. There are various electronic communication systems which operate at such voltage level. This PLL can be used at the radio receiver and super heterodyne demodulators. Design consumes *4.98 mW* at 2.5 V power supply which makes it suitable to use it in battery operated systems. This design can be implemented at different CMOS technology such as 0.18 µm CMOS technology. Since this design is fully differential, which makes it noise immune.

TABLE 2
PERFORMANCE SUMMARY AND COMPARISON OF PLLs

	Tuning range	**Phase noise**	**Power (mW)**	**CMOS (in nm)**
This work	5 MHz		4.98	250
[1]	1.44 GHz	-108 dBc/Hz	39	180
[2]	23.8-30.2 GHz	-110 dBc/Hz	31	32
[3]	30%	-124.2 at 23.1 GHz	27.2	32
[4]	3.5 GHz-7.1 GHz	-105 dBc/Hz		90
[5]			4.3 at 855 MHz	65
[6]	22.9 %	-127.3at 10 MHz from 24.7 GHz	64	32
[7]		-60.5 at 100 KHz	1.5	90
[8]	2.17-2.48 GHz	-112.77 at 1 MHz offset	14.4	180
[9]	22.9 %	-97.5@ 1MHz	16	65
[10]	6.35 %	-91.46 @1MHz offset	7.5	180

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