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TO DESIGN HIGH SPEED AND LOW POWER ALU USING VEDIC MATHEMATICS

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***Abstract*- Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculation based on formula (sutras). It deals with various branches of mathematics like arithmetic, algebra, geometry *etc*. The speed of arithmetic calculation is of extreme importance and depends greatly on the speed of multiplier. Urdhva Tiryagbhyam Vedic method for multiplication, strikes a difference of actual process of multiplication, by enabling parallel generation of intermediate product, eliminating unwanted multiplication steps with zeros and scaled to higher bit level. This formula (Sutras) is used to build high speed power efficient multiplier in coprocessor. This project is to design arithmetic module using the technique of ancient Indian Vedic Mathematics to improve the performance of coprocessor. This project is to design NxN arithmetic modules, where A & B are the two N bits inputs of these module and different sections of module are multiplier which is designed by using Vedic algorithm of multiplication named Urdhva Tiryagbhyam multiplier and with carry save adder, adder/ subtractor and MAC unit.**

***Index Terms*- DSP, Arithmetic Logical Unit, Adder, Multiplication, Vedic Urdhva Tiryagbhyam multiplication algorithm, Vedic Multiplier (VM).**

I. INTRODUCTION

Mathematics is mother of all sciences. It is full of magic and mysteries. The ancient Indians were able to understand these mysteries and develop simple keys to solve these mysteries. Thousands of, years ago the Indians used these techniques in different fields like construction of temples, astrology, medical, science *etc.*, due to which INDIA emerged as the richest country in the world. The Indians called this system of, calculations as "THE VEDIC MATHEMATICS". Vedic Mathematics is much simpler and easy to understand, than conventional mathematics.

The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge; it deals with various branches of mathematics like arithmetic, algebra, geometry *etc*. Vedic Mathematics introduces the wonderful applications to Arithmetical computations, theory of numbers, compound multiplications, algebraic operations, factorizations, simple quadratic and higher order equations, simultaneous quadratic equations, partial fractions, calculus, squaring, cubing, square root, cube root, coordinate geometry and wonderful Vedic Numerical code. The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a, subject of interest over decades. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Employing this technique in the computation algorithms will reduce the complexity, execution time, power.

II. PURPOSE OF THIS PROJECT

We know that the ALU is a mathematical unit. The mathematical unit performs arithmetic (addition, subtraction, multiplication) and logical operations (AND, OR, INVERTER).

That is why the ALU is called heart of microprocessor, microcontroller and digital signal processor. Our proposed 4-bit Vedic ALU performs arithmetic operations and performs logical operations. It performs three arithmetic operations and five logical operations. Nowadays high speed processor requirements are gradually increasing. Recent day processor having more than two ALU (quad core, Core2 duo) to improve the processor speed. So if we improve performance of the internal architecture of the ALU speed mainly depends on the speed of multiplier. Thus we have designed the high speed 4-bit Vedic multiplier using Vedic Mathematics and replaced the existing multiplier unit in ALU. Our Vedic multiplier is very fast and occupies less hardware. The switching activity of the multiplier also reduced leads to reduction of dynamic power consumption. The dynamic power is dominant (around 90 % of total power) in VLSI architecture design. The proposed ALU is implemented on FPGA hardware. The ALU diagram is given in *Fig* 2.1. The input is given to the ALU by using toggle switch on FPGA board and the data can be processed.

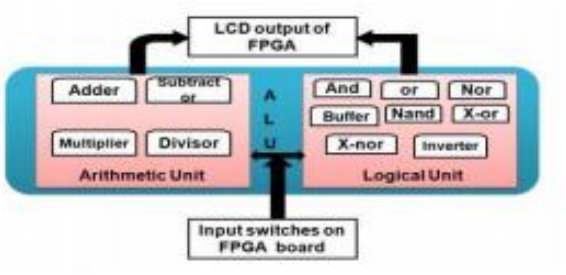

Fig 2.1 ALU block

III. COMPARISION BETWEEN BOOTH AND URDHVA TRIYAGBHYAM

Multiplication is an important fundamental function in an ALU. Since, multiplication dominates the execution time of most DSP algorithms; therefore high speed multiplier is much desired. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip. With an ever-increasing quest for greater computing power on battery operated mobile devices, design emphasis has shifted from optimizing conventional delay, time, area and size to minimizing power dissipation while still maintaining the high performance. The low power and high speed VLSI can be implemented with different logic styles. The three important considerations for VLSI design are power, area and delay. There are many proposed logics for, low power dissipation and high speed and each logic style has its own advantages in terms of speed and power. The objective of good multiplier is to provide a physically compact high speed and low power consumption unit. We applied Urdhva Tiryagbhyam sutra to binary multiplier using carry save adders. Thus Vedic multiplier using Urdhva Tiryagbhyam sutra has less delay and thus they are treated as high speed multipliers as compared to Booth's algorithm using recorded multipliers.

IV. HARDWARE USED

FPGA – Field Programmable Gate Array

A Field-programmable Gate Array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable". The FPGA configuration is generally specified using a hardware description language (HDL).

The Field Programmable Gate Arrays (FPGAs) devices, with their reconfigurable logic, practicality, portability, low consumption of energy, high operation speedy and large data-storage capacity, are a great choice for embedded systems project development and prototype.

FPGA – Architecture

FPGAs contain programmable logic components called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like many (changeable) logic gates that can be inter-wired in (many) different configurations. Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be simple flip-flops or more complete blocks of memory.

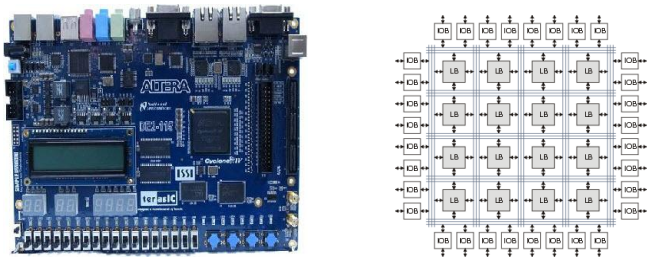

Fig 3.1 FPGA & Logical blocks of FPGA

V. TOOLS USED

A. Aldec Active HDL

Active-HDL is a Windows based, integrated FPGA Design Creation and Simulation solution for team-based environments.

The Integrated Design Environment (IDE) within Active-HDL includes a full HDL and graphical design tool suite and RTL/gate-level mixed language simulator for rapid deployment and verification of FPGA designs.

B. Quartus 2

The Altera Quartus II design software provides a complete, multiplatform design environment that easily adapts to your specific design needs. It is a comprehensive environment for system-on-a-programmable-chip (SOPC) design.

The Quartus II software includes a modular Compiler. The Compiler includes the following modules:

- Analysis & Synthesis
- Partition Merge Fitter
- Assembler
- Time Quest Timing Analyzer
- Design Assistant
- EDA Net list Writer
- Hardcopy Net list Writer

To run all Compiler modules as part of a full compilation, on the Processing menu, click Start Compilation. You can also run each module individually by pointing to start on the Processing menu, and then clicking the command for the module you want to start.

C. Simulation

- **Functional simulation**

Functional simulation is used to check the correctness of algorithm or design. It won't provide the propagation delay.
It is performed using Modelsim-Altera and Qsim(Quartus Simulator).

- **Timing simulation**

Timing simulation is used to provide propagation delay.
It also checks the correctness of an algorithm or design.
It is also performed using Modelsim-Altera and Qsim(Quartus Simulator).

D. Dsch3 and Microwind

- **Dsch3**

DSCH3 is the companion software for logic design. Based on primitives, a hierarchical circuit is built and simulated. Interactive symbols are used to friendly simulation, which includes delay and power consumption evaluation

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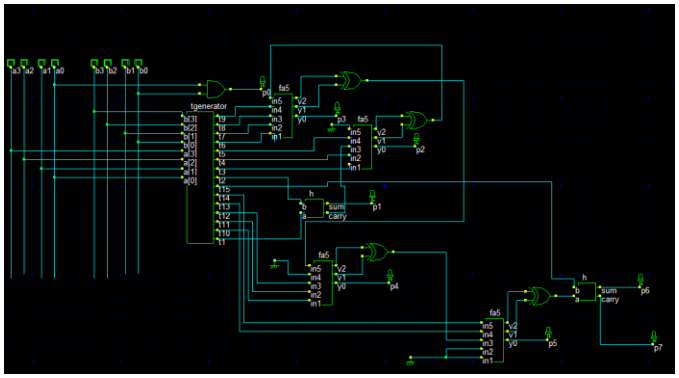


Fig 5.1 Block diagram of vedic calculator

- **Microwind**

The Microwind software allows the designer to simulate and design an integrated circuit at physical description level. Microwind3 unifies schematic entry, pattern based simulator, SPICE extraction of schematic, Verilog extractor, layout compilation.

Using Dsch3 the circuit of Vedic calculator was created and then converted to Verilog code understood by Microwind and then run command was used in Microwind to form the layout of Vedic calculator as shown in *Fig* 5.2. After that the power dissipated can be calculated which is shown Result section of this project.

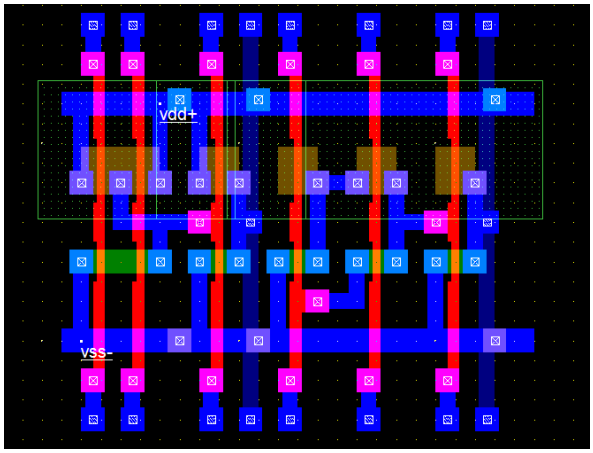


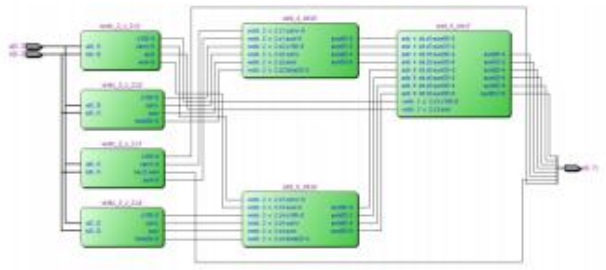
Fig 5.2 Layout of Vedic calculator

VI. RESULTS

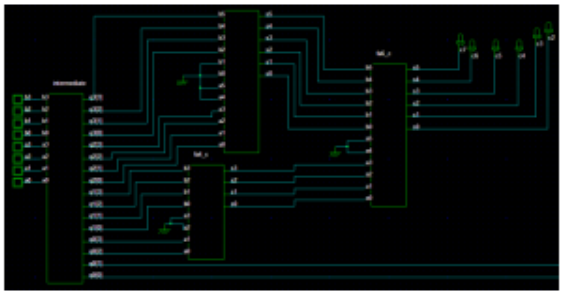
- **Timing analysis**

ALGORITHM	TIMING ANALYSIS	POWER ANALYSIS
Urdhva Tiryagbhyam	7.557 ns	156.73mW
Booth Algorithm	13.936 ns	308.88 mW

- **RTL Post Map View**



- **Digital Circuit of Vedic calculator**



(The circuit blocks are combined and implemented in DSCH Software and respective blocks are created for easy integration in DSCH software. The intermediate block contains four 4*4 Vedic calculator circuit, fa4_c is 4 bit full adder circuit and fa6_c is 6bit full adder circuit).

VII. ACKNOWLEDGMENT

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