Design and analysis of Ring VCO in 32nm CMOS technology and Comparison with LC-VCO in 70 nm CMOS technology on Variation in Power Consumption and Frequency

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***Abstract*- The proposed work depicts the execution assessment of various sorts of ring oscillator Voltage Controlled Oscillator topologies on the premise of two trademark parameters force and recurrence in 32 nm CMOS innovation. The different topologies broke down incorporates Current Starved VCO, VCO with Gates of PMOS Transistor Grounded, VCO with PMOS Diode Connected, VCO with NMOS Diode Connected, VCO with voltage connected to both PMOS and NMOS Transistor. Recreation of various parameters of ring oscillator VCO is done on Tanner apparatus Version 14. VCO topologies are assessed on the premise of recurrence and force utilization by taking lower supply voltage of 1.2 V. Execution assessment and examination of various topologies results in least power utilization of 0.005 nW by VCO with NMOS transistors diode associated topology and most extreme working recurrence of 2 GHz by VCO with Current Starved VCO and correlation with LC-VCO in 70nm CMOS Technology.**

***Index Terms*- Current Starved VCO, VCO with Gates of PMOS Transistors Grounded, VCO with PMOS Transistors Diode Connected, VCO with NMOS Transistors Diode Connected, VCO with Voltage Applied to both PMOS and NMOS Transistors, Single Switch LC-VCO, Double Switch LC-VCO and Single Switch with current source LC-VCO.**

I. INTRODUCTION

An oscillator that can be turned over an extensive variety of frequencies by applying a voltage (tuning voltage) to it, or as such, an oscillator that progression its recurrence as per a control voltage food to its control info is Voltage Controlled Oscillator [1]. As appeared in Fig. 1, the recurrence of swaying is shifted by the connected controlled voltage, while adjusting signs may likewise be bolstered into the VCO to bring about recurrence regulation (FM) or stage tweak (PM)[2][24]; a VCO with computerized heartbeat yield may comparatively have its redundancy rate (FSK, PSK) or beat width balance (PWM). The oscillator first change over voltage sign to current, and after that current is changed over into recurrence [1]. This has various applications going from recurrence synthesizers to handsets. The outline of superior solid VCO has been one of the dynamic range of innovative work in late years [22]. A CMOS VCO can be constructed utilizing ring topology;

unwinding circuits or LC tuned circuit [2]. The condition (1) demonstrates the essential meaning of VCO as indicated by its operation framing a trademark between information voltage and recurrence.

$$W_{out} = W_o + K_{vco} * V_{control} \quad (1)$$

Here, Wo speaks to the capture comparing to Vcontrol = 0 and Kvco indicates the "addition" and "affectability" of the circuit [2].

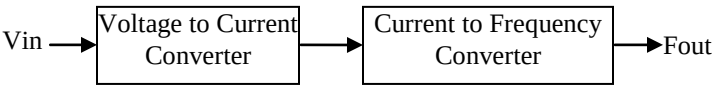

Fig.1. Definition of VCO

Here, Wo speaks to the capture relating to Vcontrol = 0 and Kvco means the "addition" and "affectability" of the circuit [2].

There are fundamentally two sorts of Harmonic oscillators, LC and Ring Oscillator. The fundamental point of interest of Ring oscillator over LC oscillator is that the ring oscillator can be effectively created in CMOS innovation when contrasted with LC oscillator, since the manufacture of inductor need tremendous measure of space [5][24].

Improvement of new plan strategy for advancement of force with low voltage:

The general wellspring of dissemination in any CMOS circuit is the current drawn while exchanging. Since knowing the number and capacitance the voltage change on a door capacitance requires charge exchange and consequently causes power utilization. When this door capacitance is charged, the entryway can keep up the DC voltage level with no extra charge development and does not expend any present. The

obliged charge to change voltage levels on the door is portrayed by the accompanying condition [18][24].

Qgate = Cgate Vdd (2)

Qgate is the charge required to change state, Cgate is the door capacitance, Vdd is the force supply voltage. Exchanging creates a present relative to working recurrence (F) of the VCO. Since current is characterized as far as coulombs every second (amperes), the current can be ascertained as appeared in condition (4) [19].

I = Qgate × Frequency = (Cgate×Vdd) × F (3)

Where I is the current in amperes (coulombs every second)

The aggregate current can be summed up into a figure which will incorporate all the hub capacitances in the gadget.

Idevice = Ctotal × Vdd × Fosc (4)

where

Idevice is the aggregate gadget current, Ctotal is the aggregate hub capacitance of all inner exchanging hubs, Fosc is the exchanging recurrence of the circuit. of the greater part of the interior exchanging hubs is an unmanageable errand, the current under various conditions can be resolved exactly by measuring the present level for a specific known recurrence and supply voltage conditions, and after that scaling the present worth to decide the conduct under various conditions [23]. The reliance of these streams is straightforwardly on the framework operation and the supply levels.

The VCO power scattering is capacity of its recurrence henceforth ought to be displayed with consideration.

Normal Power Dissipation = Fosc.N.C.Vdd (5)

Here Fosc is the oscillaton recurrence, C is the gadget capacitance and N might be the quantity of stages if there should be an occurrence of a ring oscillator.

Expecting the inverters are indistinguishable, the swaying recurrence is given in condition beneath,

fosc =1/(n* (tphl + tplh)) (6)

Where n is the quantity of inverters in the ring oscillator and (tphl + tplh) is the engendering delay time of every inverter. The engendering delay times tphl and tplh decide the contribution to-yield signal deferral amid the high-to-low and low-to-high moves of the yield, individually Ring oscillator is planned by utilizing five CMOS inverters having

(W/L)p = 12/2 and (W/L)n = 5/2. (7)

These particulars are picked in the connection

(W/L)p = 2.5 (W/L)n (8)

by applying condition for symmetric inverter i.e. Kn=Kp. By taking these estimations of W/L, if the DC attributes of CMOS inverter are watched exchanging point is found to more like 2.5(Vdd/2=5/2).

The execution assessment and correlation on the premise of two basic parameters, power utilization and recurrence, of taking after topologies of ring sort VCOs are talked about in the proposed work [24].

- Current Starved VCO
- VCO with entryways of PMOS transistors grounded
- VCO with PMOS transistors diode associated
- VCO with source voltage connected to both PMOS and NMOS transistors
- VCO with NMOS transistors diode associated

In the further areas, proposed circuit schematic of the specific topology of ring oscillator, the related reproduction results and after that the plain representation of the info parameters control voltage and time, over which the parameters under thought, power scattering and recurrence are ascertained, and the separate voltage verses recurrence diagrams are drawn, which are talked about independently finally.

II. VCO WITH GATES OF PMOS TRANSISTORS GROUNDED

Fig. 2 depicts the proposed VCO with gates of PMOS transistors grounded. It consists of five stage ring oscillator. This ring oscillator made by odd number of inverters which forms a closed loop with positive feedback. In this type of VCO, PMOS transistor is always ON since the gate terminal of PMOS transistor is connected to ground and PMOS transistor gives strong 1, so it behaves as a resistor.

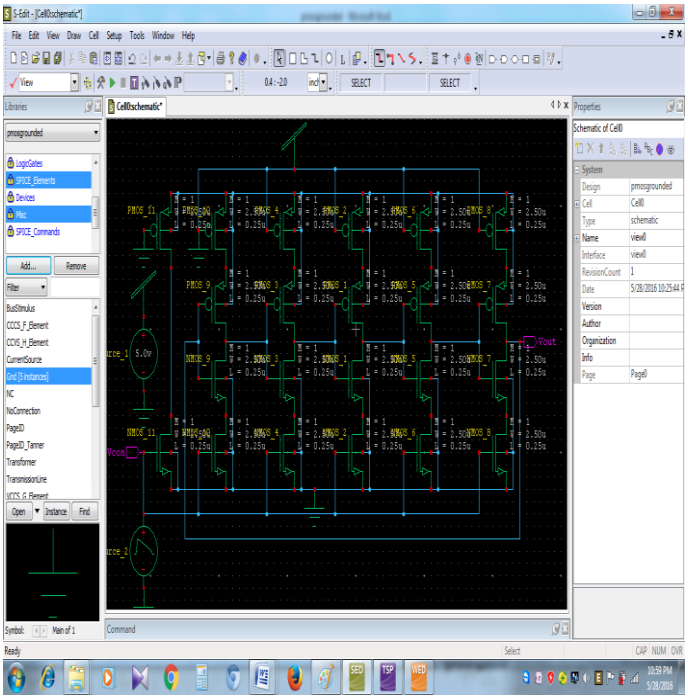

Fig. 2 Schematic Circuit of proposed VCO with gates of PMOS Transistors Grounded

SIMULATION RESULTS

The VCO with doors if PMOS transistors grounded performed after the transient investigation of PMOS transistor grounded with heartbeat information voltage, reenacted utilizing Tanner EDA ver. 14 test systems is as appeared in the accompanying fig. 3. The VCO with entryways of PMOS transistors grounded circuit animated utilizing Tanner EDA T-flavor test system.

The VCO with doors of PMOS transistors grounded draws most extreme 0.44 GHz recurrence from supply voltage of 0.4 V.

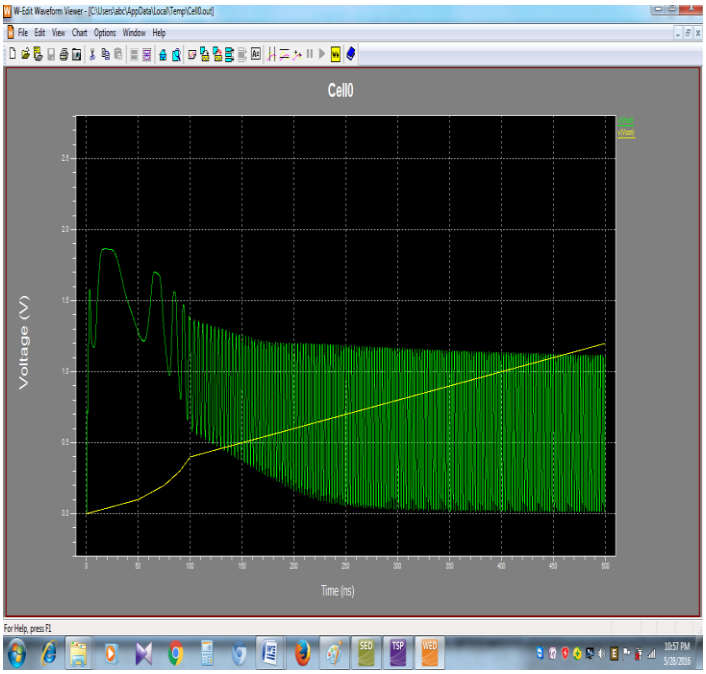

Fig. 3 Simulated results of proposed VCO with Gates of PMOS Transistor Grounded

The summary of simulated result waveform is shown in table below:

S. No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Power (nW)
1.	0.1	0	0	0
2.	0.2	0	0	0
3.	0.3	9	0.11	0.021
4.	0.4	4.6	0.2	0.038
5.	0.5	3	0.33	0.063
6.	0.6	4.8	0.38	0.072
7.	0.7	3.8	0.4	0.076
8.	0.8	3.4	0.42	0.080
9.	0.9	3.2	0.44	0.084
10.	1.0	3.0	0.44	0.084
11.	1.1	2.8	0.44	0.084
12.	1.2	2.8	0.44	0.084

Table 1 Frequency & Dynamic Power Dissipation of VCO with Gates of PMOS Transistor Grounded

A graph is plotted between voltage and frequency, which is shown in the Fig. 4, in order to observe the relation between these two quantities.

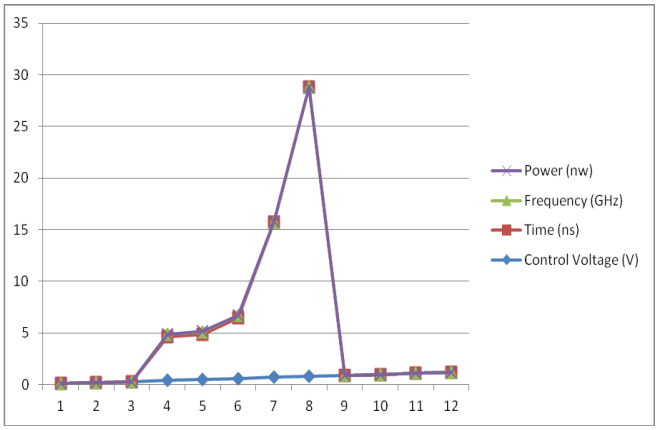

Fig. 4Voltage vs. Frequency Plot of VCO with gates of PMOS transistors grounded

III. VCO WITH VOLTAGE APPLIED TO BOTH PMOS AND NMOS TRANSISTORS

Fig. 5 depicts the VCO with voltage applied to both PMOS and NMOS transistors. It consists of five stage ring oscillator. This ring oscillator is designed by back to back connection of odd number of inverters which forms a closed loop with positive feedback as per the requisite Barkhausan's criteria. In this VCO, the two transistors M5 and M6 are eliminated and the source voltage is applied to the gates of both lower NMOS transistors and upper PMOS transistors.VCO circuit is simulated using Tanner EDA T-spice simulator ver 14.

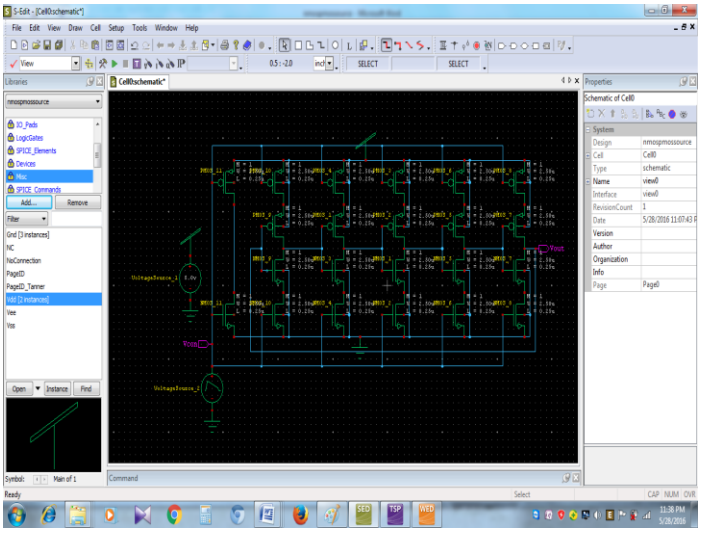

Fig. 5 Schematic Circuit of proposed VCO with voltage applied to both PMOS and NMOS transistors

SIMULATION RESULTS

Fig. 6 demonstrates the reenacted waveform of proposed VCO performed after the transient investigation of voltage connected to both PMOS and NMOS transistors with heartbeat info voltage. The VCO with source voltage connected to both PMOS and NMOS transistors circuit animated utilizing Tanner EDA T-Spice test system.

The VCO with source voltage connected to both PMOS and NMOS transistors draws most extreme 0.19 GHz recurrence from supply voltage of 0.7 V.

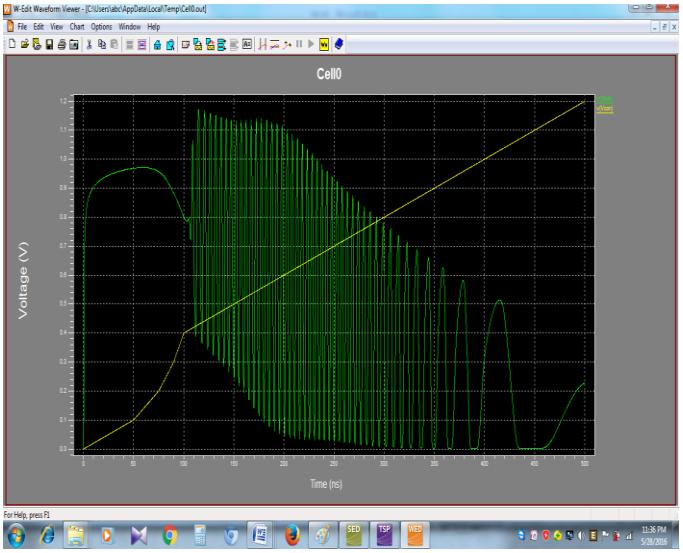

Fig. 6 Simulated results of proposed voltage applied to both PMOS and NMOS transistor VCO pulse input voltage

S. No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Power (nW)
1.	0.1	0	0	0
2.	0.2	0	0	0
3.	0.3	0	0	0
4.	0.4	6	0.16	0.030
5.	0.5	5	0.2	0.038
6.	0.6	5	0.2	0.036
7.	0.7	5.2	0.19	0.036
8.	0.8	6.8	0.14	0.030
9.	0.9	14.6	0.06	0.030
10.	1.0	0	0	0
11.	1.1	0	0	0
12.	1.2	0	0	0

Table 2 Frequency & Dynamic Power Dissipation of voltage applied to both PMOS and NMOS transistor VCO

A graph is plotted between voltage and frequency, which is shown in the Fig. 7, in order to observe the relation between these two quantities.

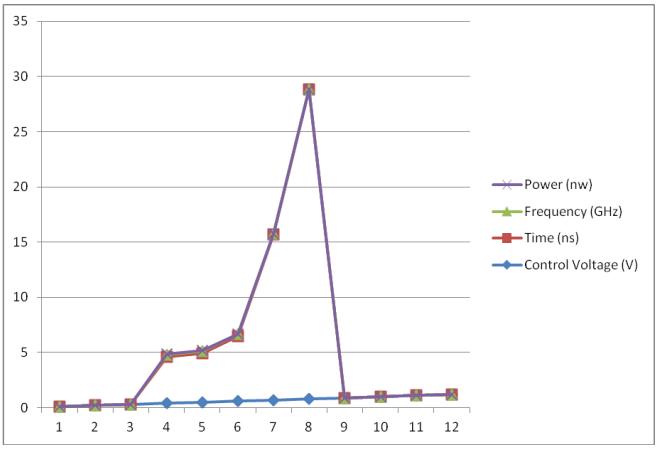

Fig.7 Voltage vs. Frequency Plot of VCO with voltage applied to both PMOS and NMOS transistors

IV. CURRENT STARVED VCO

Fig. 6 demonstrates the reenacted waveform of proposed VCO performed after the transient investigation of voltage connected to both PMOS and NMOS transistors with heartbeat info voltage. The VCO with source voltage connected to both PMOS and NMOS transistors circuit animated utilizing Tanner EDA T-Spice test system.

The VCO with source voltage connected to both PMOS and NMOS transistors draws most extreme 0.19 GHz recurrence from supply voltage of 0.7 V.

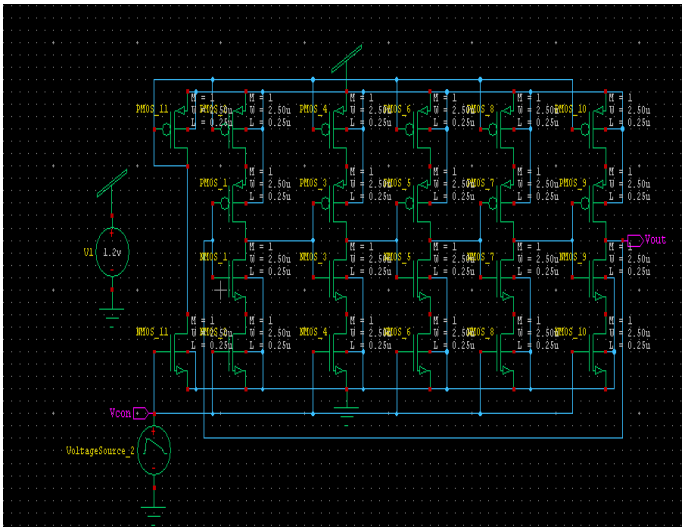

Fig. 8 Schematic Circuit of proposed Current Starved VCO

SIMULATION RESULTS:

In this paper, the current starved VCO circuit empowered utilizing Tanner EDA T-zest test system. The Current Starved VCO circuit fortified utilizing Tanner EDA T-zest test system. The Current Starved VCO draws most extreme 2 GHz recurrence from supply voltage of 0.6 V.

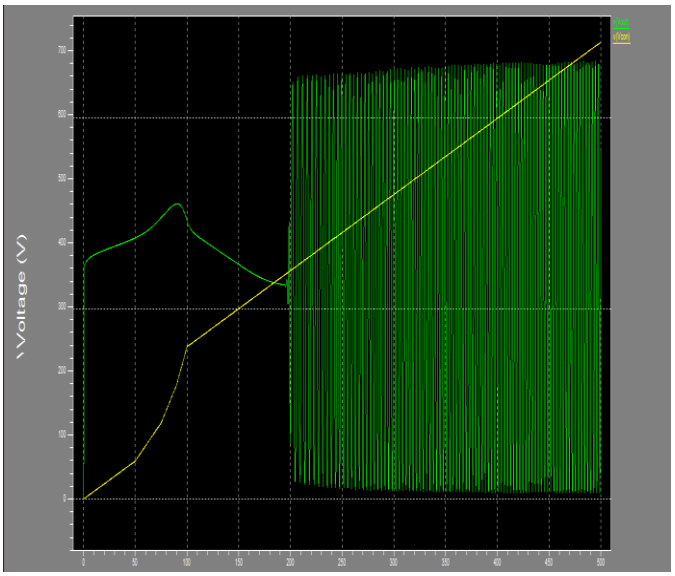

Fig. 9 Simulated results of proposed Current Starved VCO

S. No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Power (nW)
1.	0.1	0	0	0
2.	0.2	0	0	0
3.	0.3	0	0	0
4.	0.4	0	0	0
5.	0.5	0	0	0
6.	0.6	4.8	2	0.384
7.	0.7	3.8	0.26	0.049
8.	0.8	3.4	0.29	0.055
9.	0.9	3.2	0.31	0.059
10.	1.0	3.0	0.33	0.063
11.	1.1	2.8	0.36	0.069
12.	1.2	2.8	0.36	0.069

Table 3 Frequency & Dynamic Power Dissipation of Current Starved VCO

A graph is plotted between voltage and frequency, which is shown in the Fig. 10, in order to observe the relation between these two quantities.

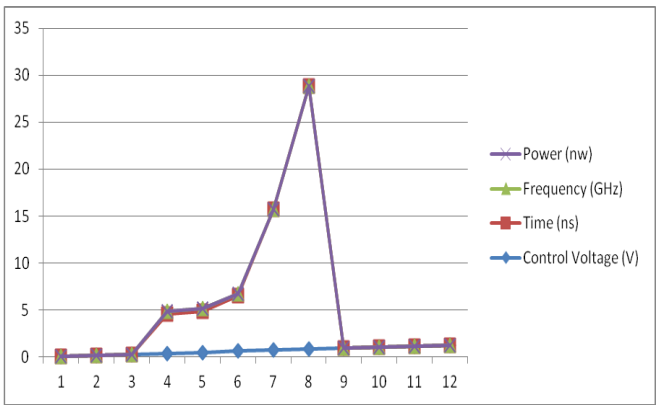

Fig.10. Voltage vs. Frequency Plot of VCO with voltage applied to both PMOS and NMOS transistors

V. VCO WITH PMOS TRANSISTORS DIODE CONNECTED

Fig. 11 delineates the VCO with PMOS transistor diode associated. It comprises of five phase ring oscillator. This ring oscillator is composed by consecutive association of odd number of inverters which frames a shut circle with positive criticism according to the imperative Barkhausan's criteria.

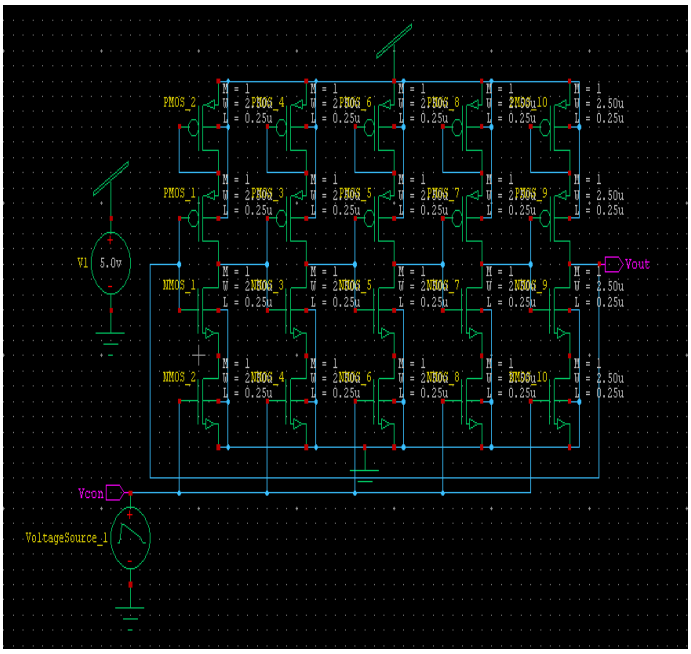

Fig. 11 Schematic Circuit of proposed VCO with PMOS transistor diode connected

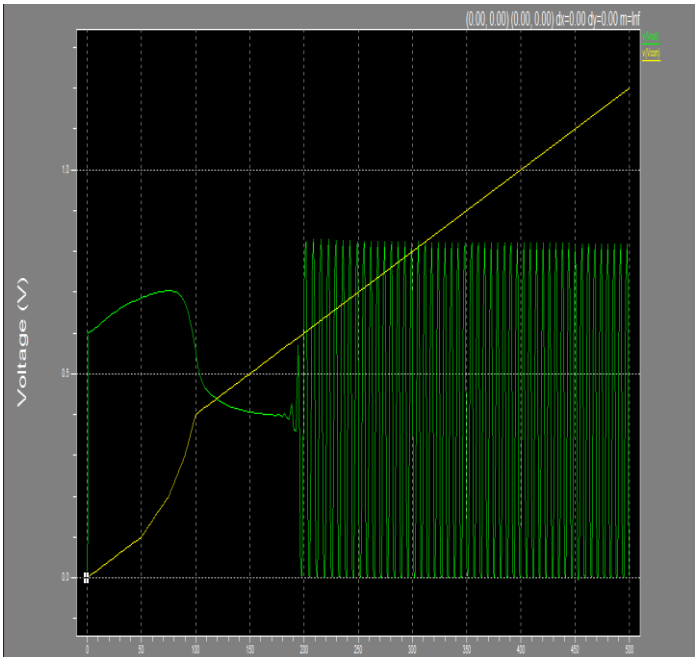

Fig. 12 Simulated results of proposed VCO with PMOS transistor diode connected

SIMULATION RESULTS:

In this paper, the VCO with PMOS transistor diode associated animated utilizing Tanner EDA T-zest test system. The VCO with PMOS transistor diode associated circuit animated utilizing Tanner EDA T-zest test system. The VCO with PMOS transistors diode associated draws greatest 0.17 GHz recurrence from supply voltage of 1 V.

S. No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Power (nW)
1.	0.1	0	0	0
2.	0.2	0	0	0
3.	0.3	0	0	0
4.	0.4	0	0	0
5.	0.5	0	0	0
6.	0.6	7	0.14	0.026
7.	0.7	6.45	0.15	0.028
8.	0.8	6.3	0.16	0.030
9.	0.9	6.3	0.16	0.030
10.	1.0	5.9	0.17	0.032
11.	1.1	5.9	0.17	0.032
12.	1.2	5.9	0.17	0.032

Table 4 Frequency & Dynamic Power Dissipation of VCO with PMOS transistor diode connected

A graph is plotted between voltage and frequency, which is shown in the Fig. 13, in order to observe the relation between these two quantities.

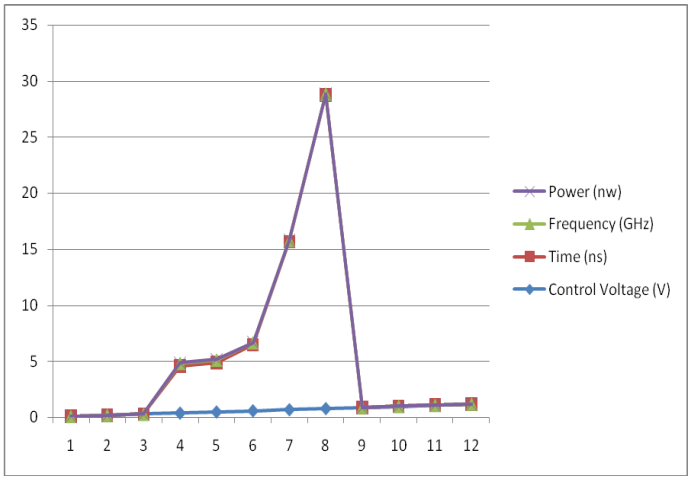

Fig.13 Voltage vs. Frequency Plot of VCO with PMOS transistor diode connected

VI. VCO WITH NMOS TRANSISTORS DIODE CONNECTED

In this paper, the VCO with PMOS transistor diode associated empowered utilizing Tanner EDA T-flavor test system. The VCO with PMOS transistor diode associated circuit invigorated utilizing Tanner EDA T-zest test system. The VCO with PMOS transistors diode associated draws most extreme 0.17 GHz recurrence from supply voltage of 1 V.

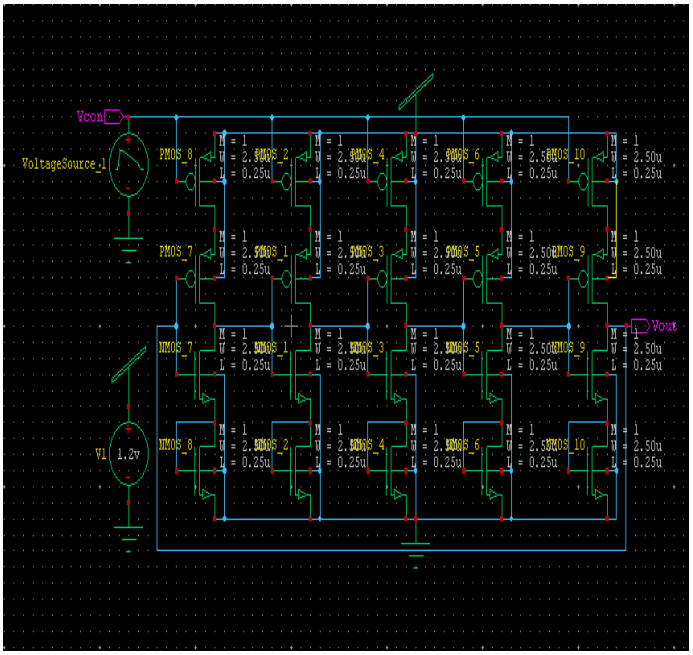

Fig. 14 Schematic Circuit of proposed VCO with nMOS transistor diode connected

SIMULATION RESULTS:

In this paper, the VCO with PMOS transistor diode associated invigorated utilizing Tanner EDA T-flavor test system. The VCO with PMOS transistor diode associated circuit animated utilizing Tanner EDA T-flavor test system. The VCO with NMOS transistors diode associated draws greatest 0.19 GHz recurrence from supply voltage of 0.7 V.

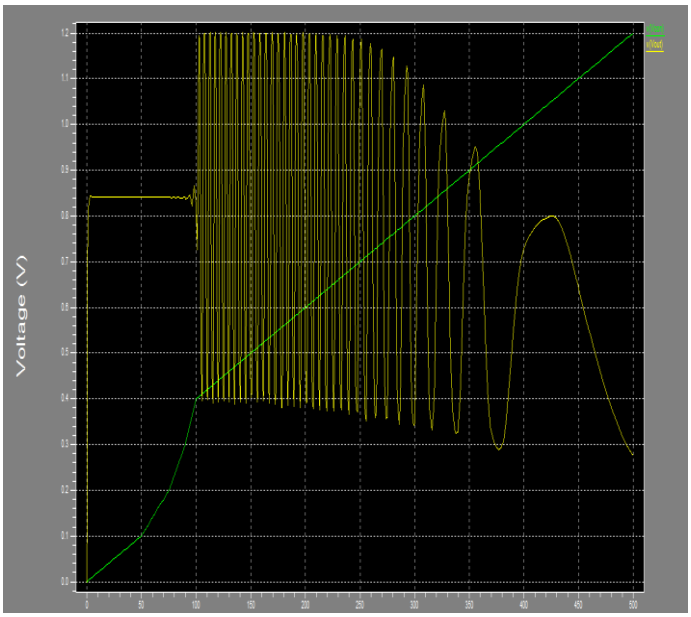

Fig. 15 Simulated results of proposed VCO with NMOS transistor diode connected

S. No.	Control Voltage (V)	Time (ns)	Frequency (GHz)	Power (nW)
1.	0.1	0	0	0
2.	0.2	0	0	0
3.	0.3	0	0	0
4.	0.4	4.2	0.23	0.044
5.	0.5	4.4	0.22	0.042
6.	0.6	5.9	0.17	0.032
7.	0.7	15	0.06	0.011
8.	0.8	28	0.03	0.005
9.	0.9	0	0	0
10.	1.0	0	0	0
11.	1.1	0	0	0
12.	1.2	0	0	0

Table 5 Frequency & Dynamic Power Dissipation of VCO with NMOS transistor diode connected

A graph is plotted between voltage and frequency, which is shown in the Fig. 16, in order to observe the relation between these two quantities.

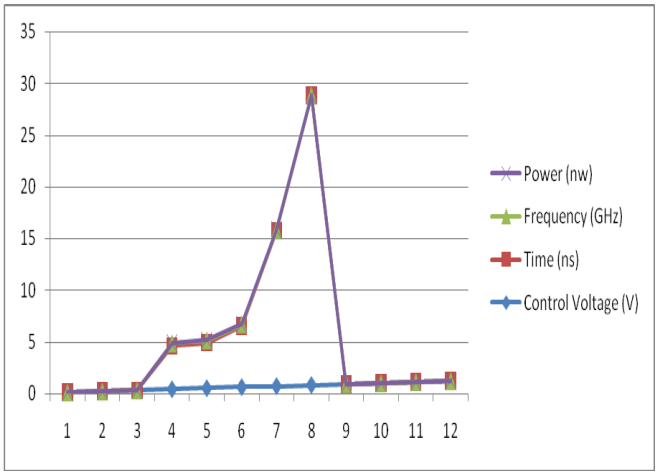

Fig.16 Voltage vs. Frequency Plot of VCO with NMOS transistor diode connected

VII. COMPARATIVE ANALYSIS OF VOLTAGE VS FREQUENCY PLOTS OF RING OSCILLATOR AND LC-VCO TOPOLOGIES

On the premise of results got from diagram plotted between the two basic parameters of ring oscillator VCO, dynamic force dissemination and recurrence for various time and control voltages, for the different ring oscillator and LC-VCO topologies, a table can is framed which looks at the consequences of the topologies under thought. Table 6 as appeared underneath sets up the correlation.

S. No.	Topology	Frequency (in GHz)		Power Dissipation
		Fmin.	Fmax.	(nW)
1.	Current Starved VCO	0.26	2	0.049
2.	VCO with gates of PMOS Transistors Grounded	0.11	0.44	0.021
3.	VCO with source voltage applied to both PMOS and NMOS transistors	0.06	0.2	0.011
4.	VCO with PMOS transistors diode connected	0.14	0.17	0.026
5.	VCO with NMOS transistors diode connected	0.03	0.23	0.005
6.	Single Switch LC-VCO.	5.4	6.9	0.0036
7.	Double Switch LC-VCO	10.2	11.79	0.0100
8.	Single Switch with current source LC-VCO	8.89	9.80	0.0129

Table 6: Performance Comparison of topologies under consideration in terms of power and frequency

The above tabular results are plotted in the form of a graph, as shown in Fig. 17, which establishes an excellent comparative study of Voltage Vs frequency plots of various ring topologies of VCO.

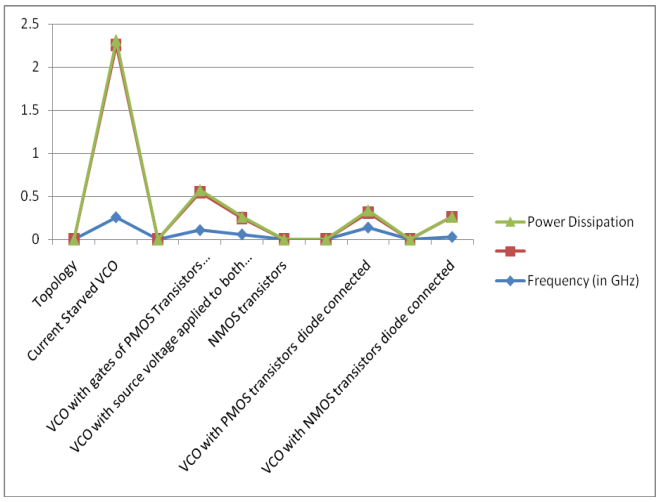

Fig. 17: Comparative analysis of Voltage Vs Frequency of ring and LC VCO topology

VIII. CONCLUSION

The proposed work sets up the distinctive sorts of VCO topologies and their examination on the premise of their voltage, force and recurrence in 32 nm CMOS innovation. These VCO's topology is outlined utilizing ring oscillator. The different topologies which we have utilized are present Starved planned utilizing ring oscillator VCO, VCO with PMOS Diode Connected and VCO with NMOS Diode Connected, VCO with Gates of PMOS Transistors Grounded, VCO with Source Voltage Applied to Both PMOS and NMOS Transistors.

For the recreation of VCO topology, Tanner EDA fourteenth form apparatus is utilized. For the recreation of these VCO's, supply voltage of 1.2 V. is utilized. On the premise of that power dissemination and recurrence is created. The diverse topology is having distinctive force dispersal and recurrence. In contrast with other VCO topology, Current Starved VCO is having higher force scattering and regarding recurrence, Current Starved VCO is having higher recurrence when contrasted with others.

Table 6 demonstrates the examination between Ring VCO and LC-VCO on the premise of force scattering and recurrence. The Current Starved VCO is having recurrence shifting from 0.26 GHz to 2 GHz and that of VCO with entryways of PMOS Transistor Grounded is from 0.11 GHz to 0.44 GHz and that of VCO with PMOS Diode Connected is from 0.14 GHz to 0.17 GHz and that of VCO with NMOS Diode Connected is from 0.03 GHz to 0.23 GHz while that of VCO with voltage connected to both PMOS and NMOS Transistor is from 0.06 GHz to 0.20 GHz. Regarding power dissemination at focus recurrence, VCO with NMOS transistors diode associated VCO is having most reduced force scattering of 0.005 nW. While most astounding force scattering is in the Current Starved VCO

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