Design of Aging-Aware Reliable Multiplier using Adaptive Hold Logic

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Abstract—Digital multipliers are among the most critical arithmetic functional units. The overall performance of these systems depends on the throughput of the multiplier. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias ($V_{gs} = -V_{dd}$), increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers.

In this paper, we propose an aging-aware multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column- or row-bypassing multiplier. The experimental results show that our proposed architecture with 16 × 16 column-bypassing multipliers can attain up to 62.88% performance improvement respectively compared with 16×16 fixed-latency column-bypassing multipliers. Furthermore, our proposed architecture with 16 × 16 row-bypassing multipliers can achieve up to 80.17% performance improvement as compared with 16×16 fixed-latency row-bypassing multipliers.

Index Terms—Adaptive hold logic (AHL), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), reliable multiplier, variable latency.

I. INTRODUCTION

Digital multipliers are among the most critical arithmetic functional units in many applications such as the Fourier Transform, Discrete Cosine Transforms, and digital filtering. The performance of these systems is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Hence, the variable-latency design is proposed to reduce maximum power consumption and timing waste of traditional circuits. The variable-latency technique divides the circuit into two parts, they are, the shorter paths and the longer paths. Shorter paths can execute correctly in one cycle. In case of the longer paths, it needs two cycles to execute. When shorter paths are activated frequently, the average latency of variable-latency designs is better than that of traditional designs. Latency is the delay from input into a system to desired outcome. Also, it is well known that multipliers consume most of the power in DSP computations. Hence, low power column-bypassing multipliers and row-bypassing multipliers have been proposed to reduce the number of delay as well as power consumption. The delay and power reduction depends on the input bit coefficient. This means that if the input bit coefficient is zero, corresponding row or column of adders need not be activated.

II. EXISTING MULTIPLIER ARCHITECTURES

2.1. Array Multiplier

The Array multiplier is well known due to its regular structure. Multiplier circuit is based on add and shift algorithm. Each partial product is generated by the multiplication of the multiplicand with one multiplierbit. The partial product are shifted according to theirbit orders and then added. The addition can be performed with normal carry propagate adder. N-1 adders are required where N is the multiplier length.
The AM is a fast parallel multiplier and the multiplication process is as shown in Fig. 1, and Fig. 2 shows the block diagram of Array Multiplier. It consists of \((n−1)\) rows of carry save adder (CSA), in which each row contains \((n − 1)\) full adder (FA) cells. Each FA in the CSA array has two outputs: 1) the sum bit goes down and 2) the carry bit goes to the lower left FA. The last row is a ripple adder for carry propagation. The FAs in the AM are always active regardless of input. In the results 16bit, 32bit array multipliers is designed and compared.

2.2 Column Bypassing Multiplier
A column-bypassing multiplier is an advanced multiplier when compared to the traditional array multiplier (AM). A low-power column-bypassing multiplier design is proposed to reduce power and delay as well. According to Column Bypasing Multiplier the FA operations are disabled with the corresponding bit in the multiplicand is 0. Fig. 4 shows the architecture of 4x4 column-bypassing multiplier. In open literature the column-bypassing multiplier is available.

2.3 Row-Bypassing Multiplier
A low-power row-bypassing multiplier is also proposed to reduce the activity power of the AM. The internal Architecture of the Row bypassing multiplier is as shown in the Fig.4. The operation of the low-power row-bypassing multiplier is nearer as that of the low-power column-bypassing multiplier, but the difference is the selector of the multiplexers and the tristate gates. The inputs are bypassed to FAs in the second rows, and the tristate gates turn off the input paths to the FAs. Therefore, no switching activities occur in the first-row FAs; in return, power consumption is reduced. Similarly, because \(b2\) is 0, no switching activities will occur in the second-row FAs. However, the FAs must be active in the third row because the \(b3\) is not zero.
III. PROPOSED MULTIPLIER

The aging-aware reliable multiplier is designed by interlinking the Adaptive Hold Technique to the either Row-bypassing or Column-bypassing multipliers. The proposed AHT Architecture consists of different blocks such as of two m-bit inputs (m is a positive number), one 2m-bit output, one column or row-bypassing multiplier, 2m 1-bit Razor flip-flops, and an AHT circuit. The overall architecture of the Aging Multiplier is as shown in Fig.5. As the two aging-aware multipliers can be implemented using similar architecture, and the difference between the two bypassing multipliers lies in the input signals of the AHT. According to the bypassing selection in the column or row-bypassing multiplier, the input signal of the AHT in the architecture with the column bypassing multiplier is the multiplicand (Md), whereas that of the row-bypassing multiplier is the multiplicator (mr). Razor flip-flops can be used to detect whether timing violations occur before the next input pattern arrives. The functioning of the each module in the proposed multiplier is illustrated as follows:

3.1 Razor flip flop

Razor flip-flops can be used to detect whether timing violations occur before the next input pattern arrives. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch, XOR gate, and multiplexer. The main flip-flop catches the execution result for the combination circuit using a normal clock signal, and the shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal. If the latched bit of the shadow latch is different from that of the main flip-flop, this means the path delay of the current operation exceeds the cycle period, and the main flip-flop catches an incorrect result. If errors occur, the Razor flip-flop will set the error signal to 1 to notify the system to reexecute the operation and notify the AHL circuit that an error has occurred.

3.2 Adaptive hold Technique

The Adaptive Hold Technique circuit is the key component of variable-latency multiplier. The AHL circuit contains decision block, MUX and a D flip-flop. If the cycle period is too short, the column-bypassing multiplier is not able to complete these operations successfully, causing timing violations. These timing violations will be caught by the Razor flip-flops, which generate error signals. If errors happen frequently, it means the circuit has suffered significant timing degradation due to the aging effect. The overall flow of the proposed architecture is as follows: when input pattern is arrived to the column or row bypassing multiplier, the AHT circuit execute simultaneously. According to the number of zeros in the multiplicand or multiplicator, the AHT circuit will decides whether the input patterns require one or two cycles. If the input pattern requires two cycles to complete, the AHT will output 0 to disable the clock signal of the flipflops. Otherwise, the AHT will output 1 for normal operations. When the column or row bypassing multiplier finishes the operation, the result will be passed to the Razor flip-flops. The Razor flip-flops check whether there is the path delay timing violation. If timing violations occur, it means the cycle period is not long enough for the current
operation to complete and that the execution result of the multiplier is incorrect. Thus, the Razor flipflops will output an error to inform the system that the current operation needs to be re-executed using two cycles to ensure the operation is correct. In this situation, the extra re-execution cycles caused by timing violation incurs a penalty to overall average latency. However, the proposed AHT circuit can accurately predict whether the input patterns require one or two cycles in most cases. Only a few input patterns may cause a timing variation when the AHT circuit judges incorrectly. In this case, the extra re-execution cycles did not produce significant timing degradation.

Fig.7 Adoptive Hold Logic Internal Structure

IV. SIMULATION RESULT

Fig.7 (a) Proposed Multiplier Using Normal 4x4 Multiplier Schematic Diagram

Fig.7 (b) Proposed Multiplier Using Normal 16x16 Multiplier Schematic Diagram

Fig.8 (a) Proposed Multiplier Using Normal 4x4 Multiplier Result

Fig.8 (b) Proposed Multiplier Using Normal 16x16 Multiplier Result
V. CONCLUSION AND FUTURE SCOPE

This paper proposed an aging-aware variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. The experimental results show that our proposed architecture with 16x16 column-bypassing multiplier scan attain up to 62.88% performance improvement compared with the 16 x 16 FLCB multipliers, respectively.
Furthermore, our proposed architecture with the 16x16 row-bypassing multipliers can achieve up to 80.17% performance improvement compared with the 16 x 16 and FLRB multipliers. In addition, the variable-latency bypassing multipliers exhibited the lowest average EDP and achieved up to 10.45% EDP reduction in 16x 16 VLCB multipliers. Note that in addition to the BTI effect that increases transistor delay, interconnect also has its aging issue, which is called electro migration. Electro migration occurs when the current density is high enough to cause the drift of metal ions along the direction of electron flow. The metal atoms will be gradually displaced after a period of time, and the geometry of the wires will change. If a wire becomes narrower, the resistance and delay of the wire will be increased, and in the end, electromigration may lead to open circuits. This issue is also more serious in advanced process technology because metal wires are narrower, and changes in the wire width will cause larger resistance differences. If the aging effects caused by the BTI effect and electro migration are considered together, the delay and performance degradation will be more significant. Fortunately, our proposed variable latency multipliers can be used under the influence of both the BTI effect and electromigration. In addition, our proposed variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electro migration and use the worst case delay as the cycle period.

REFERENCES


