Novel Approach for implementation BISR (Built In Self Repair) With Redundancies in a System On-Chip For SRAMS

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Abstract—Therefore, we implemented an MBISR generator called BRAINS+, which automatically generates register transfer level MBISR circuits for SoC designers. The MBISR circuit is based on a redundancy analysis (RA) algorithm that enhances the essential spare pivoting algorithm, with a more flexible spare architecture, which can configure the same spare to a row, a column, or a rectangle to fit failure patterns more efficiently. The proposed MBISR circuit is small, and it supports at-speed test without timing-penalty during normal operation, e.g., with a typical 0.13μm complementary metal-oxide-semiconductor technology, it can run at 333 MHz for a 512 Kb memory with four spare elements (rows and/or columns), and the MBISR area overhead is only 0.36%. With its low area overhead and zero test-time penalty, the MBISR can easily be applied to multiple memories with a distributed RA scheme. Compared with recent studies, the proposed scheme is better in not only test-time but also area overhead.

Index Terms—Redundancy Analysis, SoC, SRAM, MBISR.

I. INTRODUCTION

With a trend of system-on-a-chip, a circuit or a system needs higher capacity of embedded memories. RAM is major component in present day SOC. When systems are fabricated in emerging nano-technologies it indicates a rising level of static and dynamic faults, due to new fault mechanisms Reliability is a key aspect of any SRAM chip. To detect the faults that can occur within a memory chip, extensive testing is carried out by both manufacturers and users of those chips. Fault detection in 3D memories is even more important due to additional processing involved in building a multilayered chip. Most of these techniques belong to the dedicated BISR scheme in which each memory has a self-contained BISR circuit, e.g.,[2]-[5]

Typically, the BISR circuit only represents a small portion of the corresponding memory area. However, it is common that there are several hundreds of memory cores in a complex SOC. If each memory core with redundancy has a dedicated BISR circuit, then area of the BISR will increase dramatically. Therefore, efficient yield enhancement techniques for memory cores are essential. Built in self-repair (BISR) technique is a widely-used and efficient approach for the yield improvement of memory cores with redundancy [4]-[1]. Although soft errors are less susceptible which affect the reliability of SRAM memory chips they are still a cause of concern. These errors can occur due to excess variations in node voltages, resulting in flipping of the data stored in the cell. In 3D memory chips, integration can result in reduced lengths of global wires and increased lengths of local wires; resulting in increased chip density, better latency, wide bandwidth and lower power consumption [5].

II. EXISTING THEORY

MEMORY built-in self-repair (MBISR)[1] is increasingly necessary for system-on-chip (SoC) and highly integrated products, because embedded memories are occupying a significant amount of chip area (over 70% in many cases) [2]. Besides, memories are normally very dense and more susceptible to process variation and defects than logic circuits. As a result, embedding large memories without repairability in an SoC will likely result in a very low chip yield. Moreover, for faster yield ramp-up and shorter time- to-volume, it is necessary to develop effective and efficient methodologies and tools such as memory test and repair. This work was supported in part by the National Science Council (NSC).
redundancy scheme evaluator [5], and even MBISR schemes [1]. The need for MBISR generator follows naturally [3]. Nevertheless, 2-D redundancy repair using general row and column spares (identifying a row/column cover in an optimal way) is an NP-complete problem [3].

There have been many MBISR architecture schemes reported recently [1]-[2], including even a commercial implementation [2]. An optimal solution called comprehensive real-time exhaustive search test and analysis (CRESTA) [3]- [4] is equipped with parallel exhaustive analyzers, which is an extreme case due to very high area overhead. To reduce hardware overhead, [2] and [4] trades time with area. Heuristic redundancy analysis/allocation (RA) algorithms are widely used to solve the NP-complete problem with reasonable time complexity, area, and repair rate. The tradeoff among repair rate, test time, and area is not straightforward. Examples can be found. The spares are normally rows, columns, or words [2]. However, as the size of the embedded static random access memory increases dramatically, recently, [2], [3], RA algorithms have been limited to dealing with row/column spares. We do need more sophisticated spares [2] to improve the spare utilization and repair efficiency.

Fig1. Proposed MBISR Scheme.

III. PROPOSED SYSTEM

Embedded memories contain several hundreds of memory cores which constitute a significant portion of the chip area for typical system-on-chip (SOC) designs. With the shrinking transistor size and aggressive design rules, memory cores are easily prone to manufacturing defects and reliability problems. As these circuits have higher complexity and more sharing signals than logic blocks, they have higher failure possibilities. In order to solve this problem; designers usually add redundancy to embedded memories. Most of faults are single cell transient fault; the area of spare is effectively utilized by replacing defected cell with spare cell. Continuing advancements in semiconductor technology have made sure that the integrated circuit industry keeps following the Moore’s law, which predicts doubling the circuit density at a constant rate. This has been possible due to continuous scaling of CMOS transistor size and innovations in packaging. BISR is actually known and available for regular structures such as memory blocks, but is little difficult to implement on irregular logic.

So the repairable memories play a vital role in improving the yield of chip. In this paper we present the efficient Reconfigurable Built-in Self Repair (ReBISR) circuit which increases repair rate. The proposed repair circuit is Reconfigurable for less area, used to repair multiple memories with different in size and redundancy. Built-in self-repair (BISR) techniques are widely used for enhancing the yield of embedded memories. The techniques used for yield improvements in memories are Built In Self Test (BIST) and BIRA. BIST will verify the memory location by using MARCH CW algorithm. BIRA will perform built-in redundancy-analysis using BIRA algorithm for redundancy allocation. A shared parallel BISR can test and repair multiple RAMs simultaneously. Typically, many RAMs with various sizes are included in an SOC. Memory designers usually employ efficient built-in redundancy-analysis (BIRA) algorithms which can costeffectively be realized with built-in circuitries that are required for BISR schemes. Which are done by using spare rows and/or spare columns and spare I/O.

IV. ORGANIZATION OF MEMORY

The simplified organization of a 2m+n-bit memory chip is shown in Figure 2. Activating one of the 2m block lines is performed by the row Decode.
A. SRAM Operation Modes

In access mode, SRAM users can decide whether the BISR is used based on their needs. If the BISR is needed, the Normal-Redundant words will be taken as redundancy to repair fault. If not, they can be accessed as normal words.

At the beginning, the reset signal, forces the memory selector to send all the memories to the normal mode. In this state all memory cores can be accessed normally, i.e., the test circuits are transparent to the user. When the memory selector receives the Test signal from the processor, the selected memory core enters the test mode and receives the test commands from the processor. If a fault is detected during the test process (when the test algorithm is running), the processor pauses the test algorithm and runs the ESP algorithm to find out how to reconfigure the address of the faulty cell. This is done by the memory selector that forces the memory core to enter the reconfiguration mode. When the reconfiguration process finishes, acknowledged by the selected memory core, the processor sends the Done signal to resume the memory testing process, and the memory goes back to the test mode.

V. BUILT IN SELF TEST (BIST)

A. Top level Architecture

At the top level, the BIST circuits together behave as a wrapper to the memory. Figure 4 below illustrates the direction of information flow in the system data, address, read strobe, write strobe, and block enable are input from a memory bus, to a multiplexer (MUX). The BIST also inputs its own version of these signals to the MUX, with BIST block enable as the MUX control signal. During a test, BIST is control; during writes it sends addresses and data to the memory and during reads it sends addresses to the memory and expected data to BISR. A memory failure is determined by BISR when its CAM overflows because too many repairs have been attempted MBIST is used to test the on chip memories.
statistical analysis shows that this type of redundancy is able to achieve a very high Fault Coverage and Repair Ratio. Our new 3D structure maintains the same read/write stability. This design utilizes the Spare Registers to allocate 3D redundancy elements. We can also program the parameter of the ReBIRA scheme to meet different requirements. It uses a spare memory generated from the same memory generator as for the main memory without any built-in redundancy. Other important features of this BISR scheme are its programmability, low access time penalty, and speed testing by reusing the on-chip processor core. The programmability is again due to the proposed reconfiguration mechanism of our architecture requires negligible hardware overhead. According to experimental results, it also concludes that our approach improves the repair rate significantly. Simulation results has been verified that the proposed BISR architecture performs well even for high defect densities and requires a low memory area overhead, which had drastically improved the repair rate in comparison with the typical BIRA scheme. Especially for the defective RAMs with transient faults, the proposed scheme can provide a higher repair rate. Future challenges in embedded SOC memory testing will be driven by the following items:
1. Fault modeling: New fault models should be established in order to deal with the new defects introduced by current and future (deepsubmicron) technologies.
2. Test algorithm design: Optimal test/diagnosis algorithms to guarantee high defect coverage for the new memory technologies en reduce the DPM level.
3. BIST: The only solution that allows at-speed testing embedded memories
4. BISR: Combining BIST with efficient and low cost repair schemes in order to improve then yield and system reliability improve the yield and system reliability.

REFERENCES

Author’s Profile: Rubeena Afshan received her graduation in Electronics and Communication Engineering, 2012 from balaji institute of engineering and science and pursuing m tech in balaji institute on engineering and science. And her interested area includes analog vlsi and digital vlsi and present working as assistant professor in balaji institute of engineering and science . V.Karthik Kumar received the B.Tech. Degree in Electronics and Communication Engineering from Jayamukhi Institute of Technological Sciences(C4), J.N.T.U.Hyd in 2008 & M.Tech. Degree in Embedded Systems from Ramappa Engineering College(87), JNTUH in the year 2010. He has teaching experience of 05years & currently working as Asst. Professor in Balaji Institute of Engineering & Science, Narsampet, Warangal. Dist, Telangana, India in the Dept. of Electronics and Communication Engineering. He published 01 paper in International and National conferences.