Vernier Ring Oscillator Delay line based TDC using FPGA

Zalak Soni[1], Arpit Patel[2], Deepak Kumar Panda[3], Amit Basu Sarbadhikari[4]
[1]PG Student, GTU PG School, Gandhinagar
[2,3,4] Physical Research Laboratory, Ahmedabad

***Abstract*- Power consumption, system stability and resolution of system are most important factors in time interval measurement. Time interval measurement is needed in many TOF (time of flight) applications e.g. TOF mass spectrometer and TOF particle detector. In this paper, vernier delay line with ring oscillators based TDC (Time to digital converter) is presented for time interval measurement between two pulses. To achieve low power this algorithm is implemented on Actel Flash based FPGA. This delay line mainly comprises of two oscillators with slight difference in their frequencies, phase detector and two counters. Manual placement of the critical elements needs to be done in order to improve resolution of the system. Circuit of oscillators phase detector, design flow and timing simulation (post-layout simulation) results of implemented delay line are discussed in this paper.**

***Index Terms*- Time to Digital Converter (TDC), Field Programmable Gate Array (FPGA), Vernier Ring oscillator based Delay line, Low Resolution, Time of Flight (TOF) applications, Time interval measurement**

I. INTRODUCTION

Time interval measurement is essential for TOF applications in physics experiments as well as its needed in many medical, nuclear science and industrial applications. In time interval measurement measure between two physical events or two different pulses generally called as START and STOP signals can be digitally measure by time to digital converter. The minimum time interval that can be resolved by TDC is said to be resolution of the system. TDC can be used with many kinds of delay line discussed in different literature. [1]

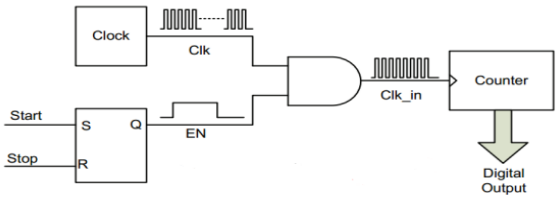

Figure 1: Basic TDC architecture

Architecture of basic TDC is as shown in figure 1. Enable signal generated from Start and Stop signal and System clock will be given to end gate. Output of end gate will be given to counter which counts number of clock cycles. After that multiplication of clock frequency with number of counts will give the input time interval [9]. Waveform of simple TDC is shown in figure 2.

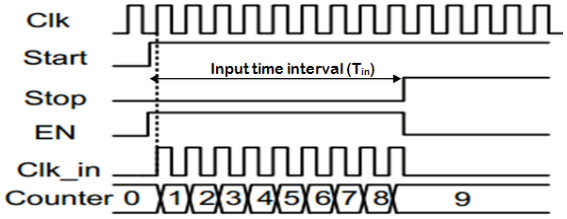

Figure 2: Waveforms of basic TDC

In this architecture, main disadvantage is that it needs large frequency of system clock to detect small time intervals. To overcome this disadvantage many techniques are available. Most of the literature uses vernier delay line [5,13,14] and tapped delay line[7] to detect smaller time intervals.

Detailed algorithm of vernier ring oscillator based delay line is discussed in section II. Followed design flow to design TDC is discussed in section III and results are discussed in section IV.

II. RELATED WORK

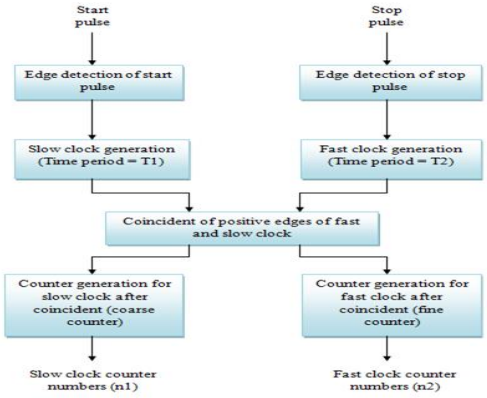

Figure 3: Algorithm of Vernier ring oscillator delay line

An important aspect of the design is two ring oscillators (slow clock and fast clock) of small difference in time periods. These ring oscillators will measure the time difference between two pulses START and STOP, as shown in figure 3. The slow clock with period T1 will start oscillating at positive edge of START pulse and the fast clock with period T2 will start oscillating at positive edge of STOP pulse. Circuit for slow clock and fast clock is given in figure 4.

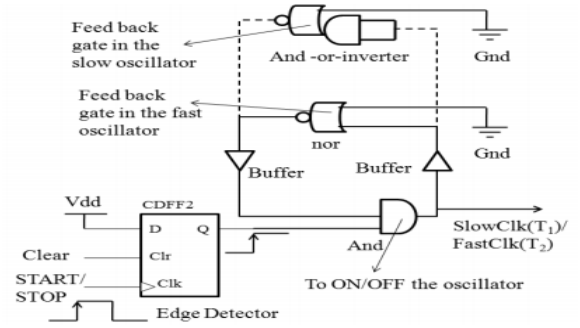

Figure 4: Slow and Fast Oscillators

Here, T2 < T1, and STOP pulse will arrive after START pulse, at some point the rising edge of the fast clock will coincide with the rising edge of the slow clock, which will detect by a phase detector. Circuit for phase detector is given in figure 5.

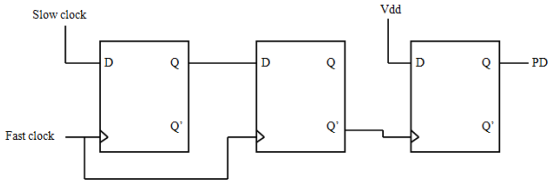

Figure 5: Phase detector

In this algorithm, slow clock and fast clock will serve as a clock to their respective counters, which are coarse counter and fine counter respectively. Both the counters will give zero when the phase detector will detect the phase coincidence of the clocks.

Formula for time interval between start pulse and stop pulse:

$T_{start\text{-}stop} = [T1 * (n1-2)] – [T2 * (n2-2)]$ (1)

Where,

T1 = Time period of slow oscillator

T2 = Time period of fast oscillator

n1 = counted number of slow clock

n2 = counted number of fast clock

Resolution of the system = T1 – T2

III. DESIGN FLOW

Design flow for implementing above algorithm is shown in figure 6. First step for the design process is to create verilog code and testbench for followed algorithm. Pre-synthesis simulation has been done to verify the algorithm. After verifying the algorithm next step is to check whether the generated hardware is same as required hardware or not. Next step is to place and route all the cells and I/O pads generated by synthesis tool. Then timing requirement has been checked by timing simulation. In timing simulation or post-layout simulation delay of different cells as well as wire delay of interconnection between cells and between I/Os and cells is included. If timing is not same as required timing then placement of component needs to be changed. When timing met was same as required timing then algorithm has been implemented on FPGA.

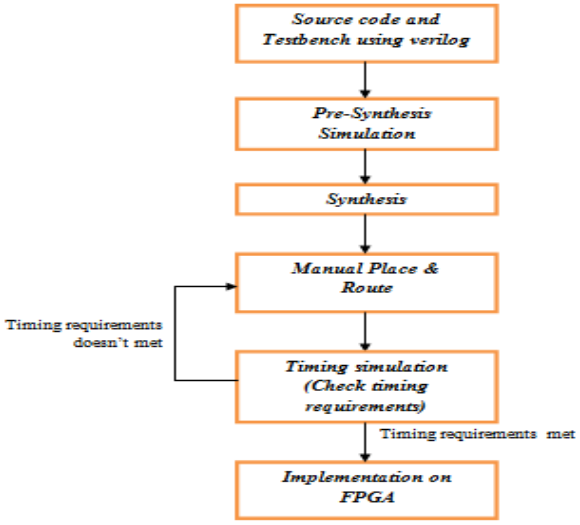

Figure 6: Design Flow

IV. RESULTS

After followed design flow discussed in section III, results of post layout simulation or timing simulation is shown in below figures. As we can see slow clock of 7.82 ns has been generated and fast clock of 6.817 has been generated. So, resolution of the system is nearly about 1 ns.

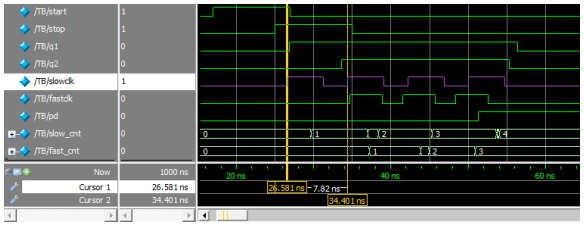

Figure 7: Time period of slow clock

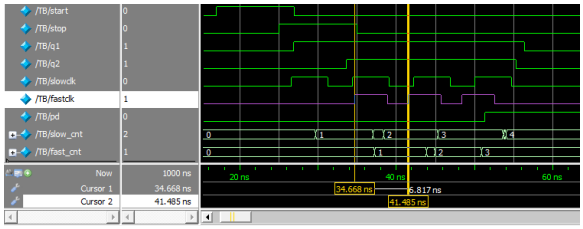

Figure 8: Time period of fast clock

IV. CONCLUSION

To decrease the power consumption and instability of the system because of higher clock frequency in time of flight applications, it is necessary to implement some alternative technique which can be used to measure the time interval. Vernier ring oscillator based delay line can give significant improvement in resolution. The paper demonstrated performance of vernier oscillator based delay line using verilog.

V. ACKNOWLEDGMENT

I would like express my deep sense of gratitude and whole hearted thank to all my project mentors for their support, encouragement and valuable guidance. And I would also like to thank my parents and friends for the inspiration and help..

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