Acquisition and Tracking of IRNSS Receiver on MATLAB and Xilinx

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Abstract- **The proposed research work aims to understand the IRNSS (Indian Regional Navigation Satellite System) as a hole and receiver in particular. The work focuses on implementing digital signal processing of Acquisition and Tracking blocks of the receiver on FPGA (Field Programmable Gate Array). Various techniques recently in use for Acquisition and Tracking was analysed from a performance point of view. The objective of the proposed research work is to contribute to the development of the commercialized IRNSS receiver, which must be cost effective with reasonably acceptable performance.**

The IRNSS receiver will be comprised of two major modules: 1) RF Front-End and 2) IF Signal Processing on FPGA. RF front-end should be comprised of two modules RF chain and ADC. RF chain is meant for receiving L5 (1176.45 MHz) and S (2492.028 MHz) band RF carrier signal from satellites and convert them into IF signal. ADC will convert Analog IF signal into Digital IF signal. The second module, IF signal processing on FPGA, is made up of various signal processing blocks such as Acquisition, Tracking, Sub Frame Identity, Ephemeris & Pseudo Range and User Position Calculation.

Index Terms- **Acquisition, IRNSS, MATLAB, Tracking & Xilinx**

I. INTRODUCTION

Indian Regional Navigation Satellite System (IRNSS) is a new independent navigation satellite system developed by Indian Space Research Organisation (ISRO) for India. Service area of IRNSS is landmark of India and surrounding 1500km from Indian boundary. It gives two types of services first is standard positioning services (SPS) which is open for all users and second one is restricted services (RS) which can use only authorized persons. Standard positioning services gives less than 20m accuracy and restricted services gives 0.1m accuracy. IRNSS works on L5 band (1176.25MHz) and S band (2492.028MHz).

Fig.1 Indian Regional Navigation Satellite System (IRNSS)

IRNSS made up of three segment

1. Space Segment
2. Control Segment
3. User Segment

Space Segment-The IRNSS space segment comprise of 7 satellites (3 GEO and 4 GSO). The 3 GEOs will be situated at 32.5^o E, 83^oE and 131° E and the 4 GSOs have their longitude crossings 55° E and 111.75^o E (two in each plane).

SATELLITE NAME	LAUNCH DATE	ORBIT
IRNSS-1I	12-April-2018	Geo-Synchronous Orbit / 55° East longitude Inclination 29°
IRNSS-1H	31-AUG-2017	55° East longitude Inclination 29°
IRNSS-1G	28-APR-2016	129.5^o East longitude with 5.1^o Inclination
IRNSS-1F	10-MARCH-2016	32.75^o East longitude with 5^oInclination
IRNSS-1E	20-JAN-2016	111.75^o East longitude 29^oInclination
IRNSS-1D	28-MAR-2015	111.75^o East longitude 31^oInclination
IRNSS-1C	15-OCT-2015	Geo-stationary earth orbit / 83^oE in 5° inclined orbit
IRNSS-1B	04-APR-2014	Geo-stationary earth orbit / 55^oE in 29° inclined orbit

IRNSS-1A	01-JUL-2013	Geo-stationary earth orbit / 55^OE in 29° inclined orbit

Table-1. IRNSS Satellites

Control Segment -The maintenance and operation of the IRNSS constellation done by Ground Segment. Following are the ground segment part:
-IRNSS Control Facility of Spacecraft (IRSCF)
-ISRO Navigation Centre (INC)
-IRNSS Range and Integrity Monitoring Stations (IRIMS)
-IRNSS Network Timing Centre (IRNWT)

User Segment-User segment which is receives satellite signal, encode satellite signal and get satellites navigation and pseudo-range, by satellite position and pseudo-range receiver calculated user position The User segment (Receiver) is consists of:
-Single frequency IRNSS receiver which is capable of receiving SPS/RS signal at L5 or S band frequency.
-A dual frequency IRNSS receiver which is capable of receiving SPS/RS signal in both L5 and S band frequencies.

II. IRNSS RECEIVER

The signals transmitted from the IRNSS satellites are received by the antenna. The input signal is amplified to a proper amplitude and the frequency is converted to a desired output frequency by the radio frequency (RF) chain. An analog to-digital converter (ADC) is used to convert received analog signal into digital signal. The antenna, RF chain, and ADC are the front end used in the receiver.

After the signal is digitized, FPGA is used to process it. Acquisition means to find the signal of a certain satellite. The tracking program is used to find the phase transition of the navigation data and reduce the phase transition by Phase Lock Loop (PLL) technique. The acquisition and tracking are performed by hardware in conventional receiver. The sub frames and navigation data can be obtained by the navigation data phase transition. Ephemeris data and pseudo ranges can be obtained from the navigation data. The ephemeris data are used to obtain the satellite positions. Finally, the user position can be calculated for the satellite positions and the pseudo-ranges.
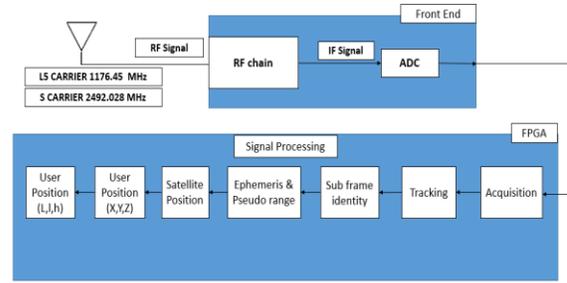

Fig.2 General Block Diagram of IRNSS Receiver

III. PRN CODES FOR SPS

Selected Standard Positioning System PRN Code and GPS C/A Gold codes both are same. Each code length is 1023 chips. The chipped rate of code is 1.023 Mcps.

The two polynomials G1 and G2 are as defined below for SPS code generation:

G1: X10 + X3 + 1 and G2: X10 +X9 + X8 + X6 +X3 + X2 + 1

Polynomial G1 and G2 are same as to the ones used by GPS C/A signal. Maximum Length Feedback Shift Registers (MLFSR) is used for the G1 and G2 generators realization. Length of MLFSR is 10bits. The chip delay is provides by the initial state of G2. The final 1023 chip long PRN sequence is generated by operation of XOR'ed between G1 and G2. The PRN sequence time period is 1 millisecond.
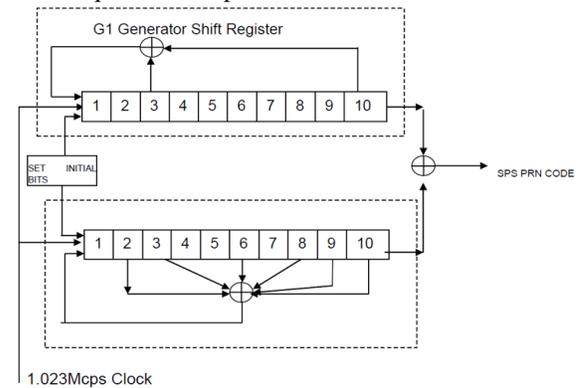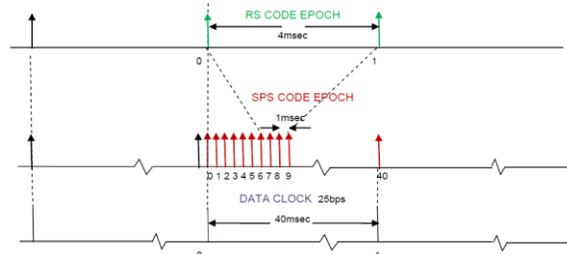

Fig.3 SPS code generator

Fig.4 IRNSS Code Timing Diagram

IV. ACQUISITION AND TRACKING

A. Acquisition of Satellite Signal

Once the digital IF signals are found, two important parameters must be measured. First is the PNR beginning code period and the second one is the carrier frequency of the input signal. A set of input data contains signals received from several satellites. Each signal is contains of different PNR code with a different starting time and different Doppler frequency. The acquisition method is to find the PNR beginning code and use this contain to dispread the spectrum. The PRN beginning code and the carrier frequency are the parameters followed by the tracking block.

The received IRNSS digital IF signal can be represented as

$r[n] = \sqrt{A}\, d[n\text{-}\tau]\, c[n\text{-}\tau]\, \cos[2\pi(f_{if} + f_d)nT_s\text{-}\varphi] + N$

Where, A is the carrier power; d[n] is the navigational data, c[n] is the C/A code, f_{if}, f_d, denote the Intermediate Frequency (IF) and Doppler shift (Hz) respectively, Ts= 1/Fs stands for the sampling period (seconds), Fs is the sampling frequency (Hz), φ is the initial carrier phase, τ is the initial code delay (samples), and N is the Additive White Gaussian Noise.

First step of acquisition is the carrier renovation from the received digital IF signal by mixing it with replica of carrier signal. Replica carrier signal frequency is same as IF frequency signal. Satellite movement gives the information about the Doppler frequency. The Doppler shift range is ±6 KHz for static user and ±10 KHz for dynamics user. The incoming IF signal is correlated with the replica of PRN code after the carrier frequency is removed. So all possible shifts in PRN code carried by the correlation process. Therefore, the acquisition process is two-dimensional process: Doppler shift to IF frequency and code delay. Show in the fig.5
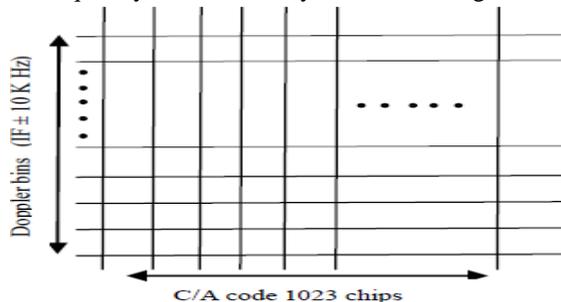

Fig.5 Signal acquisition search process

B. Tracking of Satellite Signal

The main tracking purpose is to refund the coarse values of code phase and frequency and to keep track of these by the signal properties change over time. Mainly tracking system can be classified in to Code and Carrier tracking.

Code tracking: In code tracking system, three local code (replicas) are generated and correlated with the incoming signal from acquisition system. The code tracking is implemented by delay lock loop (DLL).

Carrier frequency/phase tracking: Carrier tracking is mostly implemented by two ways either the frequency tracking or phase tracking
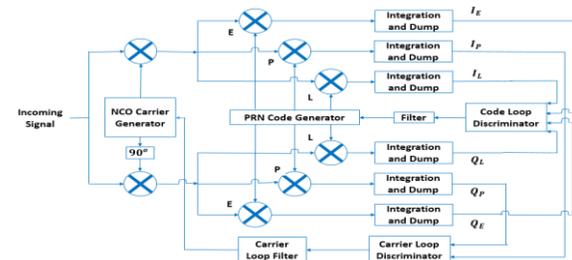

Fig.6 Block diagram of a complete tracking channel on a IRNSS receiver

Costas loop (PLL) is followed by code tracking, early-late tracking loop (DLL) in the combined code and carrier tracking loop the carrier tracking. Here the code loop discriminator is used by the early and late outputs of the in-phase and quadrature arm and the carrier loop discriminator is used by the prompt outputs of both In-phase and quadrature arm. The navigation data provided by the prompt output of the In-phase arm.

V. RESULTS

Chapter is combines of various results and analysis. Results like as SPS code generation, Tracking system simulation and Tracking Channel net-list implementation in Xilinx platform and PRN code phase and frequency bins implements in MATLAB. Timing & Power analysis also given for Ripple Carrey Adder and Look Ahead Carrey Adder by this chapters

A. SPS code generation in Xilinx

Below Figure mention the locally generation of PRN code in Xilinx Fig.7 shows the PRN code in between

0ns to 1150ns clock time and Fig.8 shows the PRN code in between 1150ns to 1200ns clock time.
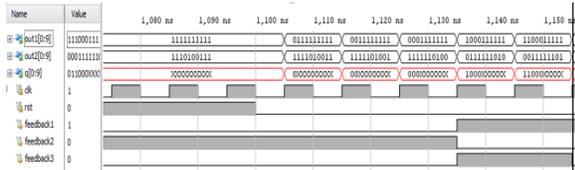

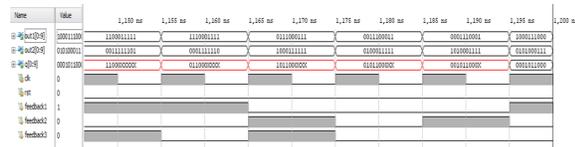Fig.7 PRN1 Code Generation in Xilinx (Clock Time: 0ns to 1150ns)

Fig.8 PRN1 Code Generation in Xilinx (Clock Time: 1150ns to 1200ns)

B. *Tracking System Simulation in Xilinx*

Shows fig.6 of tracking block diagram that indicate the Early, Prompt and Late Signal for making accurate tracking system and get for perfect correlation. Following fig.9 is that generation of prompt Signal and Fig.10 is shows the generation of late signal.
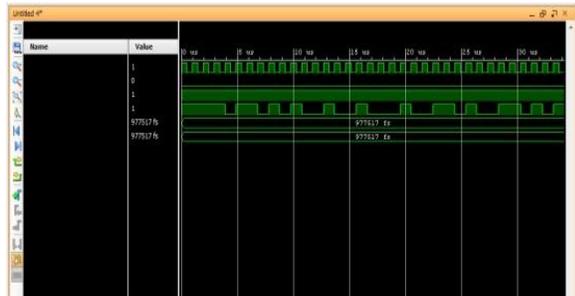

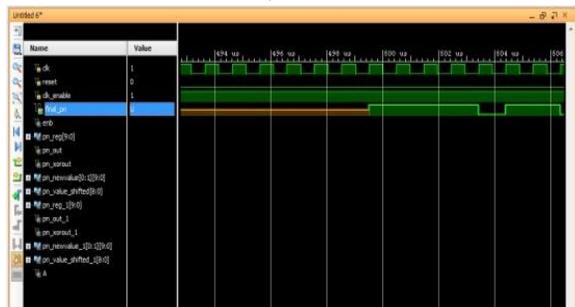Fig.9 Generation of Prompt Signal for Tracking System

Fig.10 Generation of Late Signal for Tracking System

C. *tracking Channel net-list implementation in Xilinx*

In this design we had implemented 7 tracking channels each channel consist of Clock generator,

Code Numerically Controlled Oscillator, Squaring of the signal etc. As shown in the figure below.
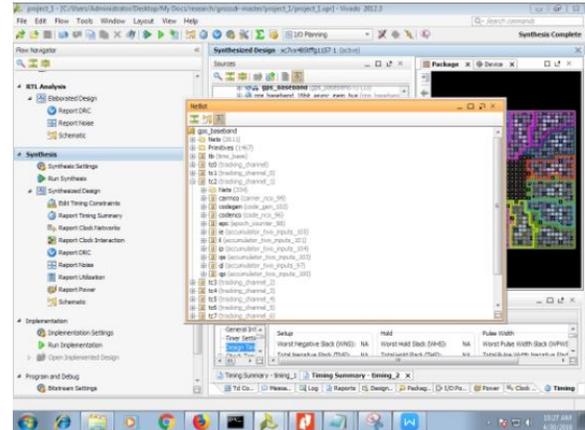

Fig.11 All Channels Net-list implementation

D. *PRN Code phase and carrier Bins in MATLAB*

Blow figure indicate the code phase bins at 0 and 70 Hz input signal frequency. Fig.12 is for PRN1 where code phase is around 100 chips.Fig.13 is indicate the correlation between in coming signal and locally genereted signal. But here the both signal has a same frequency that why it gives the correlation pick at 0 frequncy. This is called auto correlation process.
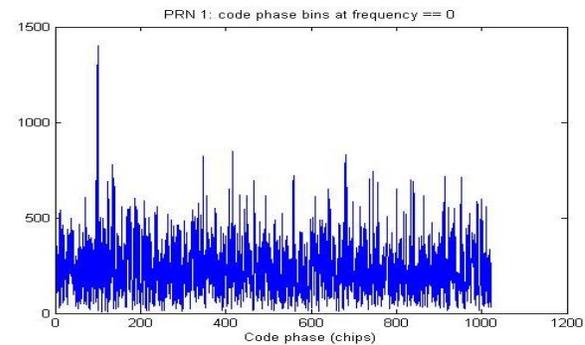

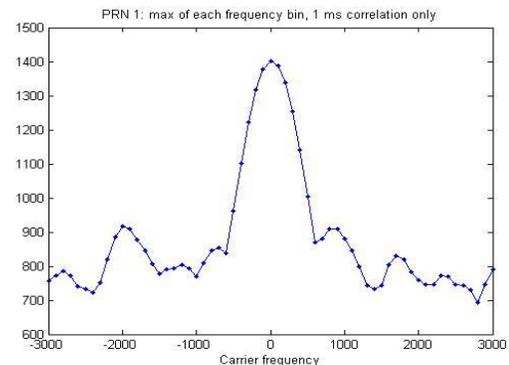Fig.12 Code Phase bins at frequency = 0 for PRN1.

Fig.13 max of each frequency bin for 1ms correlation.

D. Timing and Power Analysis

As we know the performance of a GPS receiver depends on the response of Acquision & Tracking. To improve the timing we need to reduce the worst case time. So it can acquire the signal as soon as possible. Here we are not bothering about the Signal to Noise Ratio of the signal because it includes in front end part. In back end part for error correction Cyclic Redundancy Checks are used.

Worst Case Analysis	With Ripple Carry Adder	With Look Ahead Carry Adder
	4.443 ns	3.902 ns

Table-2. Worst Case Timing Analysis

In this table we are comparing the power analysis of GPS with ripple carry adder and look ahead carry adder in Look ahead carry adder the power dissipation(Dynamic) is less because the switching is less although there is an increase in static power because the no of components is increased.

Static + Dynamic Power	With Ripple Carry Adder	With Look Ahead Carry Adder
	205mw-Static + 70mw-Dynamic	206mw-Static + 65mw-Dynamic

Table-3. Static and Dynamic Power Analysis

VI. CONCLUSION

Acquisition is the most important step to an IRNSS receiver because one must detect the signal. The acquisition generates two important parameters: the carrier frequency and the initial phase of the PRN code. In general, acquisition performed on long data will increase the receiver sensitivity. This project describes the implementation of acquisition of IRNSS signal in MATLAB by auto correlation function and tracking signal as prompt and late is implemented on Xilinx. In this report covers the timing and power analysis between Ripple Carry Adder and Look Ahead Carry Adder. Look Ahead Adder is faster but it consumes high power compare to Ripple Carry Adder. The novel FFT technique demonstrated in this report is an alternative to averaging correlation

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