A Review on MIPS RISC Processor

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***Abstract*- Microprocessor is a programmable electronic device which is used in small system such a processors used for packet transmission, pocket calculator, digital watches, smart telephone, personal computer etc. This paper describes study of 32-Bit MIPS RISC Processor Using VHDL. It uses four different format R-format, I-format, J-format and I/O format and eight 32-bit general-purpose registers. The instruction format used in this is based on MIPS RISC (Reduced Instruction Set Computer) Processor but the design process is simple which involves instruction fetch (IF), instruction decoder (ID), execution (EXE), data memory (MEM) and write back (WB) modules of 32-bit CPU. All the modules in this design are coded in VHDL language, as this language is very useful to cope successfully with the parallelism of digital hardware. The top-level module connects all the stages into a higher level. For Simulation of the design XILINX 14.5i ISE Simulator is use.**

***Index Terms*- VHDL, MIPS, RISC.**

I. INTRODUCTION

The processor or Central Processing Unit (CPU) is the heart of the computer. It determines in a large part, how fast the computer will be and what capabilities the machine will have. As the technology, hardware along with software emerges, design alternatives also emerges. Furthermore, with the enhancement in designing processors, exceptional systems can be designed. RISC architecture is a reverberation to the developing technology and the accumulation of philosophy from the CISC designs. CISC processors were designed to simplify compilers and to improve performance under constraints such as small and slower memories. The outstanding appearance of Reduced Instruction Set Computer (RISC) are they accommodate simple yet efficacious set of instruction that can execute in single clock cycle , Register-to- Register Operations, load and store operations are used to access memory, Simple Addressing Modes, Large Number of Registers, uses the Harvard architecture, pipeline is easy due to the fixed length instruction.

Most of the processors available now days have a pipelined architecture. The pipelined processors are designed in a way that they can process more than one instruction in the same clock pulse. To achieve this phenomenon of multiple processing, the processors are designed to have multiple stages. These stages work together as single unit under common clock pulse to generate the effect of multiple processing. Generally we have Instruction fetch, Instruction Decode, Execution, Memory and Wright back stages in a five stage pipelined RISC processor. Each of these stages works as a sub processor connected in the sequence. Such that with every clock pulse each of them process one instruction and forwards it to the next stage in the sequence.

In this project, the simulation of a 32 bit MIPS RISC processor based on floating point concept will be done by using VHDL. MIPS are the abbreviation for Microprocessor interlocked Pipeline Stage. This 32-bit processor design using VHDL (Very High Speed Integrated Circuit Hardware Description Language) mainly consists of eight 32-bit General Purpose Registers, 32-bit Flag Register, A Control Unit, an Arithmetic Logic Unit (ALU), Decoder and Execution Unit and Memory Unit. This processor has fixed-length of 32-bit instructions based on four different format R-format, I-format, J-format and I/O format and eight 32-bit general-purpose registers. This processor used floating point IEEE 754 Standard format for ALU operation

II. LITERATURE CITED

Paper [1]:-Mrs. Sangeeta palekar and Mr. Nitin narkhede “32-bit RISC processor with floating point unit for DSP applications” [1]

In this paper a high speed MIPS based 32 bit RISC processor with single precision floating point unit for DSP applications is design. The design is coded in Verilog HDL, simulated on XILINX ISE 13.1 and synthesized on SPARTAN 6. Results indicate that this design is optimized in speed as well as in area.

Paper [2]:-Mr. Amit Pandey "Simulating a Pipelined RISC Processor" [2]

In this paper they designed 16 bit, five stages pipelined RISC processor that is capable of resolving Data hazards by data forwarding between the stages and handles the Control hazards by inducing stall between the instructions.Such that with every clock pulse each of them process one instruction and forwards it to the next stage in the sequence.

Paper [3]:- Aneesh Raveendran, Vinayak Baramu Patil, David Selvakumar, Vivian Desalphine "A RISC-V Instruction Set Processor-Micro architecture Design and Analysis" [3]

In this paper a 5-stage pipelined 32-bit instruction set processor compatible with RISC-V ISA has been micro-architected and analyzed the design issues / options for pipeline stages in terms of grouping of instruction, decoder logic complexity, register file access and control flow instructions.

Paper [4]:-Mrs. Rupali S. Balpande and Mrs. Rashmi S. Keote "Design of FPGA based Instruction Fetch & Decode Module of 32-bit RISC (MIPS) Processor" [4]

In this paper, they analyze MIPS instruction format instruction data path decoder module function and design theory based on RISC CPU instruction set. In this paper only Fetch module and Decode module was designed for MIPS RISC processor.

III. ARCHITECHURE OF 32 BIT PROCESSOR

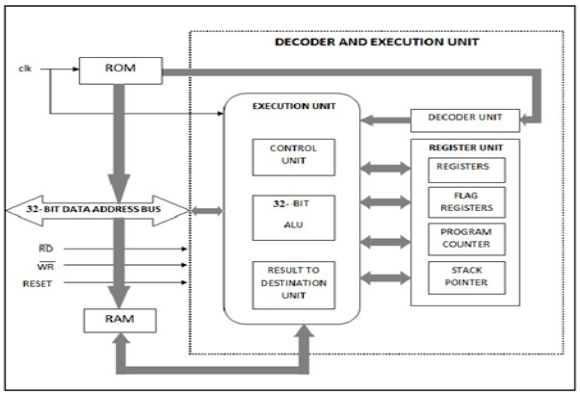

Fig1Block Diagram of 32- Bit Processor

1.32-Bit ALU:

In 32-Bit processor, ALU is of 32-Bit which can perform different arithmetic and logical operation on maximum 32-Bit number at a time. The different arithmetic operation is addition, subtraction, multiplication, division, increment, decrement etc. The different logical operation is ANDing, ORing, EX-ORing, complement etc. While ALU perform any operation either arithmetic or logical the 32-Bit result will be store into Result to Destination Unit.

2.Decoder and Execution Unit:

Decoder performs the function of instruction register and instruction decoder. Instruction register is a 32-Bit register which is used to store 32-Bit opcode. During execution of program processor will fetch the opcode from program memory and store it in instruction register. From instruction register, this opcode will be given as an input to instruction decoder. Depending upon the input to instruction decoder, one of the decoder output become active and corresponding instructional circuit available at that active output.

3.Control Unit:

The function of control unit to generate the control signal at that active output and the signals are given to all those blocks which are involved in that operation to complete the operation.

4.Register Unit:

Register unit consist of four main registers. They are as follows:

a. Registers:

It is a 32-Bit register which is used to store 32-Bit data or 32-Bit result temporary while performing any arithmetic or logical operation.

b. Flag Register:

In 32-Bit processor, flag register is of 32-Bit which consists of 32 flip-flops. Flag register is used to indicate the status of result obtained in Result and Destination Unit.

c. Program Counter:

Program counter is a 32-Bit register, which is used to store 32-Bit address of that memory location from where program opcode is to be fetched.

After every opcode read operation, PC will be auto increment by one. So that next time next opcode will be read or fetch. Thus PC can also be defined as 32-Bit register which hold 32-Bit address of next memory location from where next opcode is to be fetched or read.

d. Stack Pointer:
Stack pointer is of 32-Bit which is used to store 32-Bit address of stack top memory location in internal RAM or data memory. During PUSH operation SP will be auto increment by one.

IV. CONCLUSION

The availability of low cost, low power and small weight, computing capability makes it useful in different applications. IEEE 754 BASED SINGLE PRECISION MIPS RISC processors have high performance and less power than 32 bit processors without MIPS. VHDL is also a very useful hardware description language. It is a very powerful language with numerous languages having capability of describing very complex behavior. The CPU is described by a number of lower-level components that are instantiated to form the CPU design. The main aim of this paper is to increase frequency and relatively time is less.

V. APPLICATION

1. Personal Computer
2. Laptops
3. Game Console
4. Packet Transmission

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