Comparative analysis of different designs of Manchester Encoder based on 45nm UMC CMOS Technology

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***Abstract*- In this paper different designs of Manchester Encoder formed using CMOS inverters, Transmission Gates, NMOS switches, Pass Transistors & GDI (Gate Diffusion Input) cell that can be operated at higher frequencies are proposed. All designs have been simulated using 45nm UMC CMOS technology at 5GHz clock frequency. These designs are simulated in HSPICE tool for the successful function of the encoder. This encoder also works as XNOR gate or edge triggered D flip-flop. These designs are compared according to average power consumption, number of transistors, propagation delay and power delay product.**

***Index Terms*- Manchester code, CMOS, Optical network, Power delay product, MOSFET.**

1. INTRODUCTION

Optical access network technologies are considered as crucial characteristics of future network due to its 1 Gbit/s bidirectional transmission speed to end-users. With worldwide implementation of optical access networks, the operational cost as well as installing expenditure can be reduced. Therefore lots of attempts are conducted to modify the architecture of an optical network unit (ONU) and optical network terminal (ONT). One such instance is to continue all the light sources in OLT at the central office (CO) and ONU, whereas ONT reprocess the light which conveyed the downstream data resulting in reduced number of control related schemes and light sources in ONU and ONT. To support this several remodulation scheme were reported such as: continuous-wave (CW) light for an allotted period; differential phase shift keying (DPSK); frequency shift keying (FSK); and inverse-return-to-zero (IRZ) format. Fundamentally the CW scheme is half-duplex and requires timing control. In DPSK/FSK scheme, the constant intensity modulated downstream requires complicated transmitter/receiver structure. In IRZ scheme, with simple transceiver structure the optical power is conveyed by both logic '1' and '0'. Still, its performance reduces due to optical power fluctuation triggered by the difference in pulse width amongst the two levels.

The responsibility of a communication channel is to convey optical signal from transmitter to receiver without misrepresenting it. Most light-wave systems employ optical fibers as the communication channel as silica fibers can convey light with losses as less as 0.2 dB/km. In spite of this, optical power decreases to only 1% after 100 km. For this cause, fiber losses continue as a vital design topic and regulate the repeater or amplifier positioning of a long-haul light-wave system. Another significant design topic is fiber dispersion, which leads to widening of individual optical pulses with propagation. If optical pulses extent considerably outside their assigned bit slot, then the transmitted signal is seriously degraded.

2.CMOS LOGIC

CMOS technology has demonstrated as one of the most significant accomplishments in contemporary engineering history. Within 30 years, it has grown as the principal engine pushing the world economy. The mystery to the triumph is very modest: continue providing more functionality with lesser resources. Device scaling makes this possible. For decades, progress in device scaling has followed an exponential curve: device density on a microprocessor doubles every three years. This has come to be known as Moore's law. The minimum dimension size of a single device for present day technology is about 100 nm in gate-length. Continued

success in device scaling is necessary for further development of the semiconductor industry in the years to come. A group of leading companies publishes their projections for the next decade in the most recent International Technology Roadmap for Semiconductors (ITRS-99). The roadmap projects a device gate-length down to ~30 nm around 2014. This forecast *promises* us another ten years of brightness. Scaling beyond 30 nm, however, can be much more difficult and different. Remember, we are quite close to the fundamental limits of semiconductor physics. How much further down can we go? It is hard to answer. Nevertheless, without doubt, we are facing numerous challenges, both practically and theoretically. Device simulation requires new theory and approaches to help us understand device physics and to design devices at the sub-30nm scale. Efforts have been put forth in recent years, but much more is needed.

Scaling MOSFET's to their limits is a key challenge now faced by the semiconductor industry. Physically detailed simulations which capture the off-equilibrium transport (e.g. velocity overshoot) and the quantum mechanical effects that occur in these devices can complement experimental work in addressing these challenges. Also needed, however, is a simple conceptual view of the nanoscale transistor — to help interpret detailed simulations and experiments and to guide experimental work. Such a model has recently been outlined.

3.MANCHESTER ENCODING

Manchester encoding is a data-modulation technique that can be used in many situations but which is particularly helpful in binary data transfer based on analog, RF, optical, high-speed-digital, or long-distance-digital signals. Despite the overwhelming advantages of standard digital communication compared to analog signaling, there are some general limitations.

One is the issue of synchronization: the receiver must know when exactly to sample the incoming data.

Another is the need for DC coupling. Digital data can include long, uninterrupted sequences of ones or zeros, and thus a standard digital signal used to transmit this data will remain at the same voltage for a relatively long period of time.

Manchester encoding offers a remedy to these two limitations. It is a simple digital modulation scheme that does two things: 1) ensures that the signal never remains at logic low or logic high for an extended period of time and 2) converts the data signal into a data-plus-synchronization signal.

Manchester encoding scheme always show the transition in the data signal at the middle position of the data bit cycle. Repetition of logic '1' or '0' in NRZ data produces low to high transition or high to low transition respectively at the edge of the data bit cycle as shown in Fig. 1.

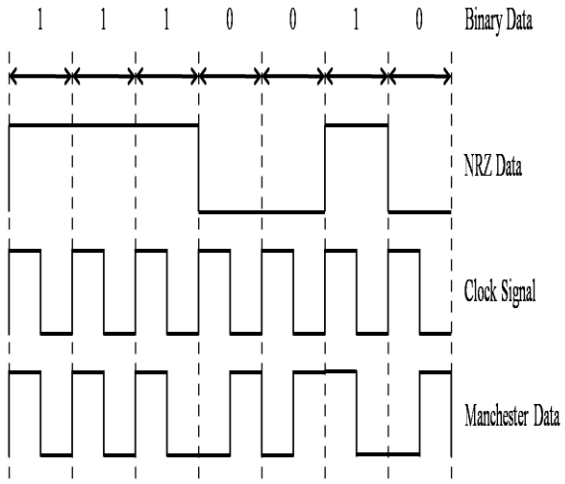

Fig-1: Waveforms for Manchester encoding

Manchester encoded data does not show any change at the edge of the data bit cycle if there is change in binary data. Manchester encoder also acts as an XNOR gate whose truth table is shown in table 1.

Table 1: XNOR gate truth table

Inputs		XOR	XNOR
A	B	Y	Z
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

4.PROPOSED WORK

In our work we have designed some efficient circuits of Manchester encoder using MOSFET which consumes less average power. All circuits are designed using 45nm CMOS technology at 5 GHz. Power supply is 1V. All the simulations are carried out in HSPICE simulation tool.

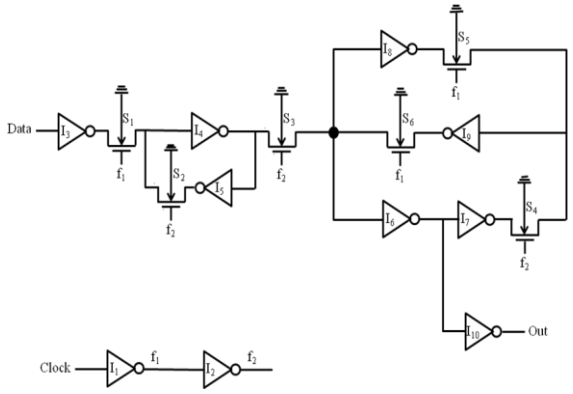

Fig-2: Manchester encoder design 1

This circuit of Manchester Encoder is designed by using NMOS digital switches and CMOS inverters. In this design an inverting latch (I_8, I_9) circuit is following a non- inverting latch (I_3, I_4, I_5) circuit. When phase f_1 happens, input signal is passed through inverter I_4. When phase f_2 occurs, inverters I_4 and I_5 latch the input signal and pass it to output node (Out) via inverters I_6 and I_{10}, at this stage inverter I_9 produces the inverse value of Out.

When the next f_1 phase occurs, inverters I_8 and I_9 latch the previously inverted output and pass it to the inverters I_6 and I_{10} and then to output node. Therefore we can conclude that rising border of the clock signal, produces the same input and falling border of the clock signal produces the inverted input at the output node. Transistors' sizes should be properly adjusted to ensure correct behavior of the circuit, to reduce propagation delay, to increase duty cycle and to reduce the power consumption of this encoder. Increase in transistor's size results in increased propagation time due to enlargement of parasitic capacitance and decrease in transistor's size directly increases the propagation time of the inverter.

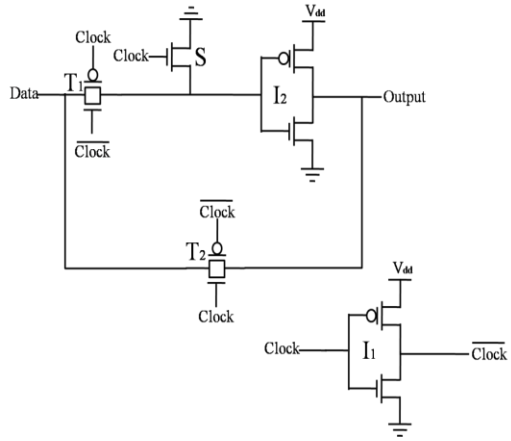

Fig. 3 Manchester encoder design 2

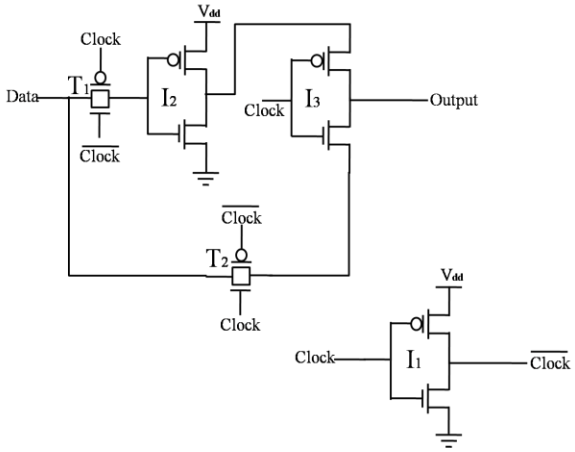

Fig-4 Manchester encoder design 3

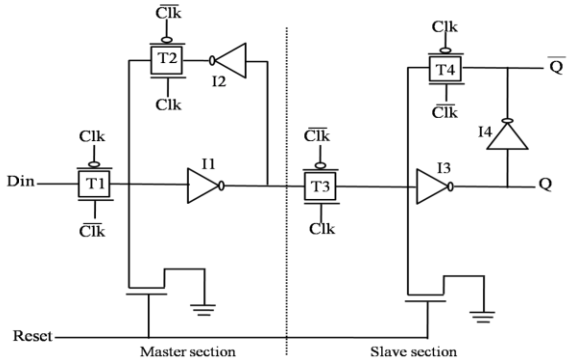

Fig-5 Manchester encoder design 4

5.EXPERIMENTAL RESULTS

In the proposed work we have considered clock signal of 5 GHz, data signal and output signal. All the designs are compared according to different parameters such as average power consumption etc. which are shown in table 2.

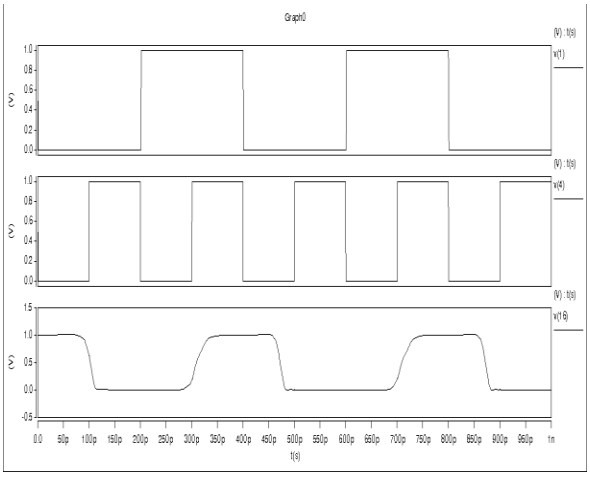

Fig-6: Output for design 1

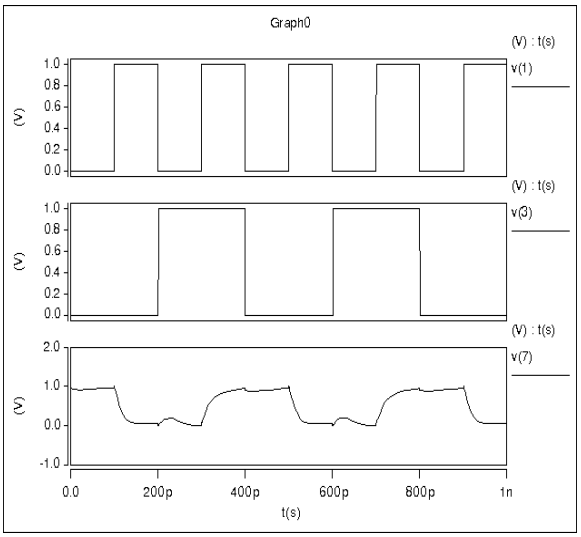

Fig-7: Output for design 2

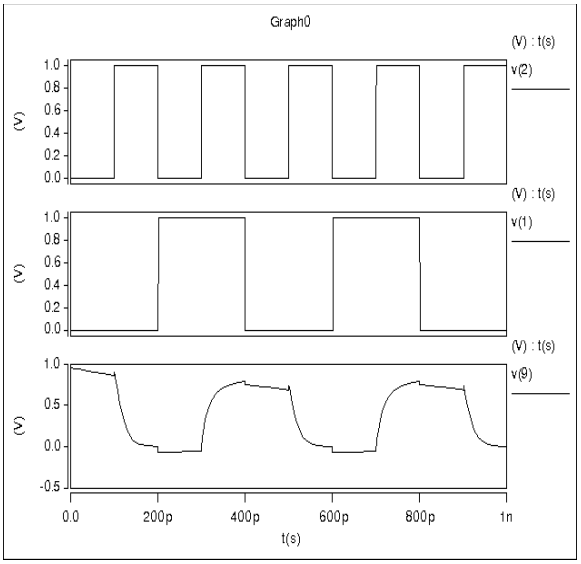

Fig-8: Output for design 3

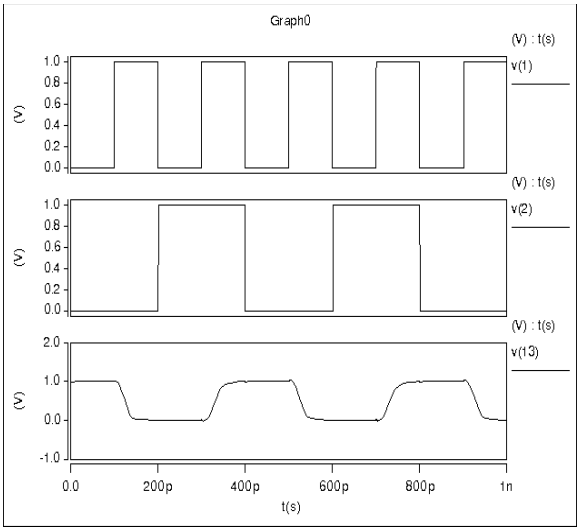

Fig-9: Output for design 4

We have calculated some parameters also which are shown in table below.

Table 2: Resultant parameters

Design No.	No. of Transistors used	Propagation Time (ps)	Average Power (µW)	PDP (fJ)
1	26	94.73	253.75	24.04
2	9	113.71	218.93	24.89
3	10	115.65	85.58	9.897
4	18	127.72	759.74	97.03

6. CONCLUSIONS

In conclusion we have successfully designed different forms of Manchester Encoder using CMOS inverters, NMOS switches, pass transistors and Gate Diffusion Input (GDI) cell. Each circuit structure has been designed using 45nm UMC CMOS technology. All the designs have been simulated in HSPICE and correct results have been obtained at clock frequency 5GHz with supply voltage V_{dd}= 1V and temperature = 25 degree centigrade. Design-III is considered to be the best optimized design of Manchester Encoder at 5GHz with average power = 85.58µW and power delay product (PDP) = 9.897fJ.

In future Manchester encoder can be designed at above 5GHz. As technology is getting advanced, 32nm, 22nm & 16nm UMC CMOS libraries are also available, therefore this encoder can be designed in different forms by using different components to reduce the chip size, average power consumed and total cost of the system by optimizing transistors' sizes.

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