Design of High Speed Clocked Comparators: A Survey

Vishal Ganpat Dalvi[1], *Deepak Sharma*[2]
[1]*M.Tech Scholar (ECE), LKCT, Indore*
[2]*Asst.Professor (ECE), LKCT, Indore*

***Abstract*- Comparators are basic building elements for designing modern analog and mixed signal systems. Speed and resolution are two important factors which are required for high speed applications. This paper presents a design for an on chip high-speed dynamic latched comparator for high frequency signal digitization. The dynamic latched comparator consists of two cross coupled inverters comprising a total of 9 MOS transistors. The measured and simulation results show that the dynamic latched comparator design has higher speed, low power dissipation and occupying less active area compared to double tail latched and preamplifier based clocked comparators. A new fully dynamic latched comparator which shows lower offset voltage and higher load drivability than the conventional dynamic latched comparators has been designed. With two additional inverters inserted between the input-stage and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability. Hence the paper lays down the foundation for a high speed comparator.**

***Index Terms*- High speed ADCs, Double-tail comparator, Dynamic clocked comparator.**

I. INTRODUCTION

The applications where high speed conversion is required, the high speed Analog to Digital converters are used such as flash ADCs which need a high speed comparator. A comparator is a basic building block for high speed analog to digital converters. As the supply voltage is smaller the designing of comparator is more challenging. High speed operation of comparator can be achieved by using large size transistors but they required more power and area[2].There are many techniques such as boosting[3] and methods like body driven transistor[4][5],which can handle higher supply voltage developed to meet the low voltage challenges but they have switching problem. Generally clocked regenerative comparator are used in many high speed Analog to Digital converters since they can make fast decision. Dynamic latched comparators are widely used in Analog to Digital converters because they have high input impedance, less energy required per conversion and fast speed. the speed of conventional dynamic comparator can be increased by adding few extra transistors to circuit[6].

The performance of dynamic comparator in terms of operation speed, low supply voltage is improved by simple structure called dynamic double tail comparator that works over a wide common mode range. A new dynamic double tail comparator by adding a few minimum size transistors is proposed ,this comparator structure does not need stacking of too many transistors not boosted voltage. This modification in conventional comparator design shows reduction in delay time and also reduction in supply voltage [10].

II.CLOCKED REGENERATIVE COMPARATORS

CMOS fully dynamic latched comparators are widely used in low power ADCs, they provide high operation speed, low power consumption, full swing output and high input impedance. Dynamic latched comparators use re-generative stage, which consist of inverters that give a positive feedback. This positive feedback stage is used to convert a differential voltage, from the input stage, into a full swing digital output state at a very fast rate [8].

Conventional Dynamic comparator

A conventional dynamic comparator has advantage of high input impedance and zero static power consumption. Conventional dynamic comparators are good beefiness against noise and they have less unbalancing problems but the disadvantages of this types of comparator is that a highly supply voltage is

required for a reasonable propagation delay time because of several stacking transistor [8].

Dynamic Double tail comparator

The dynamic double tail comparator can be achieved by simply adding extra transistors to conventional dynamic transistor, this dynamic double tail comparators are better at low power supply than conventional dynamic comparators because of less stacking of transistors. The dynamic double tail comparator that works over a wide common mode. This comparators have improved performance in terms of speed, noise, supply voltage at higher clock frequency as comparing to conventional dynamic comparators.

The speed of dynamic double tail comparators depend upon time taken by the load capacitance to charge and latching time (latch delay).therefore the total time of dynamic double tail comparators consist of latching time and capacitance load charging time[8].

$td = tL + tc$

where td total delay time

tL Latching time

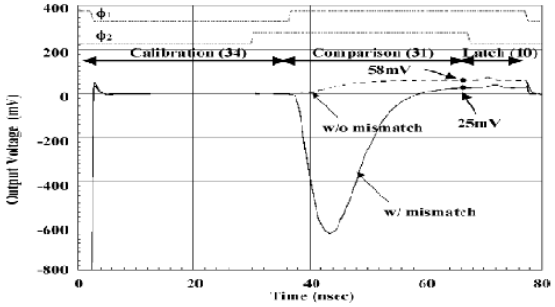
tc Capacitance load charging time

III. LITERATURE REVIEW

During the study of previous work on comparators that shows the need for very low power, fast operation and high clock frequency Analog to Digital converters use dynamic regenerative comparators. it is investigated that the parameters such as propagation time delay, energy per conversion, noise, supply voltage and sampling frequency which affect the performance of comparators and also found that there is tradeoff among these parameters.

A. CMOS multistage preamplifier deign for High-Speed and High-Resolution Comparators by Eiji Shirai

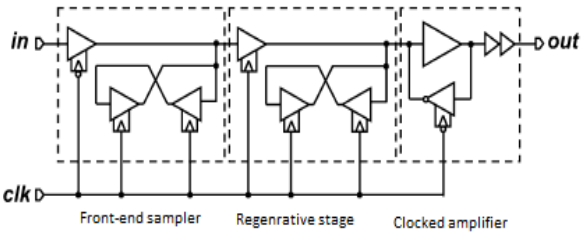
[9]In this paper, they designed multistage preamplifiers (four stage preamplifier) which are commonly used in high speed comparator to obtain sufficient gain, High speed performance and low power consumption. The main idea of this technique is to optimize, two parameters, the number of stages and the capacitance of the capacitors (offset storage),to obtain very high conversion rate. The expressions for required gain for amplifier are derived on the basis of noise.The proposed structure is fabricated in 400nm CMOS process with sampling frequency of 13Msample/s. the output result shows that the reduction in initial offsets to a great extent.



The four stage preamplifier technique used in this paper is effective to minimize power consumption and offsets of comparator but its power dissipation, energy per conversion and supply voltage can be reduced further and also it does not have better results on frequency above 13Msample/s, these are the parameters still we have to reduce.

B. 40-Gb/s CMOS clocked comparator with bandwidth modulation technique by Yusuk Okaniwa.

Fig.1 shows a clocked comparator with bandwidth modulation techniques which consist of three main parts a front end sampler, which is used for sampling and latching of input data, a regenerative stage which is amplifying stage for sampled data and a clocked amplifier which amplify the data coming from regenerative stage. This comparator is fabricated in 110nm standard CMOS technology at power supply 1.2V.



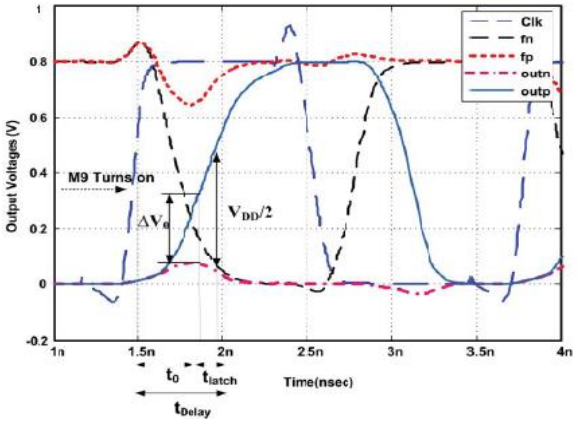
The results show sampling rate of input signal is increased to a great extent and having less bit error of this proposed comparator[10].

Now the problem in this methodology used in above proposed comparator is that, it does not reduce power consumption and it requires more die area, further we can reduce its energy required for conversion and can increase its sampling frequency.

C. Low power and low voltage inverter based double tail comparator by B. Prasanthi

In this research, the expressions were derived for comprehensive delay analysis of comparator. A new proposed double tail dynamic comparator was proposed by adding two extra N-MOSFET switches in order to reduce the propagation delay tine and power consumption. The design of proposed dynamic double tail comparator is simulated in 250 nm CMOS process. The simulation results confirmed that the delay time and energy required for conversion of proposed comparator is significantly reduced.
The results shown of above proposed dynamic double tail comparator designed in 250nm CMOS process can be improved in terms of its the delay time and power consumption, if W/L ratio of MOSFET transistors of comparator are minimized[11].

D. Analysis and design of a low voltage low power double-tail comparator by Samaneh Babayan-Mashhadi.
In this research work, a new dynamic comparator is proposed in small supply voltages for low power and high speed operation that uses the positive feedback connection for regeneration stage (amplifying stage). In this research, the analytical expressions for time delay of comparator are presented, by using these expression a new comparator is proposed . In this design a conventional dynamic comparator is modified by adding few extra minimum sized transistors. The main idea of adding these extra transistors to the proposed double tail comparator was to increase the latch regeneration speed, The design of proposed comparator is simulated in 180nm standard CMOS technology at supply voltage of 0.8V with clock frequency up to 1.1GHz. The simulation results show significantly reduction in both propagation time delay and power consumptions to a great extent for proposed comparator[8].



In the above proposed comparator, the methodology used which confirmed that is quite better in reducing propagation time delay, power consumption and effective die area but still we can improve in double tail dynamic comparator such as its time delay, power consumption, maximum sampling frequency and area.

Proposed work
In above previous research works, it is found that the following factors which affect the performance of comparator when they are designed for low power ADCs.

1. Comparator needs finite amount of time to reach final output state. This time is related to maximum speed for operation so we need reduce this time.
2. Power supply voltage coming down not large headroom available (Vdd - Vth).
3. Large die area is costly and also large bulky MOSFETs are slower and consume more power.

Latch comparators are better choice for the designing of comparator and the double tail architecture has better performance in low power applications so the design of proposed dynamic comparator is based on double tail structure, Double tail approach is better for low power low supply voltage, the main idea of proposed comparator is to design in 70nm CMOS process in order to reduce size of MOSFETs to reduces the energy per conversion, power consumption and increase sampling frequency.

Methodology
The designing of this proposed dynamic double tail comparator require some design issues which must be considered. The designing methodology for a dynamic double tail comparator for a low power ADCs are as follows

1. First of all, we will try to identify the expressions, which govern the comparator operation such as total delay time of the comparator (time taken by the load capacitor to charge and latch time), initial output voltage difference, latch effective trans conductance and energy required per conversion.
2. According to these equations we will calculate W/L ratio (width to length ratio of MOSFETs).
3. The calculated W/L ratio will be used for designing of dynamic double tail comparator.

4. All these parameters mentioned above are used to design for proposed dynamic double tail comparator in 70nm CMOS process.
5. In designing the n-MOS switches, a low-on-resistance n-MOS switch can be used in order to diminish voltage headroom limitation and try to select the size of the n-MOS switch transistor in a way that both low-voltage and low power operation are maintained.

Comparatives Results

	Multistage Preamplifier Design Method	Bandwidth Modulation Technology	Inverter Based Comparator	Double Tail Comparator
CMOS Technology	400nm	110nm	250nm	180nm
Supply Voltage	2.5 V	1.2V	1.5V	0.8V
Maximum Sampling Frequency	13MHz	2.5GHz	1GHz	2.4GHz

IV. CONCLUSION

In this comparative paper, we have presented a comparative analysis on the supply voltage, Sampling frequency, energy per conversion, power dissipation and sampling frequency of clocked dynamic comparator. There are many different techniques were used in previous works in order to improve the performance of the high speed comparators. The Dynamic double tail comparators have better performance in terms of energy, time delay, sampling frequency and power dissipation in low supply voltage. The paper presents performance comparison of dynamic double tail comparator on energy per conversion, the supply voltage, and its sampling frequency. The supply voltage and energy per conversion of this comparator can be reduced and its sampling frequency can be increased by using 70nm CMOS process to improve the performance of the dynamic double tail comparators

REFERENCES

[1] R Jacob baker, CMOS circuit design, layout and simulation, Wiley, IEEE press, Third edition, 2010.

[2] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 56, no. 11, pp. 810–814, Nov. 2009.

[3] A. Mesgarani, M. N. Alam, F. Z. Nelson, and S. U. Ay, "Supply boosting technique for designing very low-voltage mixed-signal circuits in standard CMOS," in Proc. IEEE Int. Midwest Symp. Circuits Syst. Dig. Tech. Papers, Aug. 2010, pp. 893–896.

[4] B. J. Blalock, "Body-driving as a Low-Voltage Analog Design Technique for CMOS technology," in Proc. IEEE Southwest Symp. Mixed-Signal Design, Feb. 2000, pp. 113–118.

[5] M. Maymandi-Nejad and M. Sachdev, "1-bit quantiser with rail to rail input range for sub-1V __ modulators," IEEE Electron. Lett., vol. 39, no. 12, pp. 894–895, Jan. 2003.

[6] B. Goll and H. Zimmermann, "A 0.12 μm CMOS comparator requiring 0.5V at 600MHz and 1.5V at 6 GHz," in Proc. IEEE Int. Solid-State

[7] D. Shinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps Setup+Hold time," in Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers, Feb. 2007, pp. 314–315.

[8] Samaneh Babayan-Mashhadi and Reza Lofti "Analysis and design of a low voltage low power double tail comparator" IEEE transaction Vol.22 no.2. Feb 2014.

[9] Eiji Shirai "CMOS multistage preamplifier deign for High-Speed and High-Resolution Comparators" IEEE trans. Vol.54,No.2,Feb-2007

[10] Yusuke Okaniwa, Hirotaka Tamura, Masaya Kibune, Daisuke Yamazaki, Tsz-Shing Cheung, Junji Ogawa, Nestoras Tzartzanis, William W. Walker and Tadahiro Kuroda. "A 40-Gb/s CMOS clocked comparator with Bandwidth Modulation Technique" IEEE journals.Vol.40, No. 8.Aug 2005

[11] B Prasanthi and P.Pushpalatha, "Design of Low-Voltage and low-Power inverter based Double Tail Comparator" International Journal of Engineering Research and General Science Volume 2, Issue 5, Sep, 2014 ISSN 2091-2730