A VLSI Design of LTE Turbo Encoder-Decoder with Radix 4 ACS Architecture

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***Abstract*- Wireless communication is the fastest developing portion of the communications industry. Channel coding is the most important part of digital wireless communication systems. The fading of signal due to multipath propagation causes errors which need to be corrected. The main aim of any channel coding schemes is to provide error-free data transmission by adding redundancy to information to check code and correct errors. Forward error correction (FEC) is favored strait coding procedure if the most extreme permitted transference delay is small or during the returning strait is not accessible. One imperative category of forward error correction codes are turbo codes. Turbo codes accomplish greater coding benefit and foremost utilized for error emendation in high rate wireless frameworks. This paper depicts a turbo decoder for Long Term Evolution (LTE) standard, utilizing a MAP algorithm. Long-term evolution (LTE) is expected to accomplish maximum information assess in surplus of 300 Mbps for fourth era wireless transferral networks. Turbo codes predetermined strait coding plan in LTE, experiences small decoding throughput because of frequentative decoding calculation. An effective way to accomplish favourable throughput is to utilize maximum a posteriori (MAP) basics in equidistant.**

1. INTRODUCTION

During the previous few years, 3G wireless communication requirements, inclusive of HSDPA, firmly mounted themselves as an permitting era for data-centric verbal exchange. The advent of smart-phones, internet books, and other mobile broadband gadgets sooner or later ushered in an technology of throughput intensive wi-fi applications. The fast boom in wireless statistics site visitors now begins to stress the network potential and operators are searching out novel technology permitting even higher information-prices than the ones executed through HSDPA. Recently, the new air interface widespread LTE (Long Term Evolution) has been defined by means of the requirements body 3GPP and targets at enhancing the data-costs by way of extra than 30× (in comparison to that of HSDPA) within the following couple of years. Theoretically, LTE supports as much as 326.Four Mb/s , while the enterprise plans to recognise the primary milestone at about a hundred Mb/s in 1-or-2 years. LTE specifies the use of faster-codes to make sure reliable conversation.

Parallel rapid-deciphering, which deploys more than one tender-enter tender-output (SISO) decoders running simultaneously, can be the important thing for achieving the high facts-quotes provided by LTE. However, the implementation of such may be most of the most important demanding situations in terms of computational intensity and strength consumption. The reality that not one of the recently mentioned parallel faster-decoders achieves the LTE peak facts-price or affords desirable electricity consumption for battery powered gadgets of much less than 100mW on the 100 Mb/s milestones, suggests that the structure layout for such decoders is a hard undertaking. Recently, lengthy-time period evolution (LTE) advanced has been dominated as the subsequent-generation wi-fi verbal exchange general, which is geared toward better height records fees close to a few Gb/s . The turbo decoder, which is specified in LTE, famous to be a proscribing block in the direction of this intention because of its iterative deciphering nature, excessive latency, and tremendous silicon vicinity consumption. The deciphering system is completed the usage of the algorithm foremost decoding of linear codes.

Since the implementation of the actual most a posteriori (MAP) algorithm incurs very excessive computational complexity, In order to deal with this venture, on this short, a new relation between the α and β metrics is delivered; based on this new relation, a unique add–compare–select (ACS) unit for forward and backward computation is proposed. The proposed scheme results in, at most, an 18.1% reduction in the silicon location in comparison with the designs pronounced so far.Normally, modified styles of the MAP set of rules, i.E., the max-log-MAP and log-MAP algorithms, are normally realized instead. In those opportunity techniques, the MAP middle consists of log-likelihood ratio (LLR) devices, in addition to the middle units to compute α, β, and γ, i.E., the forward, backward, and department metrics, respectively. In reality, the α and β units, due to their recursive computation nature, are the maximum challenging gadgets to implement, occupying almost 40% of the entire MAP middle location. The γ unit, on the other hand, is a trivial part of the rapid decoder, along with few addition computations. Therefore, an area-efficient architecture for α and β metrics computation is fantastically ideal, which has usually been a challenge in literature.

2. TURBO ENCODING SCHEME

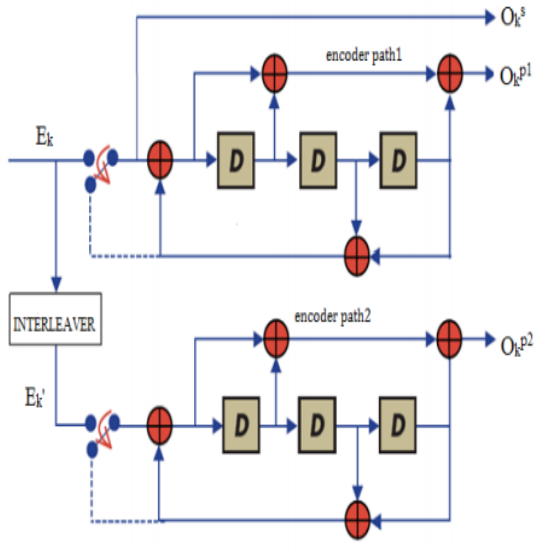

Fig-1: Turbo encoder

Turbo encoders are mainly designed by combining 2 recursive systematic convolutional (RSC) encoders with the aid of parallel concatenation technique that is separated by means of a unmarried interleaver. Fig-1 indicates the block diagram of faster encoder where the RSC encoder is chosen as rate 1/3 encoder. The input series Ek is represented by means of the binary enter values Ek = [E1, E2, E3,.....En]. These enter sequences are surpassed into the encoder path1 producing the output of systematic series Ok s and recursive redundant output collection Ok p1 referred to as the parity1 encoded bits.

The enter Ek is then interleaved the usage of a QPP (Quadratic permutation polynomial) or random interleaver. Interleaver is used inbetween to enhance the performance of turbo codes. The pseudo random interleaver is normally used, where the facts bits are examine-out in person designed fashion. These interleaved information sequences are surpassed via encoder path2 producing the opposite set of recursive redundant output collection Ok p2 referred to as parity2 encoded sequence. Thus the encoder produces three outputs from a single input, subsequently referred to as the fee 1/three encoder unit.

3. TURBO DECODING SCHEME

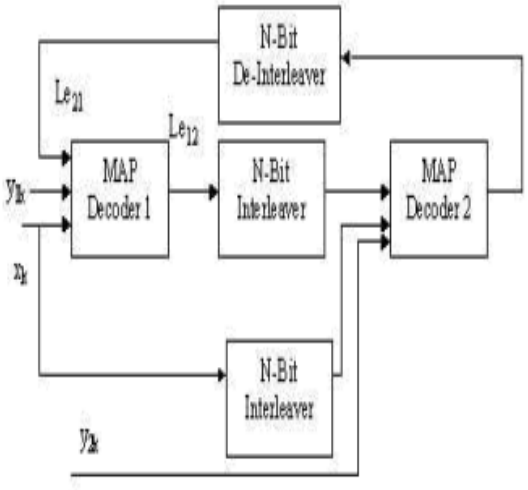

Fig-2: Turbo decoder

The deciphering plan of LTE rapid decoder is depicted in Fig. 2. In the decoder architecture, there are 2 decoders similar to 2 RSCs. Due to the existence of a remarks course as established, the operation of the faster decoder is completed in an iterative manner. For each full generation decoder contains of half of iterations such that one for every constituent code it is used. The planning of the decoder is such that the MAP decoder 1 begins running amid the number one half generation and

MAP decoder 2 works amid the second one half cycle. The 1st MAP decoder inputs are the tainted systematic array of bits Xk, the parity move of bits Y1k from the primary RSC encoder, and from 2nd MAP decoder the deinterleaved extrinsic data. To the second MAP decoder the inputs are the tainted interleaved systematic bit move, parity move of bits Y2k from 2nd RSC encoder, and from 1st decoder the interleaved extrinsic statistics. The Maximum A Posteriori (MAP) algorithm is used by Recursive Systematic Convolutional (RSC) decoders. The exemplary set of rules offers the superb deciphering executions, but it stories a completely excessive complexity at some point of implementation and coffee interpreting throughput. For those reasons the MAP algorithm is used as a reference for centered deciphering performances. The MAP set of rules, which affords the a posteriori chance for every bit, is utilized in iterative interpreting of faster codes. The MAP algorithm presents the probability of the decoded bit United Kingdom being either +1 or −1 for the obtained image sequence y by using calculation of the values as

L (uky]

Where p (United Kingdom = +1uk = −1chances of bit uk being +1 and −1, respectively.

3.1 ACS units

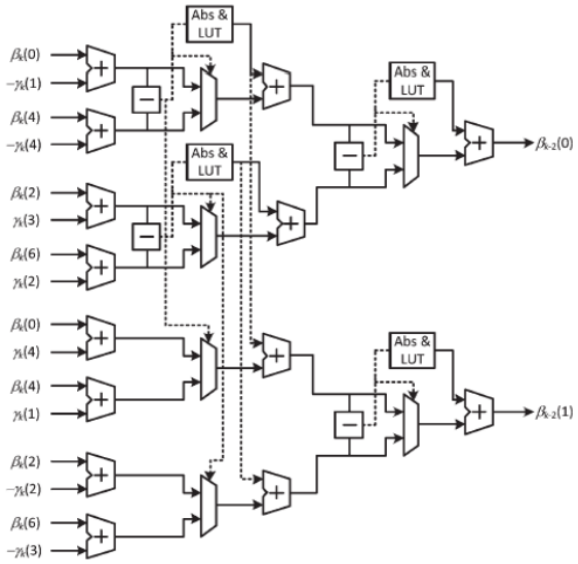

Fig-3: Radix4 ACS unit with MSR architecture

The ahead and backward recursion computation is calculated the usage of ACS architecture. The components in it include the adders, comparators and selector unit, for this reason the call ACS. The LUT (Look Up Table) is used to put in force the logarithmic time period. In order to increase the processing pace, we're combining radix2 devices to form a radix4 unit illustrated in fig-5.To understand the βk−2(0) value, each of A and B values are proposed to be applied by means of a radix-4 structure and ultimately a third radix-4 structure is used to obtain (24). A radix-four architecture employs a comparator and LUT coping with distances among two input values to pick out the maximum value, which then adds the chosen amount to the most value. It is well worth noting that the distance between two enter values of (26) is βk(zero) − βk(4) + γk(four) − γk(1), that's equal to the gap among input values of (28). The distances among each two enter values of (27) and (29) also are identical. Therefore, the compare and LUT unit for the computation of (28) and (29) are ignored main to a unique structure. Hereafter, this proposed structure is called the Maximum Shared Resource (MSR) architecture. This assets is proper for every pair of (sixteen), (17), (18), (19), (20), (21) and (22), (23) for the backward recursion metrics and also for each pair of α(0), α(four), α(1), α(five), α(2), α(6) and α(three), α(7) for ahead recursion metrics. In truth, using the proposed MSR architecture, the redundant computation is prevented, assuaging the location overhead in traditional schemes.

4. RESULTS

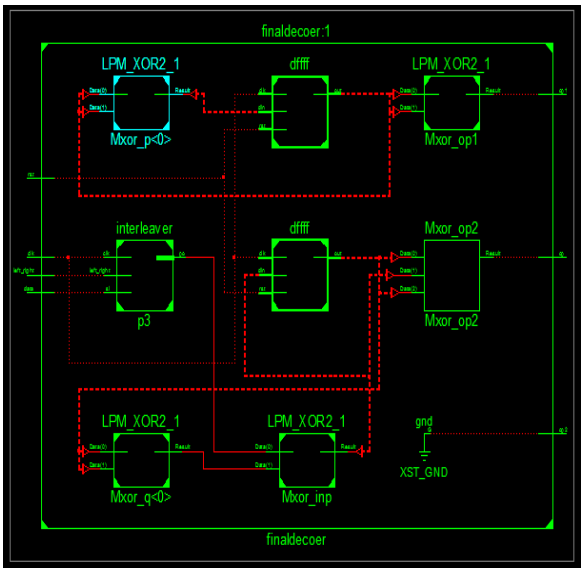

Fig4. Radix 4 ACS unit RTL SCHEMATIC

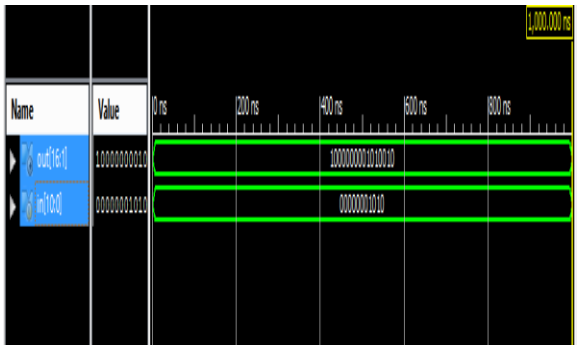

Fig5. Encoder output

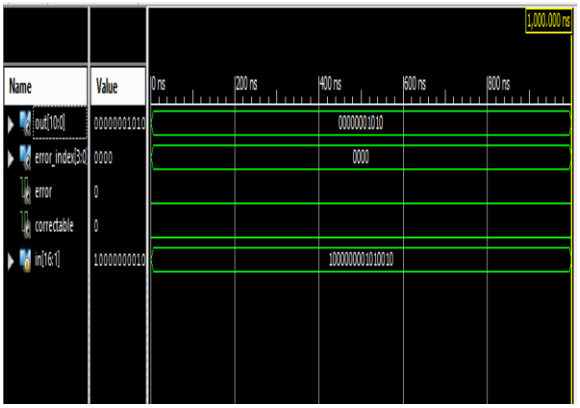

Fig6. Decoder output

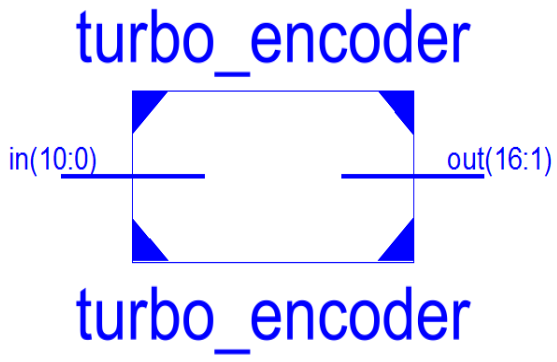

Fig7. Encoder RTL SCHEMATIC

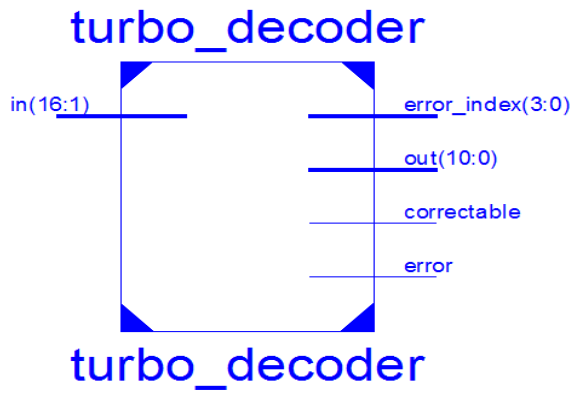

Fig8. Decoder RTL SCHEMATIC

Fig 7 and 8 shows the RTL schematic diagram of turbo encoder and decoder implemented using Xilinx 14.2. Fig 4-7 shows the simulation results for secure transmission of the data streams simulated. Initially reset is „1"and no operation is performed. When reset is „0"enc_bit_in process starts by transmitting the data bits. During reset is „0"and when dec_valid_in goes high and the output starts. Thus the output can be seen on dec_bit_out line after some latency.

4. CONCLUSION

In this paper, by investigation the relation between the rule computations, a unique methodology was projected, that is named MSR. By applying the projected methodology to the previous ACS architectures, Associate in nursing area-efficient design for algorithmic computations was achieved. The projected architectures attain at the most eighteen.1% reduction in quality in keeping with the implementation results that considerably reduces the quality of the full MAP core of the turbo decoder. What is more, the projected methodology may be used for higher base styles to cut back quality.

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