An Analytical Approach for Voltage Gain in a QZS Based Dc-Dc Boost Converter

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Abstract- **In this paper, a high step up Quasi –Z Source DC-DC converter is presented using hybrid switched capacitors switched inductor method to achieve high voltage gain. The proposed converter have solved the duty cycle limitation and voltage gain limitation while maintaining its main advantages such as low voltage stress on capacitors, diodes and switches. The proposed converter has a feature of flexible structure. The operating principle, related relationships and waveforms of the proposed converter are presented in this paper. Also, a comparison between the proposed converter and switched inductor QZS dc-dc converter is provided to confirm the superiority of the proposed converter. Simulations are done in MATLAB Simulink environment to attain high voltage gain.**

Index Terms- DC-DC Boost Converter, DC Voltage Source, Impedance Source Network, Quasi-Z Source Network.

I. INTRODUCTION

Continuous increase in the demand of electricity around the globe has created a great interest in the renewable energy sources. In order to serve high voltage applications several converter circuits are required to boost the DC output voltage. Impedance network based converters in energy conversion are introduced to overcome the disadvantages of basic dc-dc converters such as lower efficiency, higher power loss, lower reliability. They have capability of single-stage power conversion, and they could overcome the limitations of basic converters. Single-stage power conversion will result in important advantages such as fewer components, lower power loss, higher efficiency, higher reliability and lower cost. [1-11]

Z- Source converters (ZSC) is a unique impedance circuit which is connected to couple the converter main circuit to the power source unlike the traditional V/I-source converters where a capacitor and inductor are used, respectively. The impedance network shown in fig. 1, employed in a ZSC is a two-port network that consists of a split-inductor L1 and L2 and capacitors C1 and C2 connected in X shape. The dc source can be a battery, diode rectifier, thyristor converter, fuel cell, or a PV cell. Switches used in the converter can be formed by a combination of switching devices like IGBT, MOSFET or SCR, and diodes. [19]

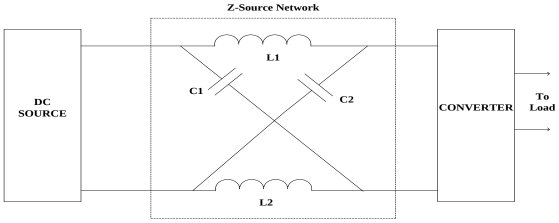

Fig. 1 Basic structure of the Z-source converter

The Z-Source converter can overcome most of the disadvantages of conventional boost converters but the discontinuous current and high voltage stress effect the reliability of the converters in a negative way.

When the ZSC is used for boost action it displays several disadvantages such as the discontinuous input current and high voltage stress on the capacitor. Moreover, control complexity is an issue when the ZSC is used in a back-to-back configuration. In order to eliminate the disadvantages of the ZSC a new circuit topology with modified structure of the ZS, known as Quasi Z-Source was introduced as shown in fig. 2.

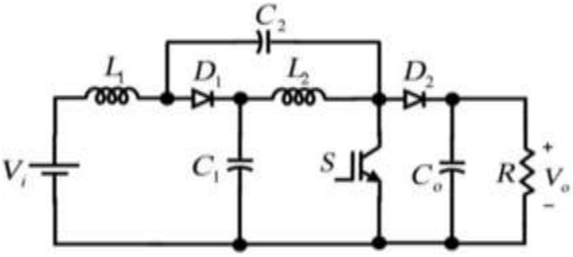

Fig. 2 Quasi Z-Source DC-DC Converter

The QZS based DC-DC converter offers several advantages such as high reliability and higher voltage gain then the traditional ZS DC-DC converter at less number of elements. But it still suffers from a disadvantage of low voltage gain. The QZS based DC-DC converter overcomes most of the limitations of ZS DC-DC converter but the voltage gain is still not as high as demanded by the high voltage applications of the DC-DC converter. [14]

Several Efforts has been made to increase the voltage gain of the QZS based DC-DC converter such use of high frequency transformers and coupled inductors but both of these methods have some of the major disadvantages: Peak of voltage/current stress on diodes and switches will be increased, the magnetic core got saturated even with a small value of dc voltage which causes disruption in the converter operation, saturation of magnetic core will result in a drastic decrease in the inductance value of transformer or coupled inductors, which causes severe stress on the switch and in the isolated converters the weight, volume and power loss are at the higher side and efficiency at the lower side. Another method proposed to increase voltage gain of the QZS based DC-DC converter is to use multiple stages of the converter but at a cost of increased number of components. This results in high power loss, low efficiency, high possibility of failure, and low reliability of the whole system.

In this paper, a QZS DC-DC boost converter is proposed. In addition to the QZS network, this converter uses switched-capacitors and an extra inductor in order to achieve high voltage gain. The proposed converter maintains the main advantages of the basic converter. Also, the voltage stress on the diodes and switch will remain unchanged, and the duty cycle of the switch won't be limited, when compared to the main QZS converter. The proposed converter has a flexible structure, and extra stages can be added to achieve even higher voltage.

II. THE PROPOSED QZS DC-DC BOOST CONVERTER

In this topology additional four switched capacitors and one switched inductor are used to increase the boost capability of the dc-dc converter as shown in fig. 3. [1]

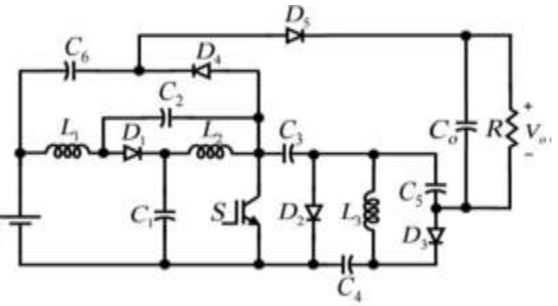

Fig. 3 A high voltage gain QZS DC-DC converter

The operation of the converter includes three operating modes. The general relation for the duty cycle of the switch stands like:

$$D = \frac{T_{on}}{T} \quad (1)$$

The on time of the switch is then stand equal to DT and the off time is given by $(1 - D)T$.

A. Mode I ($T_0 \leq t \leq T_1$)

The equivalent circuit of the converter in its first operation mode is shown in Fig. 4. This mode starts when the switch turns on. In this mode, charging of L_1 and L_2 takes place by C_1 and C_2 through the path provided by the switch. L_3 is charged by Capacitor C_3 and the load. Also, the energy of the load will be provided by the input voltage source, and C_3, C_5, and C_6 due to the conduction of D_5. Therefore, the inductors L_1, L_2 and L_3, and the capacitor C_4 get charged. Whereas, the voltages across C_1, C_2, C_3, C_5 and C_6 get discharged. This mode will terminate as the switch turns off.

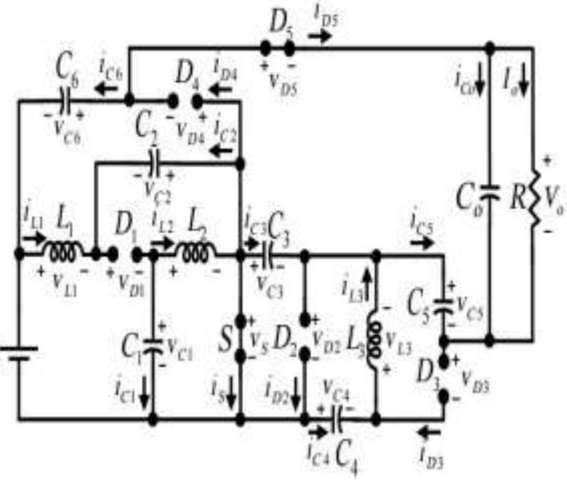

Fig.4 Equivalent circuit of the proposed converter for mode I

Through the application of the KVL following relations can be drawn for mode I operation of the converter.

$$\mathrm{V_{L1}} = \mathrm{V_i} + \mathrm{V_{C2}} \tag{2}$$
$$\mathrm{V_{L1}} = \mathrm{V_0} - \mathrm{V_{C1}} - \mathrm{V_{C3}} - \mathrm{V_{C5}} - \mathrm{V_{C6}} \tag{3}$$
$$\mathrm{V_{L2}} = \mathrm{V_{C1}} \tag{4}$$
$$\mathrm{V_{L3}} = \mathrm{V_{C3}} - \mathrm{V_{C4}} \tag{5}$$

B. Mode II ($\mathbf{T_1 \leq t \leq T_2}$)

The second mode of operation begins when the switch is turned off. In this mode, D_1, D_3 and D_4 are forward biased, while, D_2 and D_5 are reverse biased. In order to achieve the equivalent circuit for this mode of operation of the converter the mentioned on/off states of the switch and diodes are applied to the Fig 4. In this mode, the capacitors C_1, C_2, and C_3 are charged through inductors L_1 and L_2. C_6 is also charged through the path provided by D_4. Simultaneously the inductor L_3 and capacitor C_4 charge the capacitor C_5. Consequently, the capacitors C_1, C_2, C_3, C_5 and C_6 get charged, while, the capacitor C_4 and the inductors L_1, L_2, and L_3 get discharged.

By applying KVL to Mode II the following relationships can be deduced

$$\mathrm{V_{L1}} = \mathrm{V_i} - \mathrm{V_{C1}} \tag{6}$$
$$\mathrm{V_{L1}} = \mathrm{V_{C2}} - \mathrm{V_{C6}} \tag{7}$$
$$\mathrm{V_{L2}} = \mathrm{V_{C1}} - \mathrm{V_{C3}} + \mathrm{V_{C4}} - \mathrm{V_{C5}} \tag{8}$$
$$\mathrm{V_{L2}} = -\mathrm{V_{C2}} \tag{9}$$
$$\mathrm{V_{L3}} = -\mathrm{V_i} + \mathrm{V_{C3}} - \mathrm{V_{C4}} - \mathrm{V_{C6}} \tag{10}$$

C. Mode III ($\mathbf{T_2 \leq t \leq T}$)

As indicated in mode II of the operation of the converter the voltage across the capacitor C_4 falls and the voltage across capacitor C_5 rises. As v_{C4} equates v_{C5}, D_2 gets forward biased and starts conducting. Mode III of the operation begins with conduction of D_2. In this mode, the switch is still remains off, D_1, D_3 and D_4 are forward biased, and D_2 and D_5 are reverse biased. Similar to mode II the equivalent circuit can be deduced by applying the mentioned on/off states of the switch and diodes to Fig.4. During this mode, capacitors C_3 and $C_5$are charged through L_1 and L_2 and also capacitor C_6 is charged over the path provided by D_4. Due to the conduction of D_2, the capacitors C_4 and C_5 forms parallel connection and are charged through L_3. Consequently, the capacitors C_1, C_2, C_3, C_4, C_5 and C_6 get discharged and the inductors L_1, L_2 and L_3 get charged.

By applying KVL to the main circuit, it is found true that the relations for mode II are also valid for mode III. Besides this following relation can also be found true for mode III

$$V_{L1} = -V_{C4} \tag{11}$$

D. Steady State Analysis

The voltage balance law for inductor L_1 gives the following relation

$$V_i - (1 - D)V_{C1} + DV_{C2} = 0 \tag{12}$$

Similarly, application of Voltage balance law for inductor L_2 gives

$$V_{C2} = \frac{D}{(1-D)}V_{C1} \tag{13}$$

By substituting v_{C2} from (13) into (12) V_{C1} and V_{C2} in the steady state can be written as

$$V_{C1} = \left(\frac{1-D}{1-2D}\right)V_i \tag{14}$$
$$V_{C2} = \left(\frac{D}{1-2D}\right)V_i \tag{15}$$

When the voltage balance law is applied to inductor L_1 using equation (2) and (7) the following expression can be formed

$$D(V_i + V_{C2}) + (1 - D)(V_{C2} - V_{C6}) = 0 \tag{16}$$

By replacing the value of V_{C2} in equation (16) from equation (15) gives

$$V_{C6} = \left(\frac{2D}{1-2D}\right)V_i \tag{17}$$

Through the application of voltage balance law for inductor L_3 from the equations (5) and (10) gives the following relation

$$D(V_{C3} - V_{C4}) + (1 - D)(-V_i + V_{C3} - V_{C4} - V_{C6}) = 0 \tag{18}$$

Replacement of V_{C6} from (17) to (18) gives that

$$V_{C3} - V_{C4} = \left(\frac{1-D}{1-2D}\right)V_i \tag{19}$$

Application of voltage balance law for inductor L_2 using (4) and (8) gives the following relation

$$DV_{C1} + (1 - D)(V_{C1} - V_{C3} + V_{C4} - V_{C5}) = 0 \tag{20}$$

Replacing V_{C1} and $(V_{C3} - V_{C4})$ from (14) and (19) respectively into the above relation gives expression for V_{C5} as follows

$$V_{C5} = \left(\frac{1}{1-2D}\right)V_i \tag{21}$$

Now, when voltage balance law is applied for L_3 using (5), (10) and (11), the following expression can be derived

$$-V_{C4} + (D + D')V_{C3} - D'(V_i + V_{C6}) = 0 \tag{22}$$

Substitution of values from (17) and (19) into above relationship gives

$$V_{C3} = \left(\frac{1}{1-2D}\right)V_i \tag{23}$$
$$V_{C4} = \left(\frac{D}{1-2D}\right)V_i \tag{24}$$

Application of voltage balance law for L_1 from (3) and (6) gives the following expression

$$D(V_0 + V_{C2} - V_{C3} - V_{C5} - V_{C6}) + (1 - D)(V_i - V_{C1}) = 0 \quad (25)$$

While we replace all steady state capacitor voltages in above expression from (14), (15), (17), (21), (23) and (24), it gives the relation for voltage gain as

$$V_G = \frac{V_0}{V_i} = \frac{2+D}{1-2D} \quad (26)$$

III. DESIGN OF INDUCTORS AND CAPACITORS

The general relation for an inductor on a switching period is given by

$$L = \frac{V_L D}{f_s \Delta I_L} \quad (27)$$

Replacing the values of capacitor voltages in the equations of inductor voltages gives the following relation

$$\mathrm{V_{L1}} = \mathrm{V_{L2}} = \left(\frac{1-\mathrm{D}}{1-2\mathrm{D}}\right)\mathrm{V_i} \quad (28)$$

$$\mathrm{V_{L3}} = \left(\frac{1-\mathrm{D}}{1-2\mathrm{D}}\right)\mathrm{V_i} \quad (29)$$

Using the values of $\mathrm{V_{L1}}$, $\mathrm{V_{L2}}$, and $\mathrm{V_{L3}}$ in equation (27) gives us the following expressions

$$\mathrm{L_1} = \mathrm{L_2} = \left(\frac{1-\mathrm{D}}{1-2\mathrm{D}}\right)\frac{\mathrm{DV_i}}{\mathrm{f_s \Delta I_L}} \quad (30)$$

$$\mathrm{L_3} = \left(\frac{1-\mathrm{D}}{1-2\mathrm{D}}\right)\frac{\mathrm{DV_i}}{\mathrm{f_s \Delta I_L}} \quad (31)$$

ΔI_L is an indication of ripple current through the inductor and the average current passing through L_1 and L_2 is equal to input current and for L_3 it is equal to output current. Therefore, taking the ripple current as 10% of the input current for L_1 and L_2 and 50% of the output current for L_3 gives the following relations

$$\mathrm{L_1} = \mathrm{L_2} = \left(\frac{1-\mathrm{D}}{1-2\mathrm{D}}\right)\frac{\mathrm{D V_i}^2}{(0.1)\mathrm{P_{in} f_s}} \quad (32)$$

$$\mathrm{L_3} = \left[\frac{\mathrm{D(1-D)(2+D)}}{(1-2\mathrm{D})^2}\right]\frac{\mathrm{DV_i}^2}{(0.5)\mathrm{P_{in} f_s}} \quad (33)$$

Similarly, a general relation for a capacitor over a switching period is given by

$$\mathrm{C} = \frac{\mathrm{DI_C}}{\mathrm{f_s \Delta V_C}} \quad (34)$$

In above equation $\Delta \mathrm{V_C}$ is the ripple voltage for the capacitor and considered to be 2% of the voltage across capacitor. As the voltages across C_1, C_2, C_3, C_4, C_5 and C_6 has already been calculated and the voltage across C_o is equal to V_o, the capacitor values can be obtained as

$$\mathrm{C_1} = \left[\frac{\mathrm{D(1-2D)}}{1-\mathrm{D}}\right]\frac{\mathrm{P_{in}}}{(0.02)\mathrm{V_i}^2\mathrm{f_s}} \quad (35)$$

$$\mathrm{C_2} = (1-2\mathrm{D})\frac{\mathrm{P_{in}}}{(0.02)\mathrm{V_i}^2\mathrm{f_s}} \quad (36)$$

$$\mathrm{C_3} = \left[\frac{\mathrm{D(1-2D)^2}}{2+\mathrm{D}}\right]\frac{\mathrm{P_{in}}}{(0.02)\mathrm{V_i}^2\mathrm{f_s}} \quad (37)$$

$$\mathrm{C_4} = \mathrm{C_5} = \mathrm{C_6} = \left[\frac{(1-2\mathrm{D})^2}{2+\mathrm{D}}\right]\frac{\mathrm{P_{in}}}{(0.02)\mathrm{V_i}^2\mathrm{f_s}} \quad (38)$$

$$\mathrm{C_o} = (1-\mathrm{D})\left(\frac{1-2\mathrm{D}}{2+\mathrm{D}}\right)^2\frac{\mathrm{P_{in}}}{(0.02)\mathrm{V_i}^2\mathrm{f_s}} \quad (39)$$

IV. COMPARISON

In order to present a comparison between the proposed converter and the other topologies of QZS based dc-dc converters Table 5.1 has been created. Table 5.1 displays voltage gain, maximum duty cycle of the switch, voltage stress on the components of the converter.

As shown in Table 1 the proposed converter can achieve higher voltage gain than the other topologies of QZS based converters. It shows the capability of high step up with less number of switches and without any limitation of the duty cycle as compared to the other topologies of QZS converters. It has also been shown that the duty cycle of the switch can be varied to the maximum value of 50%. [14]

In order to provide a comparison of voltage gain among various QZS based converter topologies a comparative graph is prepared. The graph is shown in Fig. 5 where variation of voltage gain against the duty cycle is shown for different converter topologies. From a close observation, it can be noticed that the curves has steeper slope for the QZS converters other than the proposed converter while duty cycle is near Dmax.

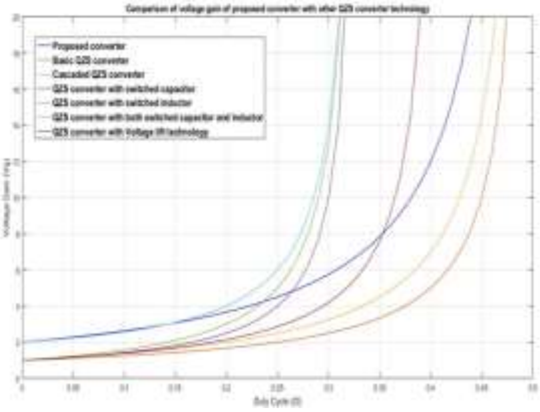

Fig. 5 Voltage gain comparison between proposed converter and other QZS based converter topologies

The proposed converter also has the capability of reaching higher voltage gains through adding extra stages. The stages can be increased by repeating the part including C3, C4, D2, and L3.

The study also presented a comparison of proposed QZS based dc-dc converter and other topologies of QZS based converters. Keeping in view the results obtained through the comparison the superiority of the proposed converter is also confirmed in terms of voltage gain, duty cycle limitation, voltage stress and consequently reliability and efficiency. The voltage gain of the proposed converter decreases for very low and very high duty cycles, which this issue is expected for all step up converters.

The proposed converter includes one drawback that the input and output does not share a common ground and this drawback can be worked upon. Besides this there is an inrush current in diode D5 for a time period of a few micro seconds.

TABLE 1 COMPARISON OF THE PROPOSED CONVERTER WITH OTHER QZS BASED TECHNOLOGY

S. No.	Name of Topology	Voltage Gain	Max. duty cycle	Advantages and shortcomings
1	Basic QZS based dc-dc converter	$\frac{1}{1-2D}$	0.5	• Low voltage gain • High voltage stress
2	Cascaded QZS dc-dc converter	$\frac{1}{1-3D}$	0.33	• Voltage gain was increased • Possibility to extend number of stages • Voltage gain improvement was not significant • Limited duty cycle • Voltage gain is still low
3	QZS dc-dc converter with switched capacitor	$\frac{1+D}{1-2D}$	0.5	• Improvement in voltage gain • Reduction in voltage stress • The voltage gain is still not satisfactory
4	Switched inductor QZS converter	$\frac{1+D}{1-2D-D^2}$	0.41	• Voltage gain was further improved • Limited duty cycle • Increased voltage stress • Voltage gain was not very high
5	Active switched capacitor and switched inductor QZS converter	$\frac{1+D}{1-3D}$	0.33	• Voltage gain was further improved • Limited duty cycle • Increased voltage stress • Increased number of switches • Voltage gain was not very high
6	QZS converter with voltage lift techniques	$\frac{2(1-D)}{1-3D}$	0.33	• Improvement in voltage gain was further improved • Limited duty cycle • Increased voltage stress • Voltage gain was not very high
7	Proposed converter	$\frac{2+D}{1-2D}$	0.5	• Capable of producing high voltage gain • Less stress on the components • Feasibility of adding extra stages

V. SIMULATION RESULTS

In order to achieve the high voltage gain of the proposed converter, simulations are done in MATLAB Simulink version R2017a. The simulation parameters are shown in table 4.1

A DC voltage source of 50 Volt is applied to the proposed converter. The converter includes seven inductors and seven capacitors to derive the proposed topology. The inductors L1& L2 and capacitors C1& C2 form the Z-Source circuit. While the inductor L3 and capacitors C3, C4, C5& C6 are used as switched inductor and switched capacitors respectively. A resistive load of 500 Ω is used to collect the output. An inductor L0 and a capacitor C0 are connected across the load to make the output voltage stable.

TABLE 2 PARAMETERS USED FOR SIMULATION OF PROPOSED QZS CONVERTER

Input Voltage (V_{in})	50 V
Inductors (L_1, L_2 & L_3)	3 mH
Capacitors (C_1 & C_2)	330 µF
Capacitors (C_3, C_4, C_5, C_6 & C_0)	100 µF
Load Resistance (R_L)	500 Ω

The simulation model of proposed QZS dc-dc converter is done at various duty cycles (D) to analyze the voltage gain and the limitations of duty cycle for the converter.

The simulation model of the proposed Quasi Z-Source based DC-DC converter shown in Fig. 4.1 is done at D = 0.20 and the output voltage obtained at the load is shown in Fig. 5.1.

As shown in the result of Fig. 6, the output voltage achieved against the input voltage of 50 Volts is around 170 Volts. The voltage gain for a duty cycle of 0.20 should fall around the similar range as found in the simulation results. The voltage gain achieved with the proposed converter is 3.4

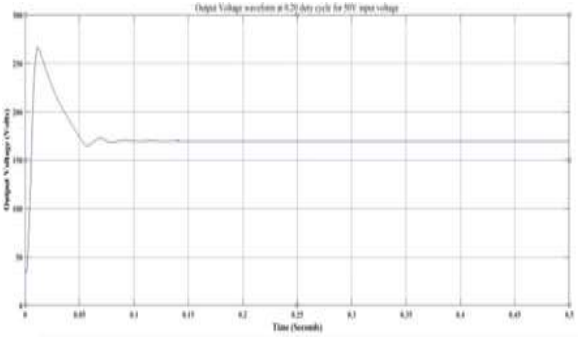

Fig. 6 Output voltage of the proposed QZS dc-dc converter with dc voltage source at D = 0.20

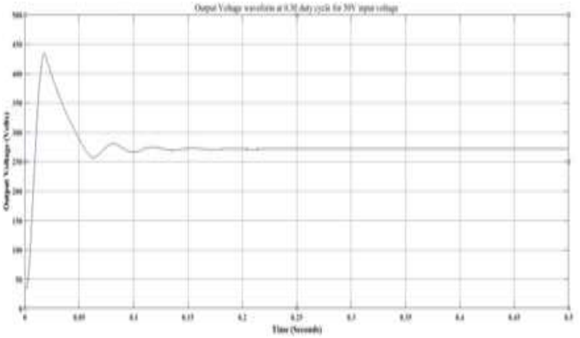

Fig. 7 Output voltage of the proposed QZS dc-dc converter with dc voltage source at D = 0.30

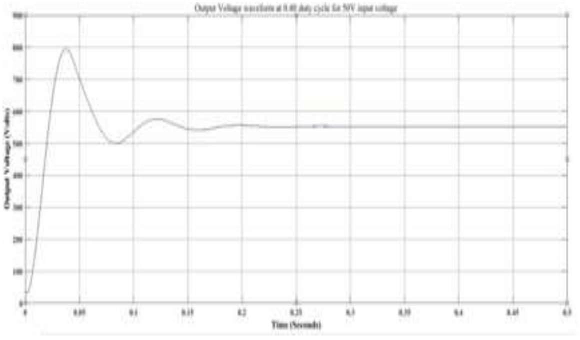

Fig. 8 Output voltage of the proposed QZS dc-dc converter with dc voltage source at D = 0.40

The output voltage achieved against the input voltage of 50 Volts is around 272 Volts. The voltage gain achieved with the proposed converter is 5.5 for D=0.30 as shown in fig. 7.

For D=0.40, the output voltage achieved against the input voltage of 50 Volts is around 552 Volts. The voltage gain achieved with the proposed converter is in around 11.1 as shown in fig. 8.

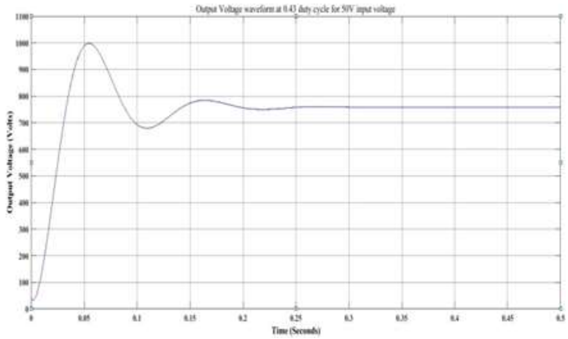

Fig. 9 Output voltage of the proposed QZS dc-dc converter with dc voltage source at D = 0.43

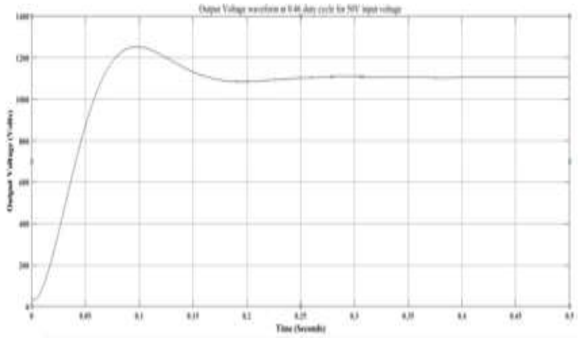

Fig. 10 Output voltage of the proposed QZS dc-dc converter with dc voltage source at D = 0.46

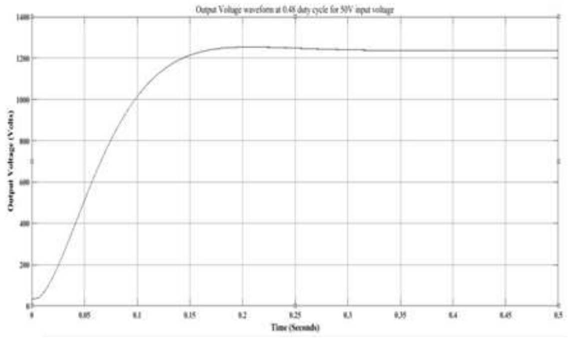

Fig. 11 Output voltage of the proposed QZS dc-dc converter with dc voltage source at D = 0.48

As shown in fig. 9, the output voltage achieved against the input voltage of 50 Volts is around 758 Volts. The voltage gain achieved with the proposed converter is in around 15.2 for D=0.43.

As shown in fig. 10, the output voltage achieved against the input voltage of 50 Volts is around 1105 Volts. The voltage gain for a duty cycle of 0.46 of the proposed converter is in around 22.1 .

The output voltage achieved against the input voltage of 50 Volts is around 1236 Volts as shown in fig. 11. The voltage gain achieved with the proposed converter is in around 24.72 .

VI. RESULTS

The results of simulation for different duty cycles are shown in tabular form as table 3. As it can be seen through the bar graph in fig.12, the converter has its best efficiency response for the duty cycles between 0.30 to 0.46. For very low and very high duty cycles, the power loss increases and the efficiency of the converter decreases.

TABLE 3 SIMULATION RESULTS OF PROPOSED QZS CONVERTER WITH DC SOURCE

Input Voltage	Duty Cycle	Output Voltage	Voltage Gain
50 V	0.20	170.0 V	3.40
	0.30	271.6 V	5.43
	0.40	551.9 V	11.04
	0.43	758.0 V	15.16
	0.46	1105.0 V	22.10
	0.48	1236.0 V	24.72

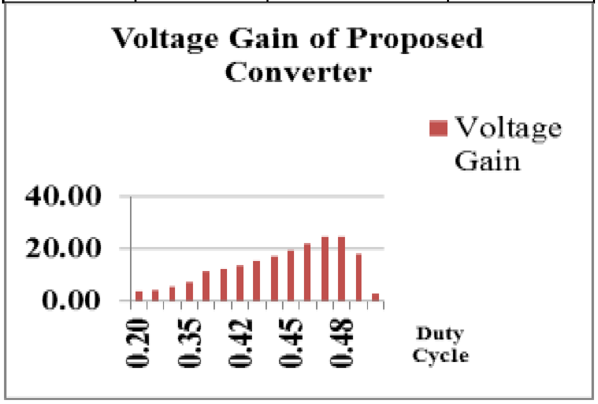

Fig. 12 Bar Chart of voltage gain of proposed QZS converter with respect to the duty cycle

VII. CONCLUSION

An improved QZS based DC-DC boost converter with high voltage gain was proposed. The proposed converter can resolve the issue of low voltage gain of the SLQZS based converter. It performs the above mentioned action without increasing the voltage stress on switching devices and the diodes. The proposed converter provided a wide range of duty cycle up to the maximum value of 0.5. It is also possible for the proposed converter to multiply its voltage gain with multiple stages of the proposed structure and it also noticed that the voltage stress on switches and diodes remains unchanged even after using multiple stages of the proposed converter.

The study also presented a comparison of proposed QZS based dc-dc converter and other topologies of QZS based converters. Keeping in view the results obtained through the comparison the superiority of the proposed converter is also confirmed in terms of voltage gain, duty cycle limitation, voltage stress and consequently reliability and efficiency. The voltage gain of the proposed converter decreases for very low and very high duty cycles, which this issue is expected for all step up converters.

Owing to the confirmed benefits of the proposed converter such continuous input current, high voltage gain and low voltage stress it can be an appropriate option for variety of applications of low voltage output generations such as Photovoltaic system and fuel cells.

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