PI-SRF Based Effective Control for DSTATCOM to Mitigate Various Power Quality Issues in 3P3W Distribution Network

Arshi Zeba Mansoori[1], Mrs. Monica Vardia[2]
[1]M.tech Scholar GITS, Udaipur, Rajasthan INDIA
[2]Associate Prof., Department of Electrical Engineering, GITS, Udaipur, Rajasthan, INDIA

Abstract- **This paper presents an propagation integral synchronous reference frame (PI-SRF) based effective control for DSTATCOM to mitigate various power quality issues in 3P3W distribution network. The proposed SRF based control found to be effective in maintaining DC-link voltage to its reference and estimate fundamental weight components of load currents for generating reference current. These reference currents are compared using actual source currents through hysteresis current controller (HCC) and generate six controllable gate signals. These controllable gate signal further utilized by DSTATCOM to enhance the power quality in distribution network. The proposed PI-SRF based effective control is capable to regulating the voltage, harmonics elimination, and balancing the loads for wide variety of loads at the PCC of 3P3W distribution network.**

Index Terms- DSTATCOM, power quality, PI-SRF, ripple filter, hysteresis current controller.

I. INTRODUCTION

The researchers belonging from generation transmission and distribution (GTD) system are emphasized on power quality (PQ). This quality of electric power has become a significant concern and mitigate as per the standards in distribution network [1]. Maintaining power quality with proliferation of non-linear and unbalanced loads in the 3P3W (Three phase three wire) distribution network is a main issue. Meanwhile, sudden change of the loads, switching, and faults are the main factors of poor power quality [2, 3]. Thus there is a strong need to examine the effect and nature of the wide variety of loads connected to the three phase three wire (3P3W) distribution network and maintains PQ at desired level as per the IEEE standards [4].

Solid state power electronics devices proposed by Hingorani and named custom power devices (CPDs). These devices are the most promising solution to enhanced power quality in 3P3W distribution network. As per the literature distribution static compensator (DSTATCOM) is found effective shunt connected CPDs to mitigate various PQ issues such as harmonics alleviation, compensation of reactive power, voltage regulation and poor power factor (PF) correction [5, 6] under non-linear load [7] in the distribution network. Moreover to improve the performance of this shunt connected device need a novel and effective control algorithm. Literature reported various control algorithm for the driving of DSTATCOM to improve PQ, include, instantaneous reactive power control (IRP) control [8], adaptive-lattice (ALSRF-PLL) [9], adaptive SRF-PLL control [10], PAC-SRF control [11], adaline based control [12], synchronous reference frame (SRF) with battery energy storage system is referring in [13] and fuzzy logic based SRF in weak AC grid system has been discuses in [14].

The aim of this research work is to design and implementation of PI-SRF based effective control for DSTATCOM to mitigate various power quality issues of 3P3W distribution network with the integration of wide variety of non-linear loads.

The paper is structured as follows: Test system under consideration in section II. In section III, control philosophy for DSTATCOM is presented. Simulation and results explained in section V. Concluding remarks in section V.

II.TEST SYSTEM UNDER CONSIDERATION

A three-phase AC grid connected to DSTATCOM integrated at point of interconnection supplying a non-linear load depicted in Fig. 1. Basic circuit structure of proposed system is depicted in Fig 2. The parameters used for MATLAB simulation are mentioned in the appendix.

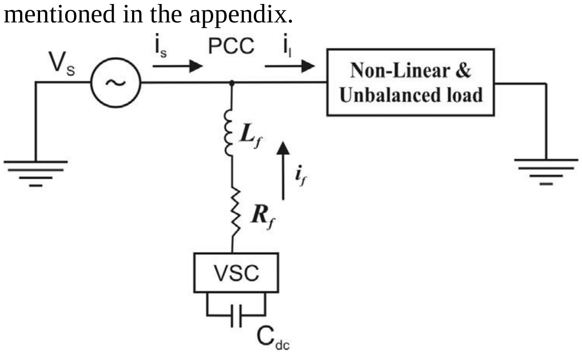

Fig. 1: One-line structure of system under consideration

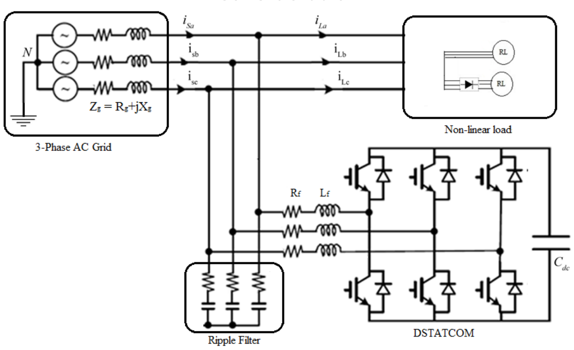

Fig. 2: Circuit structure of DSTATCOM based system.

I. control philosophy

The control philosophy for DSTATCOM has been categorized in two ways.

A. Generation of reference signals

B. Generation of the controlled switching signals with the help of hysteresis current controller (HCC).

The proposed effective control for generating control gate pulses is based on the PI-SRF control. This effective control is basically based on three phase to two phase and two phase to three phase conversion with sine and cosine signal. This signal is generated by phase locked loop (PLL) block. Figure 3 depicted the basic building blocks of PI-SRF [15].

A. Generation of reference signals:

a. Computation of reference source current signals

b. Computation of phase voltage signals

c. Computation of AC and DC bus voltage regulator

a. Computation of Reference Source Currents

The basic procedure include for the computation of reference source currents have an active (in-phase) component and quadrature (out-phase) component. Three phase voltages and currents are converted into α-β-0 axis using the given transformation.

$$\begin{bmatrix} v_0 \\ v_\alpha \\ v_\beta \end{bmatrix} = C = \sqrt{\frac{2}{3}} \begin{pmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} = C = \sqrt{\frac{2}{3}} \begin{pmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad (2)$$

The output of phase locked looped is angle θ and this angle is used to estimate reference direct axis and quadrature axis frame. The conversion from α-β-0 frame to d–q–0 frame is obtained as,

$$\begin{bmatrix} i_0 \\ i_d \\ i_q \end{bmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & \sin\theta \\ 0 & -\sin\theta & \cos\theta \end{pmatrix} \begin{bmatrix} i_0 \\ i_\alpha \\ i_\beta \end{bmatrix} \quad (3)$$

The direct and quadrature axis current components is further estimated as,

$$i_d = i_{d_{dc}} + i_{d_{ac}} \quad (4)$$

$$i_q = i_{q_{dc}} + i_{q_{ac}} \quad (5)$$

The condition for reactive power compensation and unity PF is, source should provide the mean value of the direct-axis load current component with the active power. This condition helps to retain DC link voltage of DSTATCOM. Moreover, PI (proportional–integral) controller is used to regulate the voltage at PCC by minimizing the loss (i_{loss}) component.

$$i_{loss(n)} = i_{loss(n-1)} + K_{pd}\{V_{de(n)} - V_{de(n-1)}\} + K_{id}V_{de(n)} \quad (6)$$

Where, $v_{de(n)} = v^*_{dc} - v_{dc(n)}$ is the error between the reference (v^*_{dc}) and sensed (v_{dc}) dc voltage at the nth sampling instant. K_{pd} and K_{id} are the proportional and the integral gains of the dc bus voltage PI controller. Moreover, the reference source current signal is estimated as,

$$i^*_d = i_{d_dc} + i_{loss} \qquad (7)$$

This obtained signal should be in-phase with the voltage at the PCC. Meanwhile there is no zero-sequence component with this reference source current. Further it is estimated using the reverse transformation.

$$\begin{bmatrix} i^*_0 \\ i^*_\alpha \\ i^*_\beta \end{bmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & -\sin\theta \\ 0 & \sin\theta & \cos\theta \end{pmatrix} \begin{bmatrix} 0 \\ i^*_d \\ 0 \end{bmatrix} \qquad (8)$$

Using reverse transformation for equation 8 of current vector the reference source current in the a–b–c frame is estimated as,

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = C = \sqrt{\frac{2}{3}} \begin{pmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} \begin{bmatrix} i^*_{s0} \\ i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} \qquad (9)$$

a. Computation of Phase Voltages

The line to line voltage at point of common coupling helps to estimate the phase voltages. The output of PI controller i_{qr} is used to regulate voltage at the PCC using previous value of i_{qr}, ac terminal voltage v_{Lt} and reference voltage v^*_{Lt}. Meanwhile using source voltages of phase a, b and c $v_{sa,}\, v_{sb,}, v_{sc,}$ the peak amplitude of ac terminal voltage v_{Lt} at PCC has been estimated.

$$v_{Lt} = \sqrt{\frac{2}{3}\left(V_a^2 + V_b^2 + V_c^2\right)} \qquad (10)$$

$$i_{qr(n)} = i_{qr(n-1)} + K_{pq}\{V_{te(n)} - V_{te(n-1)}\} + K_{iq}V_{te(n)} \qquad (11)$$

Where, $v_{te(n)} = v^*_{Lt} - v_{Lt(n)}$ denotes the error between reference v^*_{Lt} and actual (v_{Lt}) terminal voltage amplitudes at the n^{th} sampling instant. K_{pq} is the proportional gain and K_{iq} is the integral gains of the dc bus voltage of PI controller. The estimation of reference supply quadrature axis current are,

$$i^*_q = i_{q_dc} + i_{qr} \qquad (12)$$

The superscript (*) represents the reference quantity.

$$\begin{bmatrix} i^*_{s0} \\ i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & \cos\theta & -\sin\theta \\ 0 & \sin\theta & \cos\theta \end{pmatrix} \begin{bmatrix} 0 \\ i^*_d \\ i^*_q \end{bmatrix} \qquad (13)$$

The reference source current signal is obtained from Eq. (9).

b. Computation of AC and DC voltage regulator.

AC as well as DC link capacitor voltage is very important to control to retain source current sinusoidal under unbalanced and nonlinear load. We have been developed AC and DC voltage regulator named PI controller. Here in this proposed novel control technique we are using PI controller based SRF control for DSTATCOM.

B. Generation of controlled gate pulses

The HCC is helps to generate the controlled gate pulses. The basic terminology used in HCC is to switch each phase leg to the opposite polarity whenever the sensed current and voltage reaches in between a given boundary level. In this controller reference source current signals ($i^*_{sa}, i^*_{sb}, i^*_{sc}$) are compared with sensed source current signals (i_{sa}, i_{sb}, i_{sc}) in order to generate controlled switching signals for DSTATCOM [16].

II. TEST SYSTEM RESULTS

Proposed power quality mitigation based system is developed using matrix laboratory (MATLAB) and it is analyzed for wide variety of distribution loads. These loads include unbalanced linear load, unbalanced non-linear load. However, load unbalancing is achieved by removing one phase for 0.3 sec to 0.4 sec and 0.6 sec to 0.7 sec time period [15].

A. PI-SRF based Effective Control for DSTATCOM under Unbalanced Linear Load

The obtained MATLAB based results for PI-SRF based effective control for DSTATCOM under unbalanced linear load is analyzed in Fig 4. The proposed system is able to keep the PF unity at grid side. The proposed system has been run in MATLAB 0 sec. to 1 sec.

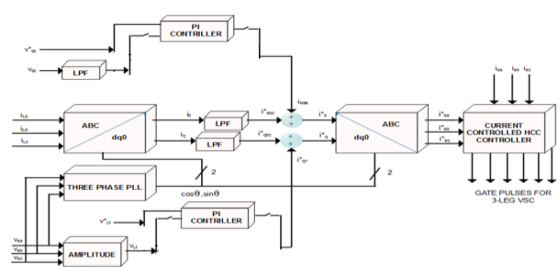

Fig. 3: Control Scheme of PI-SRF algorithm for DSTATCOM.

Under this run time of the system at 0.3 sec to 0.4sec and 0.6sec to 0.7 sec, the 3-phase load is converted to 2-phase load the loads are applied again at 0.4 to 0.6sec and 0.7 sec respectively. The source currents are observed balanced and in-phase with the source voltages at unbalanced linear load condition. The dc link voltage also obtained near to its set reference 680 V value with the terminal voltage of 340 V. This obtained results clearly depicted that the robustness and effectiveness of the control algorithm.

B. PI-SRF based Effective Control for DSTATCOM under Unbalanced N-L Load

The obtained MATLAB based results for PI-SRF based effective control for DSTATCOM under unbalanced non-linear load is analyzed in Fig 5. The proposed system has been run in MATLAB 0 sec. to 1 sec. Under this run time of the system at 0.3 sec to 0.4sec and 0.6 sec to 0.7 sec, the 3-phase load is converted to 2-phase load the loads are applied again at 0.4 to 0.6 sec and 0.7 sec respectively. The source currents are observed balanced and in-phase with the source voltages at unbalanced linear load condition. The dc link voltage also obtained near to its set reference 680 V value with the terminal voltage of 340 V. Thus, the proposed system is keep PF unity at grid side and voltage regulation is achieved. Meanwhile, at 0.3 to 0.4 sec and 0.6 sec to 0.7 sec. the essential compensating current signal is provided by the DSTATCOM and maintained level of harmonics at source side as well as PCC side. This obtained results clearly depicted that the effectiveness of the control algorithm.

Frequency spectrum (harmonics) of source current, source voltage, compensating current and compensating voltage are clearly shows that the THD values are under the international IEEE-519 standards.

We have been also mitigated the all even harmonics including 3rd , 9th and 15th and so on, odd harmonic, which is very harmful for distribution sensitive loads like computer, TV, microprocessor based equipment, etc.

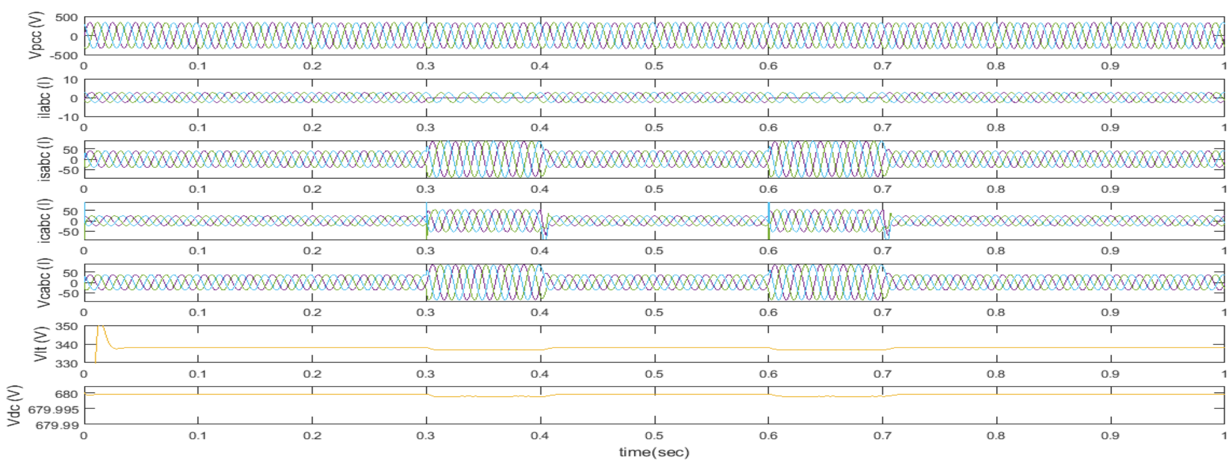

Fig. 4 Analysis of PI-SRF based effective control for DSTATCOM under unbalanced linear load

TABLE I ANALYSIS OF PI-SRF EFFECTIVE CONTROL FOR DSTATCOM BASED PROPOSED SYSTEM

Signals	THD in source current (%)			
	Linear load case study		N-L load case study	
	Without PI-SRF based DSATCOM	With PI-SRF based DSATCOM	Without PI-SRF based DSATCOM	With PI-SRF based DSATCOM
Source current	9.09	0.01	29.59	3.67
Source voltage	8.94	0.11	25.47	0.19
Compensating current	-	0.01	-	0.06
Compensating voltage	-	0.09	-	2.65
DC link voltage	Fluctuated	~ 680 V	Fluctuated	~ 680 V
AC terminal voltage	Fluctuated	~ 342 V	Fluctuated	~ 342 V
Power factor	Fluctuated	Unity	Fluctuated	Unity
3rd 7th and 15th harmonics with odd harmonics	Completely eliminated			

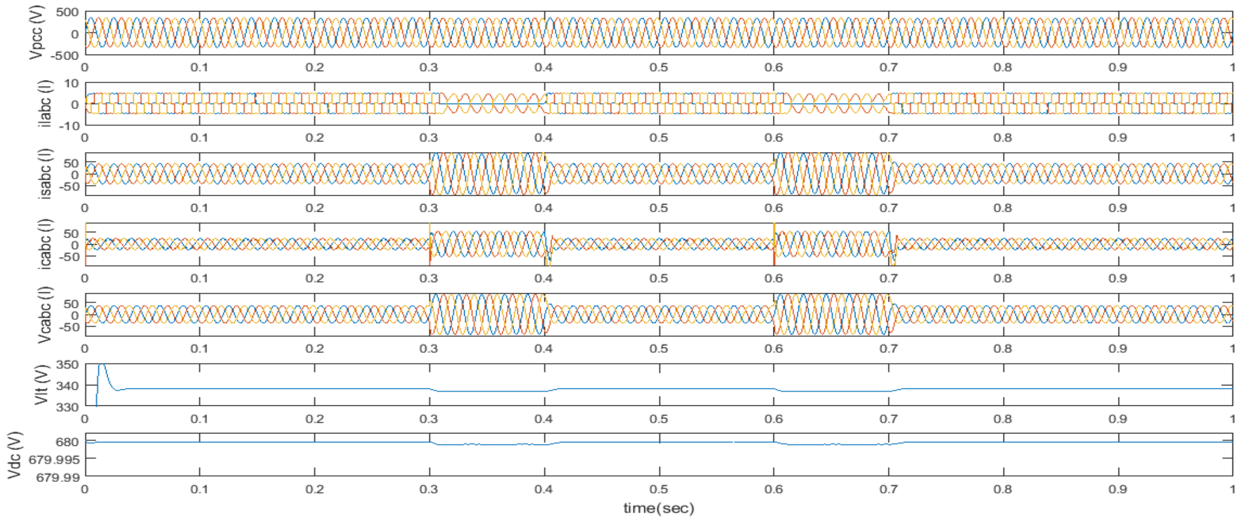

Fig. 5 Analysis of PI-SRF based effective control for DSTATCOM under unbalanced N-L load

V.CONCLUSION

The obtained results using PI-SRF based effective control for DSTATCOM under unbalanced linear load and unbalanced non-linear load is analyzed and found to mitigate various power quality issues in 3P3W distribution network. The proposed PI-SRF effective control is implemented successfully. It has been obtained that the harmonics elimination, voltage regulation and load balancing is succeeded under the international IEEE standards 519-1992.

APPENDIX

System parameters:

3-Phase AC grid voltage (L-L) = 415V, frequency (f) = 50 Hz, VA = 2MVA, Current band of HCC = 0.1, Interfacing resistor Rf = 0.01Ω, interfacing inductor Lf = 2e-3 H , ripple filter resistor = 5Ω, ripple filter capacitor = 5e-6 H, dc link capacitor = 5000 F, Sampling frequency = 10KHZ, Linear load 2000 kVA, N-L load=3-phase diode bridge rectifier with R = 50Ω, L = 100mH,

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