

Review on Error Detection and Correction Capability for BCH Code and Reed-Solomon Code

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Abstract- The BCH code is the essential class of multiple-error-correcting linear cyclic code. In actually, Bose-Chaudhuri-Hocqunghem code is an abstraction of the cyclic hamming code for multiple-error correction. The finding of errors made by noise during transmission from the sender to the recipient is called as Error Detection. The finding of errors and renewal of the original data is called as Error Correction. In this review paper shows that the studies about fixed block length and message length of the BCH code and Reed-Solomon code. In addition, the various techniques for decoding the codes are studied.

Index Terms- BCH (Bose-Chaudhuri-Hocqunghem) code; BCH Encoder; BCH Decoder; VHDL; Error Correction; BER (Bit Error Rate)

I. INTRODUCTION

Nowadays, the fastest growing area in the field of communication is Wireless Communication. Whenever the communication takes place, the data need to be transmitted through the sender to the recipient. The error is such a situation in which output information is not similar to the input information. When digital signals are transmitted from the sender to the recipient, some errors can introduce in the signals because of noise interference. That means a 0 bit may change to 1 or vice versa [16]. The significant data will be lost because of the data error.

In a communication system, detecting the error during the transmission process of data through the sender to the recipient is called error detection. For the detection of error, we can use some redundancy codes. These redundancy codes are then added to the data during transmission, such codes are termed as "Error detecting codes" [17].

Error Correction Code is a procedure of put in parity bits into real data in order to recover the message by

the receiver. We need error correcting code for good conveying message over a noisy way that has an improper BER as well as SNR is lower. Reed-Solomon codes, Golay codes, Cyclic Hamming code, BCH codes, Goppa codes are used in error correction code [5]. The computational complexity of Reed-Solomon encoder and decoder is high, but the complexity of BCH code is low.

II. BASICS OF BCH CODE

The BCH code is the essential part of the multiple - error-correcting linear cyclic code. In 1959, A. Hocqunghem and in 1960, R. C. Bose and D. K. Ray-Chaudhuri invented Binary codes which are called as BCH code. An accurate control above the multiple symbol errors correctable in the code is a central feature of Bose-Chaudhuri-Hocqunghem code. Especially, multiple bit errors can be corrected by designing binary Bose-Chaudhuri-Hocqunghem codes [18]. BCH code depends on Galois field arithmetic which includes describing the binary actions over finite collections of an element [5].

Bose-Chaudhuri-Hocqunghem code is the subclass of cyclic codes. In order to give good error correction capability, we have to specify the roots of the generator polynomials. BCH code can identify and overcome the error up to 't' arbitrary errors per code words because every BCH code has 't' error correcting code. BCH code has following factors:

Block length: $n=2^m-1$

Number of message bits: $k \geq n-mt$

Minimum distance: $d_{\min} \geq 2t+1$

Here 'n' is the block length and 'k' is the message length. The above factor can correct the 't' errors or fewer error. The generator polynomial of this code is identified in respect of its roots from the Galois field GF (2^m) [11].

A. Encoding of BCH Code

BCH code is a subset of cyclic code, the organized method of encoding is related to the method of binary coding. For the BCH code, the generating polynomial is:

$$g(X) = g_0 + g_1X + g_2X^2 + \dots + g_{2t-1}X^{2t-1} + X^{2t}$$

The number of parity bits is equivalent to the degree of generator polynomial. Since the degree $2t$ is equal to the generator polynomial, there must be a precisely $2t$ successive powers of α that is the roots of the polynomial. Message polynomial $m(x)$ can be transferred into the leftmost $n-k$ stages of a code word register and then tacking on a parity polynomial $p(x)$ [5].

B. Decoding of BCH Code

There are many algorithms for decoding BCH codes. The most common follow this general outline:

1. Calculate the syndromes for the received vector
2. Determine the number of errors and the error locator polynomial from the syndromes
3. Calculate the roots of the error location polynomial to find the error locations.
4. Calculate the error values at those error locations
5. Correct the errors

During some of these steps, the decoding algorithm may determine that the received vector has too many errors and cannot be corrected [18].

III. LITERATURE REVIEW

The author in [7] used BPSK and QAM modulation scheme for encrypting and decrypting of the RS code and BCH code by the Rayleigh fading channel. Here, numbers of iteration were performed to get the result of BCH code and RS code. The ratio of E_b/N_0 was changed from 1 to 10. It was noticed that the BCH code was performed better than the Reed-Solomon code [7].

In [6] and [8] paper authors proposed method designed the BCH encoder on FPGA for (15, k) using AWGN channel with numerous error correcting code. Considered (15, 11, 1), (15, 7, 2), and (15, 5, 3) BCH encoder for error correction according to the highest degree of a polynomial. Here encoder of (15, 5, 3) was more beneficial than the remaining, because of the necessity of speed. When the noise corrupted the

original data, the BCH encoder was corrected 3 errors at the receiver side [6], [8].

Saeideh Nabipour, Javad Javidan, Gholamreza Zare Fatin [5] proposed a method using the Berlekamp-Rumsey-Solomon algorithm through the Chien-search process, to get the roots of error locator polynomial for BCH decoder. The new algorithm was implemented in C++ programming language to show the performance. The algorithm was improved to 1.5 times faster than the Chien search method [5].

In [9] the author has performed (63, 51, 2) BCH encoder and decoder to find out the application in IEEE 802.15.6 WBAN. The 51 message bits were encoded and any 2-bit error was spotted and modified from the 63-bit code word. For that encoder used LFSR and decoder used Berlekamp algorithm and Chien Search algorithm. The design implemented in FPGA and synthesis was done effectively by Xilinx ISE 14.2 [9].

Sahana C*, V Anandi [2] presented a binary encoding of (255, 215, 5) for the simulation of encoder also Syndrome computation. The message bits of 215 were encrypted and any 5-bit error was detected from the 255-bit code word. LFSR was used for the encoder process and Finite field polynomial multiplication was used for the calculation of syndrome [2].

In [3] the author studied the encoding and decoding process of RS code and the error probability for Reed-Solomon code. For large block length, the error probability of the RS code showed that the BER operation was improved and for lower SNR, BER performance was poor [3].

Samir Jasim Mohammed [10] designed and simulated BCH encoder codes of (31, 26, 1), (31, 21, 2), (31, 16, 3), (31, 11, 5) and (31, 6, 7) utilizing Xilinx-ISE 10.1 and enforced in FPGA. Here, a 31-bit size code word was used in this implementation. The (31, k) BCH encoder was properly examined and compared. The BCH encoder code (31, 6) occupied a greater area than the other codes. The results showed the system works well [10].

In [11] at the time of corrupting the actual data, binary BCH code (15, 11, 3) and (63, 39, 4) were corrected 3-bit error and 4 error on the output side respectively. Here, iterative algorithm was used to identify the location of the error. Due to this, the speed and utilization of the device were improved [11].

In [12] author has designed a (15, 7) BCH encoder and decoder. By utilizing algorithms, two errors have been acknowledged and adjusted in the BCH code which is worked at the single cycle. The result showed the area and delay were reduced [12].

The author in [1] proposed a new method for compressing the LUT and reduces the requirement that was compared to prior design. The throughput of the decoder was greater and the area has been reduced by 19% for (1023, 993) BCH code over $GF(2^{10})$ [1].

Dejan Azinović, Klaus Tittelbach-Helmrich and Zoran Stamenković [13], introduced the mathematical background of BCH encoding and decoding process in software and hardware implementation. Implementation cost and the performance of the system were calculated for various parameters of the code. The main focus is on the 255 code lengths and the investigation of the different implementation code was corrected [13].

In [14], the author designed Reed-Solomon encoder and the decoder of $n=23$ and $k=19$. The finite field $GF(2^5)$ has been represented to this RS code and had to correct the capability up to 2 short burst error as well as detecting 4 errors capability. This process was simulated in Xilinx 14.1 [14].

Sweta Thakur, Tabassum Nasrat and Soumyasree Bera [15] studied the performance of two channel coding techniques, i.e., BCH and Reed Solomon. Using MATLAB software the process of simulation has been done. Here, compared the BER and SNR value of the BCH and Reed Solomon code, also compared the uncoded and coded transmission. The result was similar in both software and hardware [15].

IV. PROBLEM FORMULATION AND PROPOSED WORK

In the existing work, BCH and Reed-Solomon encoder and decoder has been developed. In the current work fixed block length and message length code are decoded as well as the fixed error correcting capability (t) are calculated. This result showed the improvement in speed and utilization of the device. Also, the channel coding techniques and encoding and decoding process are studied.

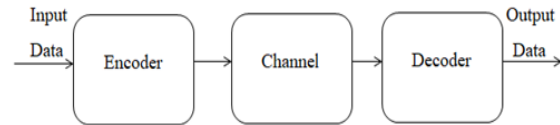


Fig. 1: Block Diagram of the BCH Code

The proposed work is to implement the variable length BCH encoder and decoder using VHDL. At the sender side, the data streams are encrypted by adding some additional bits with message bits called as parity bits. The message bits composed with parity bits named as a 'Code word'. At the receiver end, a code word is checked for any error in the receiver side and then the corrupted bits are corrected. This is called a decoding process. After correcting the errors in received data, the original message is regained. We will design a variable length system. In which we will decode the codes for any block length and message length. Due to this, we may improve the throughput of the system.

V. CONCLUSION

This work introduced the review of BCH and Reed-Solomon encoder and decoder. Here, we have mentioned the various block length and message length of the BCH Code and Reed-Solomon Code which is fixed in all. Also, we have shown the various techniques used to calculate errors.

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