Area Efficient Ripple Carry Adder Using 22nm Strained Silicon CMOS Technology

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Abstract **- In this research proposal, the existing ripple carry adder (RCA) is analysed to find the possibilities for area minimization. Based on the analysis, the full adder is further modified with OAI circuit and AOI circuit and the corresponding design of RCA are proposed for the BTA. The RCA is designed for m bits (m=8,16,32 bits) has reduced in transistors count than the existing RCA. Using this RCA design, the multi-operand adder (n=8) BTA structure is proposed. The RCA and Binary tree structure is synthesised at 22nm CMOS technology. Result reveals that the proposed RCA and BTA-MOA provides the efficient results in area minimization compared to previous structure, suitable for multipliers and other applications. Therefore, this modified ripple carry adder based binary tree adder can be a better choice to develop the efficient digital systems for signal and image processing applications.**

Index Terms **- Ripple Carry Adder, AOI Gates, OAI Gates, Binary tree adder.**

1.INTRODUCTION

Multi-operand adders are critical for mathematics layout blocks in particular withinside the summation of partial results of hardware multipliers. Multi-operand adders are required for constructing multipliers in which more than one partial product results ought to be brought as much as have the multiplication result. Since maximum of the electricity is fed on the mathematics blocks, in particular at multipliers, lower power circuit designing with decreased switching noise is desirable [3].

The operands taken into consideration for addition may be single bit or of more than one bit, for that reason the input and output of the adder may be in more than one bits [4]. Multi-operand adder may be represented easy through an structure comprising of a compressor tree, which reduces the partial sum and propagated carry [4]. There are various sorts MOA however the adders used in multipliers are Array tree adder, Wallace tree adder, Balanced delay tree adder and Overturned-stairs tree adder. For any arithmetic functioning unit, adders are the maximum critical additives due to its useful resource consumption. Adders additionally form part of multipliers that's every other useful resource extensive aspect of mathematics circuits [4]. The most effective MOA is a binary tree adder (BTA), designed through connecting two-operand adders in binary tree configuration for the addition of more than one operand [5]. There are various forms of adders consisting of ripple bring adder (RCA), carry-look-ahead adder (CLA), parallel prefix adder (PPA), which may be used to increase the BTA design, in which every adder has its very own tradeoffs between area consumption.

Among all adders, RCA has much less area and power with better delay, while different adders (speedy adders) having much less delay with better area and power. On the alternative side, area and power are the primary constraints in maximum of the structures which call for the addition of a huge wide variety of operands. The Binary tree adder used in those structures have to be area and power efficient.

2.LITERATURE SURVEY

Multiple operands summation, that is extensively utilized in block designs and rapid functions. The review is carried out in unique angles for consciousness of noticeably efficient multi-operand addition for clinical IoT subject devices. The traditional adders used withinside the multipliers and filters for summation of the intermediate outcomes has a tendency to area and delay occurrence. Multi-operand addition and compressor trees may be used greater correctly for decimal operations, that allows you to lessen the delay without a lot overhead in area [1]. For enhancement of area consumption, delay and

power, unique multiplication strategies including upload and shift technique and Wallace tree (WT) multiplier are used for the multiplication [6].

However, the adder systems counselled for CLA and PPA [7-14] are efficient in concept of delay however they occupy a huge area and devour greater power, while the design recommended for RCA in [15,16] includes much less area and power with better put off. Therefore, the carry selects scheme-primarily based totally adder [17] has been counselled to acquire the overall performance among RCA and CLA. Plus, Carry Select Adder is perhaps the quickest adders applied in several statistics processing. It is obvious that there's extension for lessening the area and energy usage withinside the CSLA [18,19].

To appreciably lessen the area and energy of the CSLA, the layout makes use of a easy gate-stage alteration. 8, 16, 32, and sixty-four bits square-root CSLA (SQRT CSLA) structure relying on modifications were evolved and in comparison, with the everyday SQRT CSLA structure. In [20], binary to the excess-1 converter- primarily based totally good judgment layout technique is recommended for the implementation of CSLA to lessen the area and energy.

Besides, the Australian computer scientist Chris Wallace has evolved some other sort of green MOA referred to as Wallace tree adder (WTA) [15]. In this Wallace tree adder, operands might be decreased to 2 phrases with the aid of using the usage of the carry-save adders and eventually those phrases are delivered collectively with the aid of using some other -operand adder to compute the end result of addition [15]. The carry-save adder is designed the usage of complete adders (FAs) and it introduces simplest one FA put off. BTA is greater famous than Wallace tree adder and utilized in numerous packages because of its easy and regular structure however it's put off is a chief concern.

3.EXISTING WORK

The existing RCA relies on new logic formulation; however, the AOI/OAI gate's inputs depend upon X-OR circuit, previous full adder carry, and conjointly the AND gate output. In this existing work the area and delay of OAI/AOI gates depends on all attainable inputs to AOI/OAI gate. And for comparison it's projected at numerous bit widths (m=8,16,32bits). This ripple carry adder is employed for binary tree structure for adding multiple operands, as (N=number of operands, N=8,16,32) with every quantity of sixteen bits.

The Multi operand structure designed is RCA- based BTA, where the adder structure's area unit synthesised in Synopsys design Compiler 22 H-spice simulation code at 22 nm CMOS technology. input supply voltage used is 0.8v as construct of power consumption for low power circuits. This Ripple carry adder structure is economical style in terms of area, delay and energy than the other RCA structures.

3.1EXISTING RIPPLE CARRY ADDER

The Full adder designed with AOI/OAI circuit, is used for the RCA design. The fig.1 is block diagram of 4-bit Ripple carry adder, similarly m-bit RCA is designed (m=8,16,32 bits) and their area and delay is calculated.

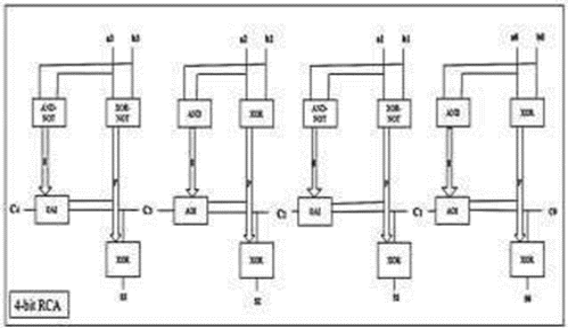


Fig .1 Four Bit RCA

The inputs are given at the same time and every adder produces carry, the delay of every full adder is calculated by the subsequent general expression,

TRCA = (m/2) TAOI-FA +(m/2) TOAI-FA (1)

The ripple carry adder delay is vital since it is used for binary tree adder. The area is calculated by subsequent general expression,

ARCA = (m/ 2) AAOI − FA +(m /2) AOAI − FA(2)

Where m-represents the no. of bits, A is the area of that specific gate.

4.PROPOSED WORK

The proposed Ripple carry adder design is concentrated on area minimization. For miniature circuits the area consumption depends on numbers of transistors used etc., the existing ripple carry adder design is modified by replacing the 2-1 AOI circuit by 2-2 AOI circuit in full adder structure.

4.1REDESIGNED FULL ADDERS

In the previous design, carry side AOI circuit includes only ONE AND, OR, NOT gates. These gates together

in CMOS consists of 6 transistors. The AND gates in CMOS consists of 6 gates. Thus, in Carry part of full adder the total numbers gates of AND & 2-1 AOI circuit is 12 transistors. Where the 2-2 AOI design consists of ((AND- AND)-OR-NOT), the total number of transistors reduced to 8 transistors

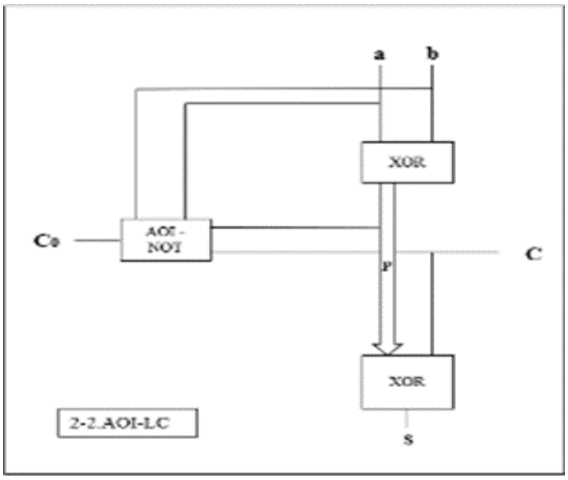


Fig 2. (2-2)AOI -Full Adder

The above fig. 2 is block diagram of 2-2AOI Full adder circuits, where the AOI-NOT block performs one or more AND operations followed by an OR operation then an inversion and NOT to invert the output

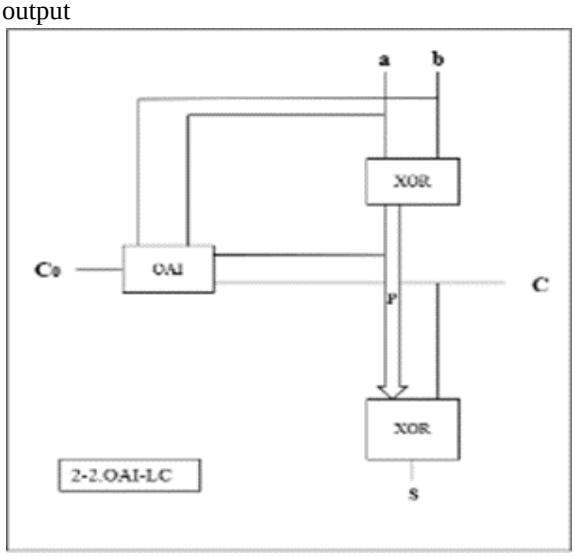


Fig 3. (2-2)OAI -Full Adder

In the previous OAI full adder design , the 2-1 OAI circuit was used. The fig 3. Shows the 2-2 OAI full adder block diagram. In previous version the outputs of XOR gate, AND gates are inverted for OAI circuits. But in this design no need of such inversions, where the output of AOI full adder is inverted.

4.2MODIFIED RIPPLE CARRY ADDER

The above proposed full adders are used for design of efficient ripple carry adder. The RCA is coded form bits (m=8,16,32 bits) , since for the area comparison with existing design work. The fig 4.is the block diagram for m=4 bits, similarly it is designed for m bits.

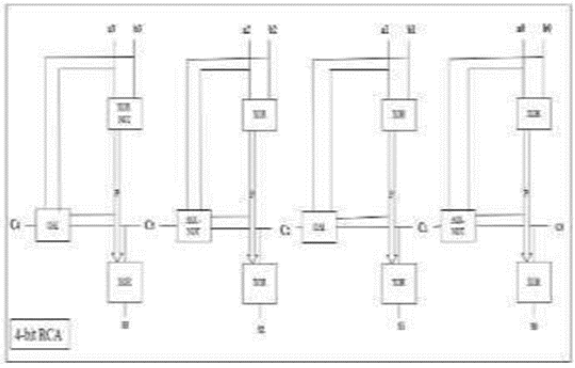


Fig 4. Modified Ripple Carry Adder

This ripple carry adder designed is used to rebuild binary tree adder (BTA), Binary tree adder is used in numerous applications. The Binary tree adder is designed using multiple operands as (a,b,aa,ab,ba,bb etc.,) ,the Multiple operand adder is defined by N-bits where the N refers to number of operands. Binary tree adder is designed for (N=8 Operands) every operand is of 16-bits.

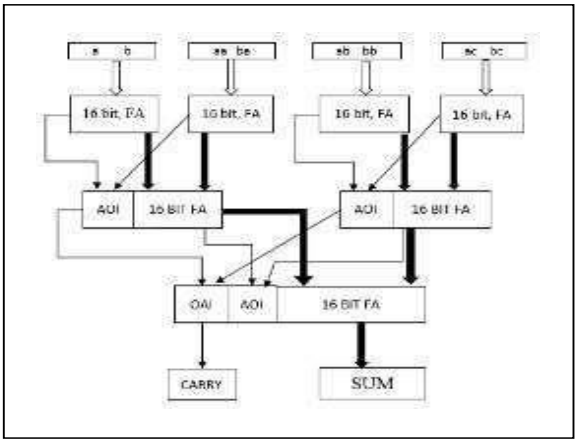


Fig 5. Modified Rca Based Binary Tree Adder For Multi Operand Adder

5.SYNTHESIS RESULTS

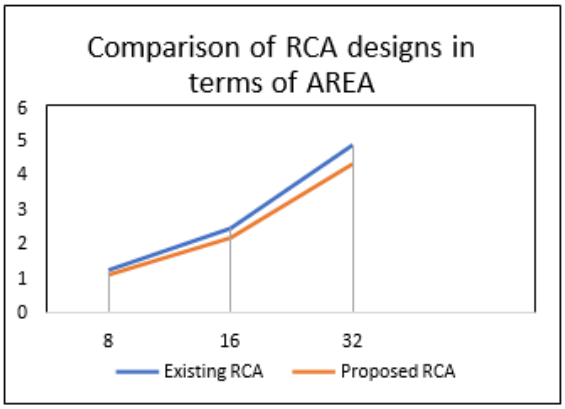
The simulation of circuits is done using H-Spice simulation software, the result analysis shows circuits works efficiently. The below table .1 gives the comparison for each bit of Ripple carry adder in terms

of area consumption. The results are calculated in units of micro-square meter.

Table .1 Comparison of RCA design

Adder design	Bit width(m)	Existing RCA Area, μm^2	Proposed RCA Area μm^2
RCA	8	1.211	1.074
	16	2.423	2.148
	32	4.846	4.297

Based on the comparison results the graph is plotted for inference as shown in graph 1.it can be observed that the proposed design is more efficient design than previous structure in terms of area.



Graph 1. Graph based on comparison of RCA design

The area of the Binary tree based multi operand adder is also calculated. The values defined in table .2 are area converted from nano scale to microscale values.

Table .2 comparison of RCA -BTA Design

Adder design	Bit width(N)	Existing Area, μm^2	Proposed area, μm^2
Binary tree adder	8	27.24	24.16

6.CONCLUSION

The RCA- BTA is widely used in Multi operand adders due to its simple regular structure that leads to area and energy efficient circuit design. But, work for designing miniature and efficient circuits keeps in search for redesigning and upgradements. Therefore, the area analysis of RCA-based BTA is presented in this paper. Based on the comparison on this work, the modification of full adder for RCA shows better results in area reduction and correspondingly the RCA design can be used for higher orders of multi operand adders.

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