Design of Asynchronous SAR ADC of 10-bit with EA-based bandgap reference voltage generator using bootstrap switch & two stage dynamic comparator

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***Abstract*--The proposed prototype of a 10-bit asynchronous Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) with an EA-based bandgap reference voltage generator is designed to optimize power consumption, static, and dynamic performance. Several techniques are proposed to achieve these objectives. One of the proposed techniques is the dual-path bootstrap switch, which aims to increase the linearity of sampling. The Voltage Common Mode (VCM)-based Capacitive Digital-to-Analog Converter (CDAC) switching technique is also implemented for the CDAC part to alleviate the switching energy problem of the capacitive DAC. This helps to reduce power consumption while maintaining dynamic performance. The proposed architecture of the two-stage dynamic latch comparator is another technique to achieve high speed and low power consumption. This helps to reduce the time required for bit conversion, which is important for practical applications. To achieve faster bit conversion with an efficient time sequence, asynchronous SAR logic with an internally generated clock is implemented, which avoids the requirement of a high-frequency external clock. All conversions are carried out in a single clock cycle, making the ADC more efficient. Finally, the proposed error amplifier-based bandgap reference voltage generator provides a stable reference voltage to the ADC, which is essential for accurate conversion. The EA-based bandgap reference voltage generator helps to improve the static performance of the ADC.**

***Index Terms*: Asynchronous SAR logic and comparator clock generator; bandgap reference voltage generator; two-stage dynamic comparator; low power consumption.**

I. INTRODUCTION

ANALOG TO DIGITAL CONVERSION

Digital Signal: A digital signal is a signal that represents data as a sequence of discrete values; at any given time it can only take on one of a finite number of values.

Analog Signal: An analog signal is any continuous signal for which the time varying feature of the signal is a representation of some other time varying quantity i.e., analogous to another time varying signal.

The ADC is a broadly used mixed signal electronic device that converts an input analog electrical signal (commonly a voltage) to a digital (binary) word as shown in Figure 1.1. The ADC had an analog reference voltage or current to which the input analog signal was compared. The digital output words expressed the fraction of reference current or voltage relevant to that of the input signal.

The ADC performed the conversion periodically that is by taking samples of the input instead of performing continuous conversion. Therefore, there was a requisition of defining the rate at which new digital values were sampled from the input analog signal. The rate of new digital values was called as sampling frequency or sampling rate of the converter. For the faithful reproduction of original signal, the sampling rate should be higher than twice the amount of highest frequency of the input signal which was stated as Shannon – Nyquist sampling theorem. The conversion also included the quantization of input to obtain the digital signal.

The following techniques can be used for Analog to Digital Conversion:

- Successive Approximation Register ADC
- Integrating or Dual Slope ADC
- Flash ADC
- Pipelined ADC
- Delta Encoded ADC
- Sigma Delta ADC

SAR ADC evaluated each bit at a time from most

significant bit to least significant bit through all possible quantization levels. The comparator was used in this ADC to compare the input signal with the reference signal obtained from the DAC. SAR logic was used to obtain the digit bits as output of the ADC which was also input of the DAC. The Successive Approximation Register ADC is One of the most common analog-to-digital converters used in applications requiring a sampling rate under 10 MSPS is the Successive Approximation Register ADC. This ADC is ideal for applications requiring a resolution between 8-16 bits. For more information on resolution and sampling rates, please refer to the first in this series of articles: Deciphering Resolution and Sampling Rate. The SAR ADC is one of the most intuitive analog-to-digital converters to understand and once we know how this type of ADC works, it becomes apparent where its strengths and weaknesses lie.

II.SAR ADC IMPLEMENTATION

The basic successive approximation register analog-to-digital converter is shown in the schematic below:

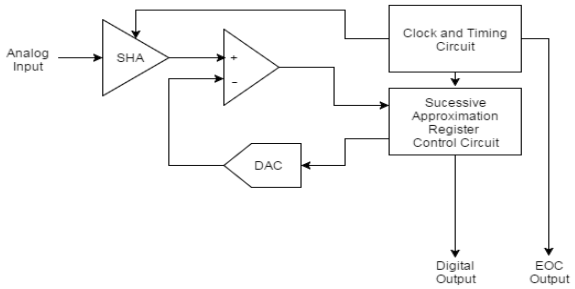


Figure 1: SAR ADC Operation

The SAR ADC does the following things for each sample

The analog signal is sampled and held.For each bit, the SAR logic outputs a binary code to the DAC that is dependent on the current bit under scrutiny and the previous bits already approximated. The comparator is used to determine the state of the current bit. Once all bits have been approximated, the digital approximation is output at the end of the conversion (EOC).

The SAR operation is best explained as a binary search algorithm. Consider the code shown below. In this code, the current bit under scrutiny is set to 1. The resultant binary code from this is output to the DAC. This is compared to the analog input. If the result of the DAC output subtracted from the analog input is less than 0 the bit under scrutiny is set to 0.

The algorithm that a SAR ADC performs can be understood by examining the waveforms depicted in the figure1.1.

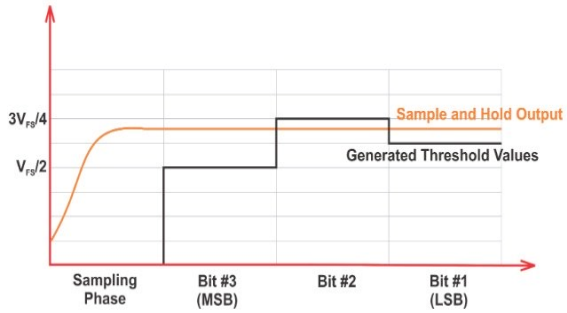


Figure1.1: Operation of 3-bit SAR

The above waveforms illustrate the operation of a three-bit SAR ADC. During the sampling phase, the input value is sampled and held for the entire conversion phase. A SAR structure usually needs one clock cycle to sample the input and one clock cycle to determine every bit of its digital output. Therefore, an N-bit SAR ADC usually needs (N+1) clock cycles to digitize the input analog value. For the three-bit example above, we need a total of four clock cycles.

Switched Capacitor DAC

Using a comparator and an array of binary-weighted capacitors, we can efficiently implement the DAC and comparator blocks of a SAR ADC.

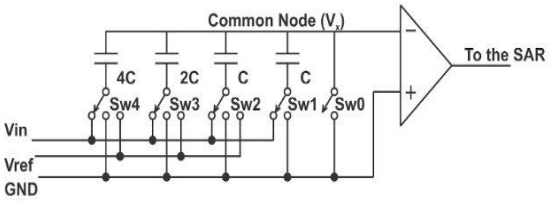


Figure1.2: 3-bit Example.

During the sampling phase, SW0 is closed, and the common terminal of the capacitors (V_x) is connected to ground. In this phase of operation, the other terminal of the capacitors is connected to the analog input (V_{in}). Hence the input signal is sampled onto the parallel combination of all the capacitors in the array.

During the conversion phase, SW0 is open. Assuming that the input impedance of the comparator is infinite, the common node of the capacitor array (V_x) is left floating (it doesn't have a low-impedance path to ground or V_{ref}). Hence, the total charge stored in the

capacitor array will remain constant during the conversion phase. However, while the total charge is constant, connecting the lower plate of the capacitors to either V_{ref} or ground can cause charge redistribution among the capacitors. This charge redistribution will change the voltage that appears at the comparator input. For example, assume that after the sampling phase, the capacitors are connected to ground. In this case, a voltage equal to $-V_{in}$ will appear at the comparator input (because the parallel combination of the capacitors has stored the input value V_{in}). Now, if we connect only the largest capacitor (4C) to V_{ref}, the voltage at the input of the comparator will increase by $\Delta V=Vref4CCtotal=Vref4C8C=Vref2$

In this equation, C_{total} is the sum of all the capacitors in the array (for an n-bit capacitive DAC, we have: $C_{total}=(1+1+2+2^2+...+2^{n-1})C=2^nC$). Using the superposition principle and noting that the initial voltage at the comparator input was $-V_{in}$, the new voltage applied to the comparator will be $Vnew=Vref2-Vin$.

The comparator of Figure 3 compares this value to 0 V. This is equivalent to comparing the input value with the threshold Vref2 (See Figure 1).

The result of this comparison determines the MSB value. The result also determines whether the MSB capacitor (4C) should be connected to V_{ref} (MSB=1) or ground (MSB=0) for the rest of the conversion cycle. For the next significant bit, the corresponding capacitor will be connected to V_{ref}. This will increase the voltage at node V_x by Vref4.

The comparator output at this stage will be used to determine the value of the second most significant bit. It will also determine whether the capacitor (2C) should be connected to V_{ref} or ground during the next conversion cycles. This procedure will continue until all of the bits of the digital output are found.

Integrating or Dual Slope ADC

The dual slope ADC used counters to generate the output digital bits. As per the name, the ADC had two phases where first phase ramped up with a slope proportional to the input voltage for a fixed time period and second ramped down with a different slope proportional to the reference voltage for a varied time period.

Advantages

Very precise.

The sources of errors were only comparison with zero and clock period.

Disadvantages

Low speed.

Needed time to ramp up and down the output voltage which doubled with addition of each bit added to the representation.

For the effective performance we choose SAR ADC.

PERFORMANCE METRICS OF ADCS

The metrics that characterize the performance of ADCs are divided into two groups namely static and dynamic. The static performance metrics of ADCs are Figure of Merit (FOM), Differential Non-Linearity (DNL) and Integral Non-Linearity (INL). The dynamic performance metrics of ADCs are Effective Number of Bits (ENOB), Total Harmonic Distortion (THD), Signal to Noise Ratio (SNR), Signal to Noise and Distortion Ratio (SNDR) and Spurious Free Dynamic Range (SFDR).

Differential Non-Linearity

The difference between an actual step width and ideal value of one LSB is termed as DNL error. The calculated DNL value must be less than 1 LSB.

1LSB = VFSR / 2N

Where VFSR is full scale voltage range

N is bit resolution of the ADC

$$DNL(LSB)=\left|\frac{V_{p+1}-V_p}{V_{ideal}-1}\right| \quad for\, 0<p<2^N-2$$

where Vp is the physical value corresponding to the digital output code

V_{ideal} is ideal spacing of two adjacent digital codes

Integral Non-Linearity

The deviation in LSB or the percent of full scale range of an actual transfer function is INL error. The INL is classified into two types namely the best straight line INL and end point INL.

Figure of Merit

The FOM is a quantity used to represent the measure of efficiency and effectiveness of ADC. The FOM is given as

$$FOM\ (J/step) = \frac{P_{signal}}{\min(f_s, 2f_{in}) \times 2^{ENOB}}$$

where Psignal is the average power of the signal
fs is sampling frequency
fin is frequency of the input signal
Effective Number of Bits (ENOB)
ENOB can be obtained by

$$ENOB\,(bits) = \frac{SNDR - 1.76}{6.02}$$

where 1.76 is the term comes from quantization error in an ideal ADC
6.02 is the term which is used to convert decibels into bits
Signal to Noise and Distortion Ratio
SNDR is defined as the ratio of total received power to noise plus distortion power.

$$SNDR\,(dB) = 10\log\frac{P_s + P_n + P_d}{P_n + P_d}$$

where Ps is the average power of the signal
Pn is the average power of the noise components
Pd is the average power of the distortion components

CHALLENGES IN DESIGNING ADC
In mixed signal designs, combining analog circuits on a digital IC substrate was very difficult. Hence, there must be performance trade off and 15 sometimes there might be error in the designs. There were key challenges to be aware of while designing ADCs. The unavoidable challenges were:
Sampling rates, Bit resolution, SNR, ENOB.
Power, Supply voltage
Sampling Rates
To satisfy Nyquist sampling theorem, the sampling rate should be higher than twice the higher frequency of the input signal. However, faster sampling rate demanded higher bandwidth which in turn consumed more power and required better synchronization among the bits.

Bit Resolution
Bit resolution was a reflection of how closely the analog signal represented as a digital word. The resolution was used to convey how many discrete values can be produced over the range of analog values. So, it was necessary to determine the bit resolution of the ADC.
SNR
In ADC, any noise that presented in the signal reduced the accuracy of the digital output. So, care should be taken while considering the placement of neighbouring components and circuitry on the chip.

ENOB
ENOB was a broad way to measure the impact of distortion, noise and temperature impact on the performance of ADC. So, it was essential to have ENOB as high as number of ADC bits.

Power
In all SOC designs, power became an increasingly critical concern. There was an increase in power consumption whenever any of the performance metrics was improved. Always power became a trade off in the design of ADC.

Supply Voltage
As the need for portable devices were drastically increased, there was a necessity to design the circuits with reduced supply voltage. The design of analog circuits with reduced supply voltage was critical when compared to that of digital circuits. So, more concentration should be taken when it came to supply voltage for the ADC architectural design.

III. EXISTING METHODOLOGY

The power-limited applications such as wireless sensor networks, biometrics, and portable mobile handsets do not require high performance but do require the power-efficient ADC to extend the battery power duration. The power efficient feature needs the ADC circuit to be not only low power but also bandwidth effective. Power saving can be achieved in many aspects. Different ADC architectures may consume different power for the same specification. Literature published a SAR ADC for applications which require low power consumption, but it only accomplishes a SNDR of 43.3dB at 0.5 V supply voltage. The main sources of power consumption in a SAR DAC are the comparator and charge/discharge of the capacitor array [2]. The main power consumption in the SAR ADC architecture includes digital control circuit, comparator and capacitor digital-analog converter (DAC). To reduce the power consumption of digital circuits has recently become the targets of.it uses energy saving mode to reduce power dissipation. Actually, these techniques increase the SAR control

logic complexity, and thus consume more power. In this paper, an 8-bit SAR ADC is proposed which a passive sample-and-hold stage and a capacitor-based DAC are used to avoid application of opamps, since opamp operation consumes higher power. This ADC applies SAR control logic which reduces half comparator and digital circuit power consumption and then achieves low power consumption. The desired low power characteristic is preserved without making the sacrifice of its bandwidth. A power-saving switching sequence technique to reduce the power consumption of the capacitor array is presented and the content is organized as follows.

The prototype ADC was implemented using a one-poly-six-metal (1P6M) 0.18-µm CMOS process.

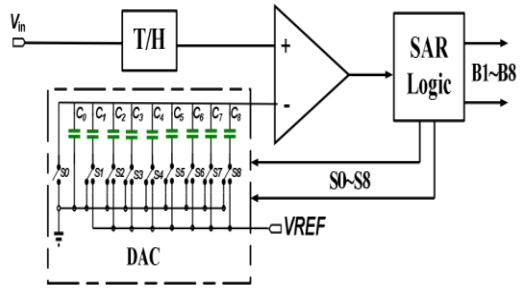


Figure1.3: 8-bit SAR ADC

In fact, the power of the boosted switch is negligible since the boosted driver operates at one ninth the clock frequency. Even though both MOSFETs have small spect ratios, the boosting technique keeps the on-resistance of the sampling switch small.

Simulation

The circuit is simulated using the tanner software and the VI & VO are the signals we get from the SAR logic block and the out1,out2,out3 are obtained as per the given inputs in the selected lines.

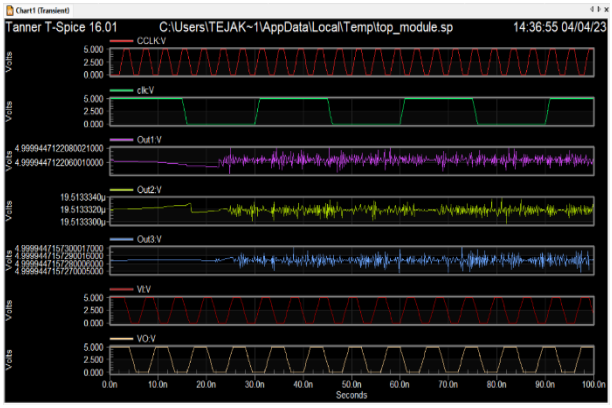
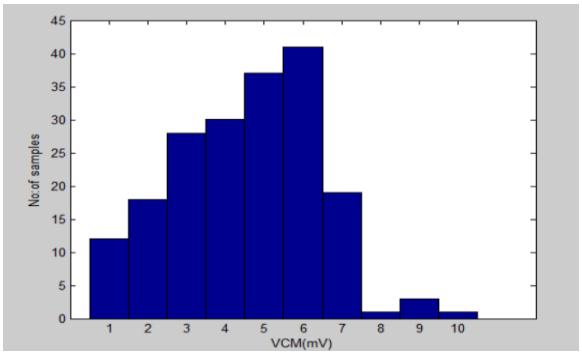


Figure1.4; Circuit simulation

The Static and dynamic performance are obtained by using the mtalab which include calling the tanner EDA function with F_s=1MS/s speed



Fgure1.5: simulation result of cascaded EA based voltage generator

The graph shows the sampling rate as per no of samples taken as per the applied voltage

The measured INL and DNL of the proposed ADC are shown in the figures

INL-Integral nonlinearity is a measure of performance in data converters and DNL Differential nonlinearity is a commonly used measure of performance in digital-to-analog (DAC) and analog-to-digital (ADC) converters These terms are generally important in measurement and control applications.

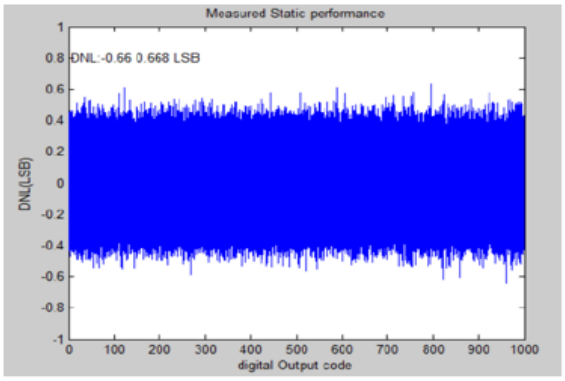


Figure1.6: DNL performance

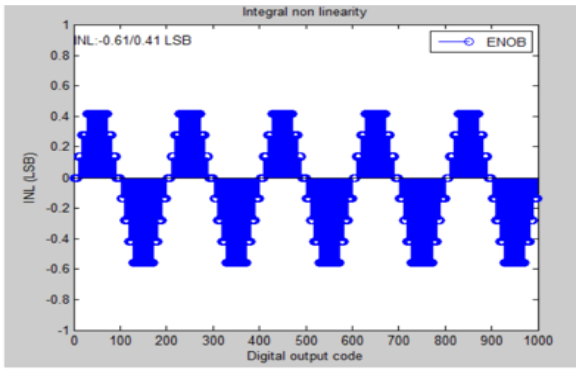


Figure1.6: INL performance

The Power consumption at each stage of simulation and how much the each and every stage consumed is shown in the figure 1.7

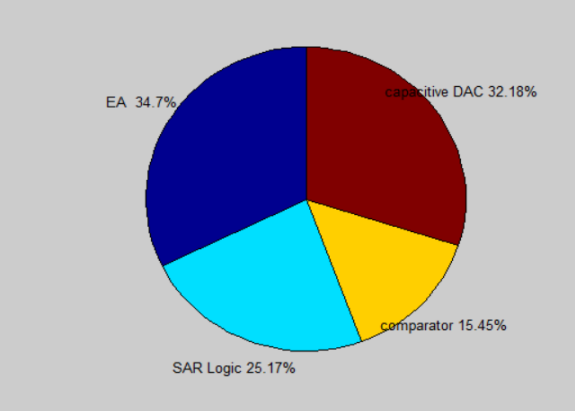


Figure1.7: The power consumption at each level

As compared to the power consumption the based generator consumed more power as compared with other levels.

IV.SYSTEM IMPLEMENTATION

The proposed single-ended asynchronous SAR ADC topology is designed and fabricated for a 10-bit resolution with a sampling speed of 1 MS/s, and the architecture is presented in Figure2.1. The proposed SAR ADC contains a binary weighted capacitive DAC, a bootstrap switch, dynamic comparator, asynchronous SAR logic with an internal comparator clock generator, and a bandgap reference generator. A dual-path bootstrap switch is presented that overcomes the sampling nonlinearity. The VCM-based switching sequence is proposed, which reduces the capacitive DAC's total capacitance by half due to the additional reference of VCM. Owing not only to the reduced capacitance, but also to the reduced switching step size as well as the removed switching-back operation, the VCM-based CDAC switching achieves excellent energy efficiency. The capacitive DAC is controlled by the digital output code, which is stored by asynchronous SAR logic and the decision made by the comparator. In the proposed single-ended asynchronous SAR ADC, a reference voltage of 0.6 V is generated by the error amplifier (EA)-based bandgap reference voltage generator. The 10-bit capacitive DAC provides the reference voltage DACP to the one input of the comparator, and the other input comparator has common-mode voltage sampling and hold operation is conducted by the sampling switch and capacitive DAC capacitors. The sampling signal, DACP<9:0>, CCLK, and SSAM are the control signals generated from the asynchronous SAR logic. The CCLK signal is provided to the comparator for the fast comparison of the comparator. For high speed and power efficiency, we implemented a two-stage dynamic latch comparator. In addition to this, for practical use, we implemented an on-chip bandgap reference voltage generator that provides better stability and reduced offset voltage distribution.

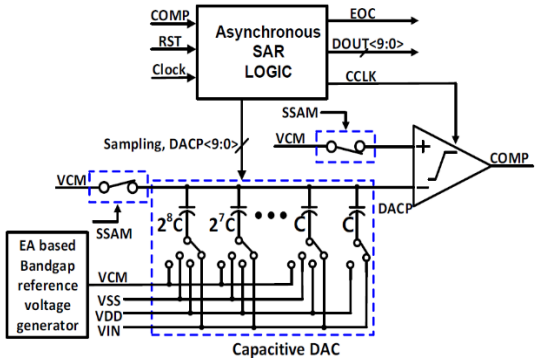


Figure 1.8: The proposed block diagram of the asynchronous SAR ADC with an EA-based bandgap reference voltage generator with two stage dynamic comparator.

Bootstrap Switching

Nowadays, for linear sampling, a bootstrap switch is frequently used, and its non-idealities have become pronounced; thus, its linearity is seriously degrading. Several techniques have been used to improve the performance of the bootstrap switch, such as modifying the circuit network or incorporating fast-turn-on circuits [13]. In figure1.8, we propose a technique to improve the linearity of the bootstrap switch. Ideally, to achieve the constant switch on-conductance, the Vgs of the sampling transistor M10 is independent of and constant with the input. The proposed technique integrates the dual-path bootstrap switch to improve the sampling nonlinearity, and operates at the sampling rate of 1 MS/s, with a 50% duty cycle and peak-to-peak voltage of 600 mV, as shown in figure1.8. This technique creates two paths for the signal; one is the main path, which contains M2 and C2, and the other is an auxiliary path, which contains M1 and C1. In the auxiliary path, the PMOS transistor's M1, M2, and M4's bulk terminals are connected to the V_X node, which prevents forward biasing. By the proposed dual-path bootstrap

switching technique, the nonlinear capacitance drives through the auxiliary path, while the gate of the sampling switch propagates the input signal, and hence the nonlinear capacitance is not directly being loaded into the main path. In this way, we can maximize the drive strength and signal linearity by independently optimizing the auxiliary path and the main path. The formula for voltage transfer to V_g from VIN and its phase are expressed as follows:

$$\frac{V_g}{VIN} = \left(sR_4C_g + \frac{C_g}{C2} + 1\right)^{-1}$$

$$\Phi = \omega_{IN} R_4 C_g \left(1 + \frac{C_g}{C2}\right)^{-1}$$

where $R_4 = 1/G4$, G4 is the on conductance of transistor M4, and Cg is the gate capacitance of transistor M10. By the proposed bootstrap switch, G4 is more linear because, instead of the supply voltage VDD, the bulk of M4 is connected to the nonlinear voltage V_X. Therefore, the square root of the error of nonlinear voltage V_X is directly proportional to G4. Hence, to improve the nonlinearity, the nonlinear voltage V_X goes through the bulk of M4, and nonlinear parasitic capacitance from the main path is removed by C2.

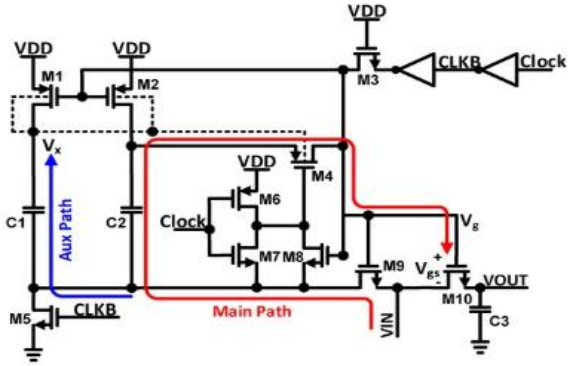


Figure 1.9: The schematic of the proposed bootstrap switch

CAPACITIVE DAC

Various circuit techniques could further enhance the low power advantage of SAR ADCs. A large amount of research has been conducted to save the CDAC's switching power consumption. Unlike the traditional SAR ADC architecture with two voltage references, the VCM-based switching scheme proposed could reduce the total capacitance of the CDAC by half due to the additional reference of VCM. It does not only reduce the overall CDAC capacitance, but also reduces the switching step size. With the removed switching-back operation, the VCM-based CDAC switching could achieve excellent energy efficiency and become popular for low-power designs. One drawback of the VCM-based switching scheme might be the difficulty in designing low-resistance switches for VCM. The monotonic switching technique can eliminate the need for VCM by the asymmetric CDAC switching, but this scheme has a varying common-level problem [14,15]. The energy-saving switching technique could implement VCM-based-like switching behavior without utilizing VCM by splitting each capacitor in half. The improved process controllability of advanced CMOS technologies also contributed to reducing the CDAC switching power consumption by decreasing the minimum unit capacitor values without the need for a dedicated process for capacitor implementation.

Two-Stage Dynamic Comparator

In the proposed two-stage dynamic latched comparator, two inverters are added to make the V_i node's voltage strong by providing a higher regeneration speed, as shown in Figure 2. The proposed architecture of the two-stage dynamic latch comparator provides high speed and power efficiency, and lowers the input-referred offset compared with conventional comparator architecture [16,17,18]. When the clock signal CCLK is turned off, the PMOS transistors M11 and M12 are on, then the V_i nodes are charged to VDD, and VB_i nodes are discharged to VSS during the reset phase. Consequently, there is no static power dissipation and static path due to charge sharing, and no DC flows in the static state of the proposed comparator. The NMOS transistors M9 and M10 drain, and output nodes charge to VDD, while the PMOS transistors of the regeneration stage turn on, and the VB_i nodes discharge to VSS.

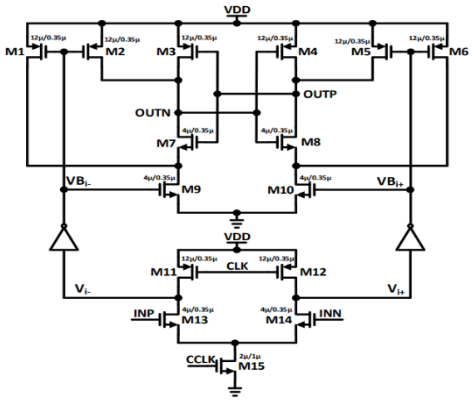


Figure 2: Transistor-level schematic of the dynamic comparator.

In the evaluation phase, when the clock signal CCLK increases, the V_i nodes discharge to VSS depending on the input voltage through the input transistors M13 and M14, and the tail transistor M15. The VB_i nodes are charged from VSS to VDD, while the V_i nodes are discharged to VSS in the evaluation phase. Other transistors will be turned on when the NMOS transistors M9 and M10 are turned on in the second stage and either of the VBi nodes reaches the threshold voltage V_{th}. Consequently, the latch is activated and regenerates the digital voltage at the output.

Asynchronous SAR Logic and Comparator Clock Generator:

o achieve faster bit conversion with an efficient time sequence, asynchronous SAR ADC is more popular [19,20]. Asynchronous SAR logic with an internally generated clock avoids the requirement for the high-frequency external clock, as all conversions are carried out in a single clock cycle. Asynchronous SAR control logic is implemented for a shorter critical path.A clock generator for SAR control logic is proposed, as shown in figure2.1 a. The asynchronous clock generator consists of a delay cell, variable delay, an edge counter, delay adjust block, and logic gates. VCOMP or VCOMN are low, which allows VI to decrease after the decision of the comparator. Then, after the variable delay, VO is also low, which makes the CCLK decrease, and the SAR logic controller is triggered. The comparator starts the comparison when the reset of the comparator is completed, and VI, VO, and CCLK increase. To maximize the sampling period of conversion and to adjust the time delay, the delay adjust block and counter are used in feedback.

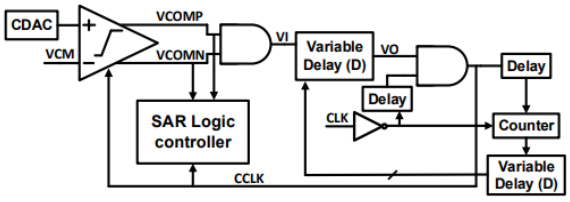


Figure 2.1: Block diagram of the clock generator.

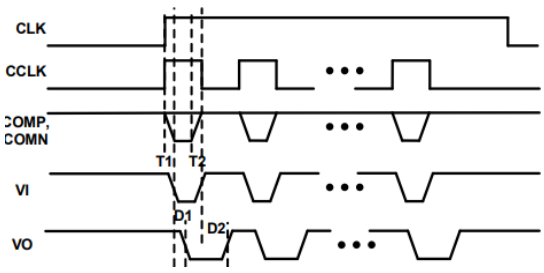


Figure 2.2: Timing diagram of the clock generator.

CCLK provides the reset time of the comparator and more time for DAC settling, as shown in Figure2.9. The proposed clock generator eliminates the memory effect in the comparator and speeds up the bit conversion. Hence, it also helps to improve the ADC robustness. The timing diagram of the proposed clock generator is shown in Figure2.9. The comparator's decision time and reset time are represented as T1 and T2, respectively. D1 and D2 are the delay time, and unequal D1 and D2 can be obtained by the variable delay cell, as depicted in Figure 3. The variable delay cell is composed of an inverter array, implemented to achieve the desired variable delay. The arrangement of the inverter array leads the delay D1 to be small for the falling edge from VI to VO and delay D2 to be large for the rising edge.

Reference voltage generators are required to stabilize the overall PVT variation, and also need to be implemented without modifying the fabrication process. The bandgap reference voltage generator (BGR) is a popular reference voltage generator that successfully achieves the requirements. Low power and low voltage operation are the characteristics of reference voltage generators. The error amplifier feedback keeps the same voltage level at both inputs of EA, and R3 generates the voltage difference between the two BJTs, as represented in Figure3.1. A Soft-Start circuit is added to the output; when the power signal is high, a current starts to flow through the PMOSs, M11, M12, and M13 connected in diode fashion. To prevent the BGR peak voltage, it slowly charges the capacitor C3, and the BGR output voltage rises. The output of the error amplifier controls the gate of transistors M1 and M3 so that the input voltages of the error amplifier are equal. The positive feedback and negative feedback improve the loop stability of the proposed error amplifier. A detailed schematic of the error amplifier-based BGR circuit is shown in figure 2.3. VB1, VB2, and VB3 are the biasing voltages provided by the bias circuit to the cascaded error amplifier. We assume that the transistors M15–M18 and M23 are matched in terms of their aspect ratios, and the drain current of M18 is represented as:

$$I_{18} = I_{17} = I_{15} = I_{16} = I_{24} = \frac{g_{m24}}{2}(OUT - V_{THn}) = \frac{g_{m16}}{2}(V_{ds23} - V_{THp})$$

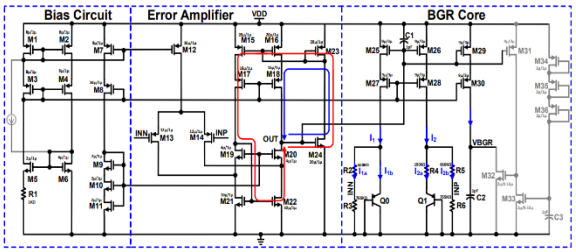


Figure2.3: Detailed schematic of the proposed error amplifier based bandgap reference voltage generator;

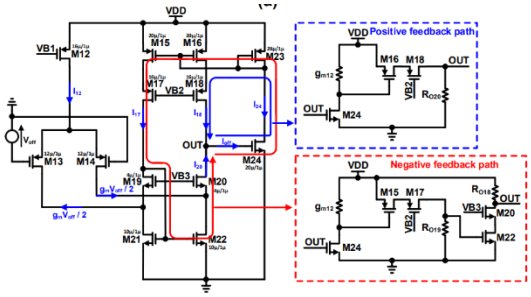


Figure 2.4: Proposed folded-Cascoded error amplifier with intentional positive and negative feedback loop.

Initially, V_{off} caused the output offset current I_{off} of the proposed error amplifier circuit shown in Figure2.4. Between the feedback stage and cascade stage output, OUT triggers the two opposite currents. The offset currents I_{18} and I_{20} are the positive feedback path and negative feedback path, respectively, and act contrary to each other. Therefore, the output offset current I_{off} is expressed as follows:

$$I_{off} = I_{18} - I_{20} = I_{18} - (I_{22} - I_{14}) \quad (4)$$

$$I_{off} = \frac{g_{m16} V_{ov16}}{2} + \frac{g_{m14} V_{off}}{2} - \frac{g_{m22} V_{ov22}}{2} \quad (5)$$

where V_{ov} is the overdrive voltage; $V_{ov} = OUT - V_{TH}$ and $I_{20} = g_m V_{off}/2$. By carefully setting the overdrive voltage V_{ov} and transconductance g_m, we can alleviate the output offset current I_{off}, as estimated by Equation (5). We assume that all transistors' transconductance is the same; then Equation (5) can be expressed as:

$$I_{off} = \frac{g_m}{2} (V_{ov16} + V_{off} - V_{ov22})$$

Equation (6) represents that we can reduce the output offset current I_{off} by adjusting the V_{ov22} to $V_{ov16} + V_{off}$. This type of reduction in the output offset current I_{off} can be achieved by inducing the intentional feedback loop in the proposed error amplifier. The Monte Carlo simulation of the proposed error amplifier-based bandgap reference voltage generator is depicted in Figure. An on-chip voltage generator with a standard deviation of less than 1 LSB is used in the proposed ADC architecture.

V.SYSTEM SIMULATION RESULTS

The proposed block diagram of the asynchronous SAR ADC with an EA-based bandgap reference voltage generator with two stage dynamic comparator. Is simulated using the Tanner software and the performances response are obtained as per the applied voltage using the selected lines applied at vcm.

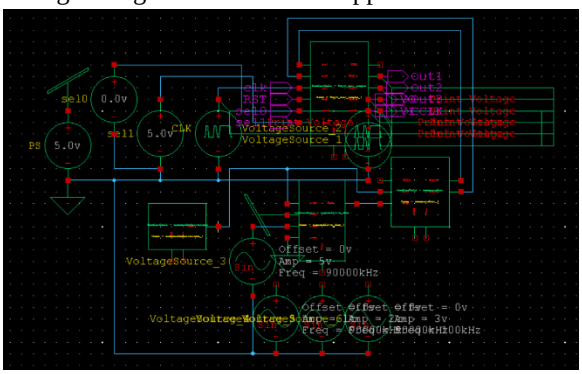


Figure 2.5: The asynchronous SAR ADC with an EA-based bandgap reference voltage generator with two stage dynamic comparator.

The block diagram includes with cascaded erroramp with the blocks shown in the Figure 2.3, figure 2.4.we use two stage dynamic comparator for the fast response. The bootstrap switch used in the capacitive ADC for Storing and Improves the non-Linearity factor, sampling rate.

The circuit simulation result is shown in the figure 2.6 with the improved performance as compared to the existing with increasing in the speed and overcome the delay.

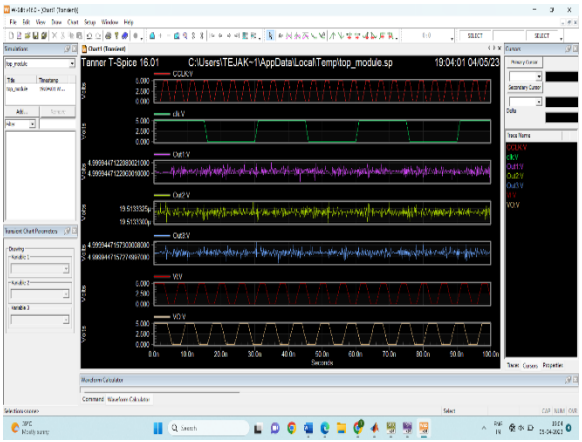


Figure2.6:The Asynchronous SAR simulation.

The Performance of the system and the details regarding the levels and power consumption at each level and INL and the DNL performance are obtained using the matlab and the Tanner EDA function.

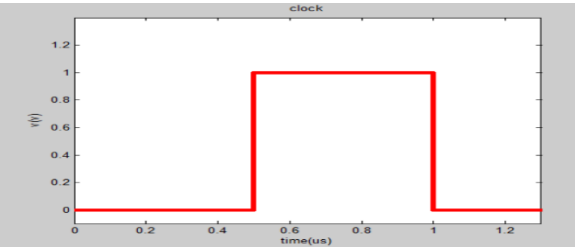


Figure 2.7: Clock Signal.

The figure2.7 gives the applied clock response to the capacitive DAC.

The Simulation of the Capacitive DAC gives the response in DACP and the end of conversion factor. CDAC shows the output of the capacitive DAC (DACP) settling of input signals according to the clock signal. An end-of-conversion (EOC) signal will be generated after the completion of the conversion cycle based on the asynchronous SAR logic.

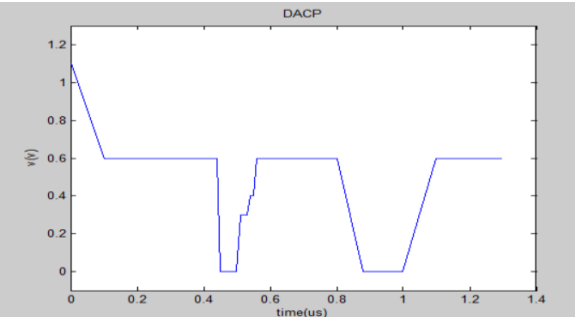


Figure 2.8: DACP

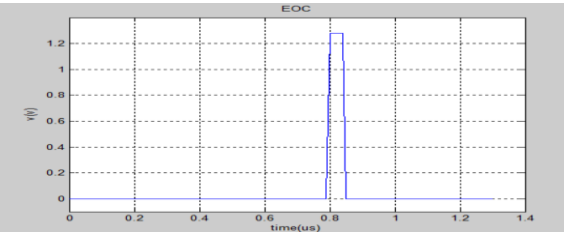


Figure 2.9: End of Conversion (EOC)

In the sampling phase, the bottom plates of all capacitors are connected to the VCM and the top plates are connected to the VIN. Thus, the input voltage is sampled on the binary weighted capacitor array, and we obtain the first signed bit without consuming any switching energy. Depending on the first signed bit, the next conversion cycle is either charged to VDD or discharged to VSS from VCM. Hence, the MSB capacitor is not required in the proposed switching scheme. The sensitivity due to the capacitor mismatch, dynamic, and static performance of the proposed capacitive DAC switching scheme is checked based upon the behavioral simulation in MATLAB.

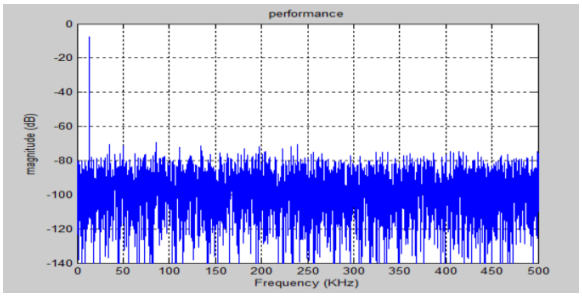


Figure 3: Dynamic performance of proposed switching with unit capacitor

In the static performance we get INL and DNL response of the proposed switching with unit capacitor. the deviation in LSB or the percent of full scale range of an actual transfer function is INL error. The INL is classified into two types namely the best straight line INL and end point INL. The measured INL and DNL of the proposed ADC are shown in the figures INL-Integral nonlinearity is a measure of performance in data converters and DNL Differential nonlinearity is a commonly used measure of performance in digital-to-analog (DAC) and analog-to-digital (ADC) converters These terms are generally important in measurement and control applications.

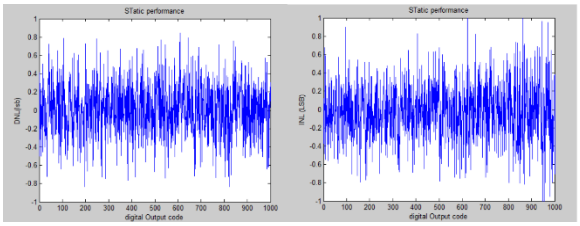


Figure 3.1: Static performance of proposed switching with unit capacitor.

Monte Carlo simulation is a statistical method used to model and analyze the behavior of complex systems. It involves generating a large number of random samples and using them to estimate the distribution of possible outcomes.

In the context of a bandgap reference voltage generator, Monte Carlo simulation can be used to analyze the impact of variations in the manufacturing process on the performance of the circuit. The circuit typically consists of an error amplifier, which compares a reference voltage with the output of a temperature sensor, and a voltage divider that generates a stable reference voltage. Variations in component values, such as resistor and transistor

parameters, can affect the accuracy and stability of the output voltage.

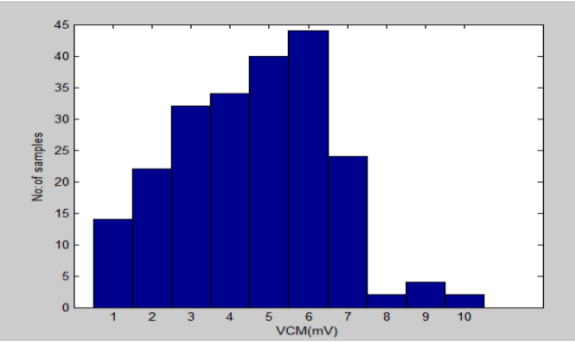


Figure 3.2: Monte Carlo analysis result of error amplifier-based bandgap reference voltage generator

Measured dynamic performance at a sampling speed of 1 MS/s with the two different input frequencies and shown in the figure 3.3.

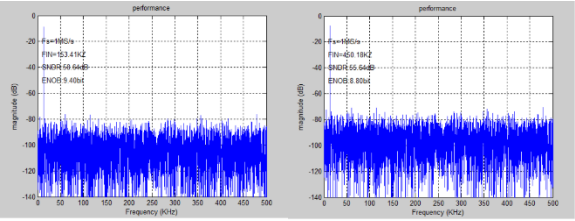


Figure 3.3: Dynamic performance with two different frequencies.

To explain the terms used in this statement, SAR ADC stands for Successive Approximation Register Analog-to-Digital Converter, which is a type of ADC commonly used in many applications. DNL stands for Differential Non-Linearity, and INL stands for Integral Non-Linearity. These are measures of the deviation from an ideal linear response in the ADC, and are important parameters for evaluating its performance. A negative DNL or INL value indicates that the ADC is producing output values that are lower than expected, while a positive value indicates that the output values are higher than expected. the measured DNL and INL results presented in Figure 3.4a,b are likely plotted as a function of the input signal amplitude, and show how the non-linearity of the ADC varies across its operating range.

The fact that the DNL and INL values are both positive and negative indicates that the ADC is not perfectly linear, but still falls within an acceptable range for many applications.

ENOB stands for Effective Number of Bits, which is a measure of the resolution of an ADC. A higher ENOB value indicates that the ADC is able to provide more precise and accurate measurements. The trend of the proposed ADC's ENOB with an on-chip EA-based bandgap reference voltage generator is likely presented in Figure 3.5, and shows how the ENOB varies with different operating conditions, such as input signal frequency or amplitude.

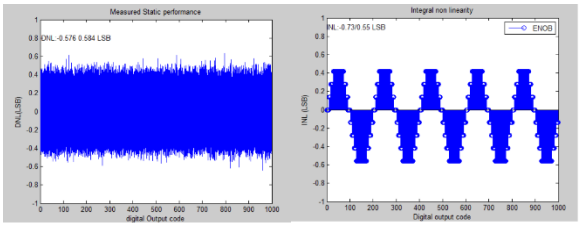


Figure 3.4: Measured static performance: (a) Differential non-linearity (DNL); (b) Integral non-linearity (INL).

Finally, an EA-based bandgap reference voltage generator is a circuit that produces a stable and accurate voltage reference, which is important for the proper operation of many analog circuits, including ADCs. The power breakdown of the proposed EA-based bandgap reference voltage generator likely shows how the power is distributed among the different components of the circuit, and can provide insight into the efficiency and effectiveness of the design. As shown in the figure 3.6.

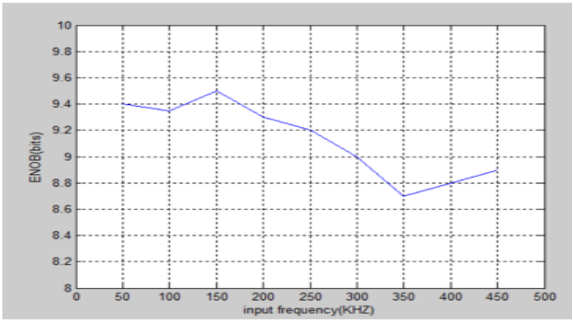


Figure 3.5: ENOB Variation

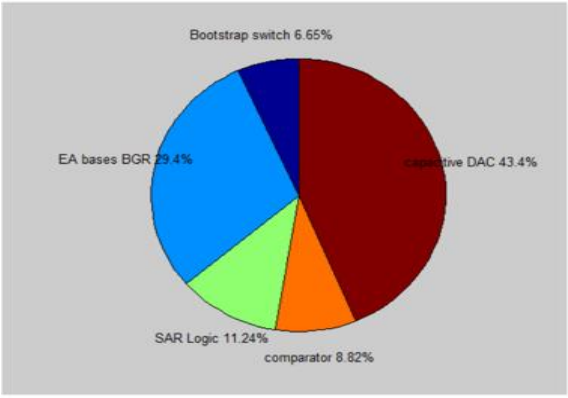


Figure 3.6: Power consumption at each stage

VI.CONCLUSION

The specific architecture for a SAR ADC (Successive Approximation Register Analog-to-Digital Converter) that uses high threshold voltage cells. The Sample and Hold circuit, which is used to capture and hold the input voltage during the conversion process, is designed using high threshold voltage transistors, and compared with a low Vt (threshold voltage) circuit. The open loop comparator, which compares the input voltage to a reference voltage, is also designed using high Vt cells, which helps to reduce power consumption and delay. The DAC (Digital-to-Analog Converter) block, which converts the digital output of the SAR register into an analog voltage, is also designed using high threshold voltages.

By using high threshold voltage cells in these different parts of the ADC, the overall power consumption and delay of the ADC are significantly reduced. The binary search algorithm is used for the SAR conversion process, and the sampling rate of the ADC is optimized for use with an ECG (Electrocardiogram) signal. This results in the best possible performance for the given application.

A SAR ADC architecture using high threshold voltage cells has been presented. The transmission gate Sample and Hold circuit is designed using high threshold voltage transistors and compared with low Vt Sample and Hold circuit. The open loop comparator using basic operational amplifier has been designed with high Vt cells to reduce power consumption and delay using CMOS technology. The resistor string type DAC block has also been designed in CMOS technology using high threshold voltages. Such an ADC approach significantly reduces power consumption and delay of the ADC. This ADC uses the binary search algorithm and fit with the sampling rate of the ECG and gives the best performance.

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