Review of 2X2 Vedic Multiplier Using Various Full Adders

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***Abstract*- The complexity of the chip is increasing as the advances in VLSI technology leads to accumulation of more and more devices on the single chip. Due to this high density of the chip, the power dissipation of the chip also gets increases demanding in the low power CMOS VLSI designs. Multiplication is one of the basic arithmetic operations in digital computer system and digital signal processor. In a typical scientific program 8.72% of all instructions are multiplies.**

***Keywords* - Nikhilam Navatascaramam Dasatah, Vedic Sutra, Adders, VLSI Design, DSP.**

I.INTRODUCTION

In this we are analyzing 2x2 multiplier architecture based on Vedic sutra" Nikhilam Navatascaramam Dasatah", which enhances the speed of the multiplier, further the design is implemented using various logic full adders such as 9A full adder, 9B full adder, 28T full adder, Complementary and Level Restoring Carry logic (CLRC), 13A full adder, 10T full adder, 10T adder 1, Gate Diffusion Input based adder (GDI).

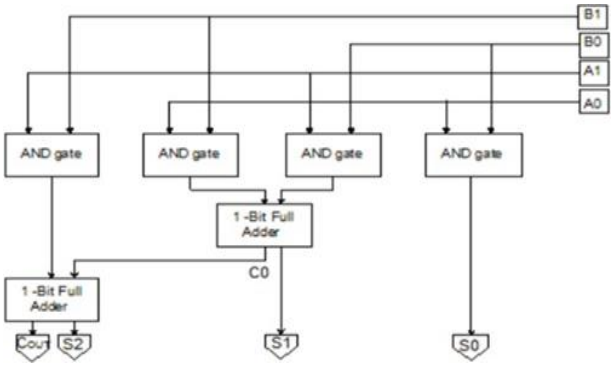

Fig. 1. Block Diagram of 2x2 Vedic Multiplier

WORKING

The 2x2 Vedic multiplier will be implemented using four, 2 input AND gates and using two adders as same in the block diagram and schematic diagram as shown in figure 1 and 2 respectively. The AND gates are used for the multiplication of bits in the multiplier and multiplicand, and the adders are used to add the products with the carry to give the exact output of the multiplication. The inputs are $A_0 A_1$ and $B_0 B_1$. The process for multiplication of two bits are as, the last bits of the multiplier and multiplicand i.e. A_0 B_0 are multiplied and this gives the last bit of the final product i.e. S_0. The next bit of the multiplicand and multiplier i.e. $A_0 B_1$ and $A_1 B_0$ are multiplied and that partial product is added with the adder to get the next bit i.e. S_1 of the final product. Then the MSB of the multiplier is multiplied with multiplicand i.e. A_1 B_1 are multiplied using AND gate and that product is added with the carry from the previous bit using another adder, the output from this adder will give the MSB of the final product of the multiplication i.e. S_2 and the carry from the multiplication of the final bit will give the final carry bit i.e. C_{out} of the multiplication

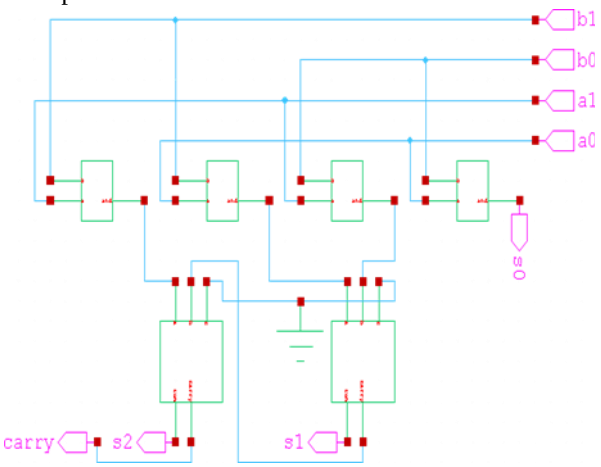

Fig. 2. Schematic Diagram of 2x2 Vedic Multiplier.

II.TRUTH TABLE OF 2x2 VEDIC MULTIPLIER

The table 1 shows the truth table of 2x2 Vedic multiplier in that A_0 A_1 and B_0 B_1 are the input bits and S_0, S_1, S_2 are the output bits and C_{out} is the carry bit and the equations for the output bits are as follows,

$S_0 = A_0B_0$

$S_1 = (A_0B_1) + (A_1B_0)$

$S_2 = A_1B_1$

INPUT				OUTPUT			
A_1	A_0	B_1	B_0	Cout	S_2	S_1	S_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

Table. 1. Truth Table of 2x2 Vedic Multiplier

III. OUTPUT WAVEFORM OF 2x2 VEDIC MULTIPLIER

The figure 3 shows the output waveform of 2x2 Vedic multiplier and the S_0, S_1, S_2 are the output bits and C_{out} is the carry bit for the 2x2 Vedic Multiplication.

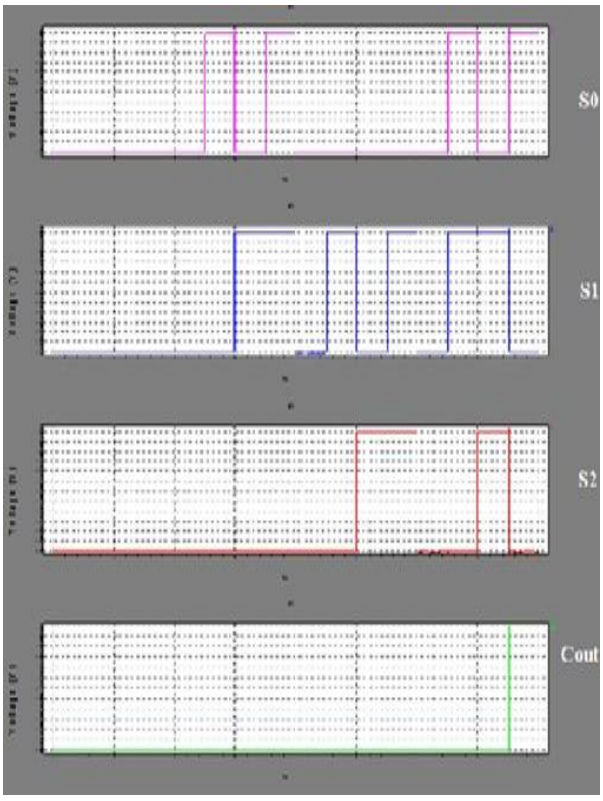

Fig. 3. Output Waveform of 2x2Vedic Multiplier

IV.RESULT AND COMPARISON OF 2x2 VEDIC MULTIPLIER

Here the comparison of delay, power delay product, average power consumption, static power dissipation, Transistor Count (TC) and area of 2x2 Vedic multiplier using 9A full adder, 9B full adder, GDI, 13A full adder, 10T full adder, 10T adder 1, 28T full adder and CLRCL full adder are made and their comparison table are shown in table 2, 3, 4 and the figures 4, 5, 6 shows the comparison charts of above parameters using various full adders.

2X2 MULTIPLIER USING	DELAY (ns)	AREA (um^2)
9A	2.90	10.00
9B	4.34	10.00
10T	1.54	10.00
10T 1	1.07	10.00
13A	2.83	10.00
28T	5.67	14.50
GDI	5.98	10.00
CLRCL	2.57	10.00

Table 2 Comparison Table of Power Consumed, Static Power Dissipation and TC

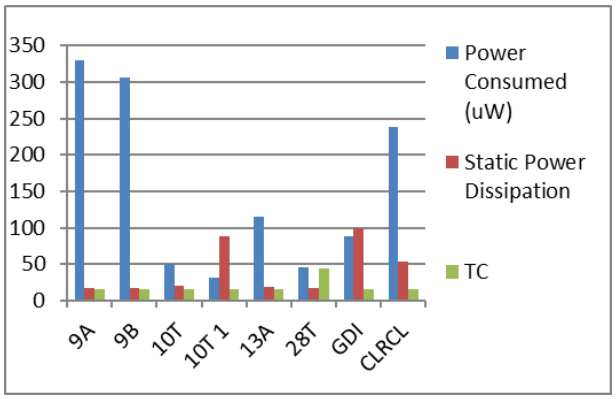

Fig. 4. Comparison of Power Consumed, Static Power Dissipation and TC

2X2 MULTIPLIER USING	AVERAGE POWER CONSUMED (uW)	STATIC POWER DISSIPATION (nW)	TC
9A	329.92	17.30	16
9B	305.48	17.36	16
10T	49.78	20.93	16
10T 1	30.78	88.41	16
13A	115.74	19.21	16
28T	45.74	17.44	44
GDI	88.55	99.48	16
CLRCL	237.77	52.95	16

Table 3 Comparison Table of Static Power Dissipation

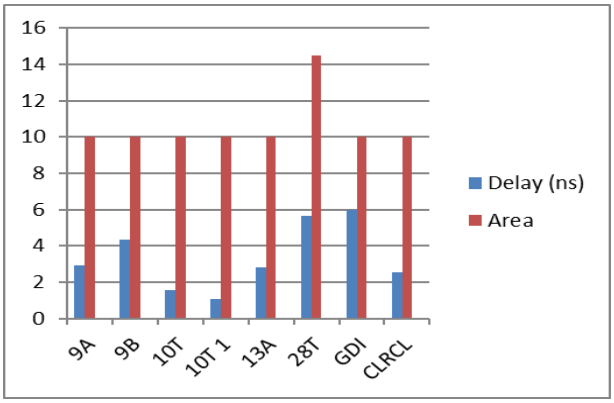

Fig. 5. Comparison of Static Power Dissipation

2X2 MULTIPLIER USING	DELAY (ns)
9A	2.90
9B	4.34
10T	1.54
10T 1	1.07
13A	2.83
28T	5.67
GDI	5.98
CLRCL	2.57

Table 4 Comparison of Delay

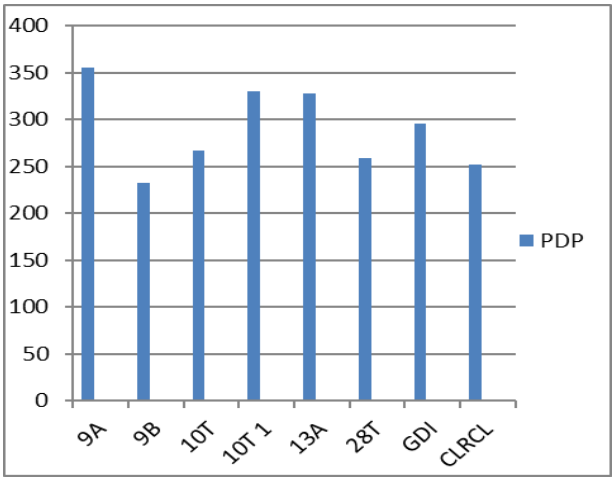

Fig. 6. Comparison of Static Power Dissipation

V.CONCLUSION

In this paper 2x2 multiplier using various logic full adders such as 9A full adder, 9B full adder, 28T full adder, Complementary and Level Restoring Carry logic (CLRC) adder, 13A full adder, 10T full adder, 10T adder 1, Gate Diffusion Input based adder (GDI) have been designed, simulated, analyzed and compared using tanner EDA tool with 130nm technology. From the above comparison of 2x2 Vedic multiplier using various full adders, 9A full adder is the best in case of power consumption, power delay product, area, transistor count and static power dissipation. 9A full adder will produce best output but the main disadvantage is that it will consume more power comparing to other adders.

REFERENCE

[1] Manoj Duhan, Kusum Dalal, Viplove Kumar, "A Studyof Full Adder circuits from Power and Speed of Operation Perspective", 2014.

[2] S.K.Manikandan, C.Palanisamy, "Design of an Efficient Binary Vedic Multiplier for High Speed Applications Using Vedic Mathematics with Bit Reduction Technique", 2016.

[3] Ch.Harish Kumar, "Implementation and Analysis of Power, Area, and Delay of Array, Urdhva, Nikhilam Vedic Multipliers", Volume 3 Issue 1, 2013.

[4] Navya Rajput, Ankit Jindal, Sahil Saroha, Rithesh Kumar, Geetanjali Sharma, "A Novel and High Performnace Implementation of 8x8 Multiplier based on Vedic Mathematics Using 90nm Hybrid PTL/CMOS Logic, Volume 69-NO- 27, May 2013.

[5] Shweta S. Khobragade, Swapnili P, Karmore, "Low Power VLSI Design of Modified Booth Multiplier" Vol.9, No.1, July 2013.

[6] Poornima M, Shivaraj Kumar Patil, Shivukumar, Shridhar K P, Sanjay H, "Implementation of Multiplier using Vedic Algorithm" Volume-2, Issue-6, May 2013.

[7] Savita Nair, Ajit Saraf, "A Review Paper on Comparison of Multipliers based on Performance Parameters", ICAST 2014.

[8] Arvind Nigam, Ragavendra Singh, "Comparative Analysis of 28T Full Adder with 14T Full Adder using 180nm", March 2016.

[9] Pushpalata Verma, K K Mehta, "Implementation of an Efficient Multiplier based on Vedic Mathematics Using EDA Tool" Volume-1, Issue-5, June 2012

[10] Sumit Vaidya, Deepak Dandekar, "Delay-Power Performance Comparison of Multipliers in VLSI" Volu-2, No-4, July 2010.

[11] Sayali Shembalkar, Samiksha Dhole, Tirupati Yadav, Prasheel Thakre, "Vedic Mathematics Sutras- A Review", Volume-5, Issue-1, Jan 2017.

[12] MD. Masood Ahmad, Dr.K. Manjunathachari, Dr.K.Lalkishore, "Design and Analysis of Low run-time Leakage in a 13 Transistors Full Adder in 45nm

Technology", 2016.
[13] Kripa Mathew, S. Asha Latha, T. Ravi, E. Logashanmugam, "Design and Analysis of an Array Multiplier Using an Area Efficient Full Adder Cell in 32nm CMOS Technology", Volume-2, Issue-3, 2013.
[14] Pankaj Kumar, Poonam Yadav, "Design and Analysis of GDI based Full Adder circuit for Low Power Applications" Volume-4, Issue-3, March 2014.
[15] M.B.Damle, DR.S.S.Limaye, M.G.Sonwanai M.B.Damle, DR.S.S.Limaye, M.G.Sonwanai, "Comparative Analysis of Different Types of Full Adders" Volume-11, Issue-3, June 2013.
[16] Subodh Wairya, Rajendra Kumar Nagaria, "Comparative Performance Analysis of X-OR-X-NOR Function based High Speed CMOS Full Adder circuits for Low Voltage VLSI Design" Volume-3, No-12, April 2012.
[17] Chilton Fernandes, Samarth Borkar, "Application of vedic mathematics in computer architecture" Volume-1,Issue-5, September 2013.
[18] Sumit R. Vaidya, D. R. Dandekar, "Performance Comparison pf Multipliers for Power-Speed Trade-off in VLSI Design,
[19] R.Senthil Ganesh, K.Hemamalini, V.Indhu, S.Kamala Prabha, " Review of Vedic Sutras", Volume-6, Issue-1, Feb 2018.
[20] Manjunath K M, Abdul Lateef Haroon P S, Amarappa Pagi, Ulaganathan, "Analysis of Various Full- Addercircuits in Cadence" 2015.
[21] Soniya, Suresh Kumar, "A Review of Different Type of Multipliers and Multiplier-Accumulator Unit" Volume-2, Issue-4, August 2013.
[22] Shivashankar Mishra, V.Narendra, Dr.R.A.Mishra, "On the Design of High-Performance CMOS 1-bit Full Adder circuit" 2011.
[23] Shennu rana, Rajesh mehra, "Optimized CMOS Design of Full Adder using 45nm Technology" Volume 142, Issue-13, May 2016.
[24] R.Senthil Ganesh, K.Hemamalini, V.Indhu, S.Kamala Prabha, "Low Powered High Speed and Area Efficient Full Adders" Volume-5, Issue-2, Feb 2018.
[25] R.Senthil Ganesh, K.Hemamalini, V.Indhu, S.Kamala Prabha, "Review of Multipliers" Volume-4, Issue-4, March-2018.