A High-Speed, Area-Efficient Transfer Method Using A Reverse Carry Propagate Adder

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Abstract- The most important component of any electronic device has historically been the arithmetic and logic unit. An efficient algorithmic function, such as addition and multiplication, which is required for an arithmetic as well as logic unit to be significant in the current improvement. For performing modular arithmetic in several cryptography and pseudorandom bit generator (PRBG) algorithms, the three-operand binary adder is the fundamental functional unit. In this paper, this study purposes a reverse carry propagate adder. A carry input signal is more important than the carry output signal because, in the RCPA structure, the carry signal flows counter-clockwise from the most significant bit to the least significant bit. In the presence of delay changes, this carry propagation technique results in greater stability. Three implementations of the reverse carry propagate full-adder cell with different delay, power, energy, and accuracy levels are introduced by this study. As a result, it continues as one of the greatest options for creating huge arithmetic circuits with little increase in area and minimal power and energy usage.

Keywords: Pseudorandom bit generator, RCPA, three-operand binary adder, reverse carry propagate adder.

I. INTRODUCTION

Addition is one of the common and widely used fundamental arithmetic operation in many VLSI systems. Other similar arithmetic operations are subtraction, multiplication, division, address calculation etc. Using binary adders the full adder is designed and improving 1-bit full adder performance plays an important role in VLSI. Different varieties of full adders exploit completely different logic designs and technologies [1-2]. This method unremarkably aim at increasing speed and reducing power dissipation. To improve the performance of adder there we have two methods. One is 'System Level viewpoint' method and second method is critical Style view point'. In system level viewpoint it consists of finding the longest signal path in the ripple adders and reduce the trail so as to scale back the full signal path delay [3-4]. In the majority of cases, the carry out bit is the most significant bit, which has to be determined along the longest signal path. The second method is 'Circuit Style Viewpoint' in transistor level, semiconductor device services are supported by designing of high performance full adder. An optimized design is required to prevent any decrease in signal magnitude, provide small delays, consume less power in critical paths and even at low supply voltage maintain consistency while moving headed for smaller designs such as in nanometre range. Driving capability for different loads, outputs without glitches, layout regularity [5-8].

One of the major challenges in today's world is to create a circuit type that offers not only low power consumption but also good performance in VLSI circuits and the ability to minimise delay parameters at the appropriate time. To achieve the desired result, we might enhance these two characteristics. [9-10]. There are three major improvements through which we can consume the power such as the active power due to charging and discharging of the circuit capacitances during switching. Due to the leakage current, there is a leakage power in the circuit. [11]. Adiabatic Logic is one of the most prominent technique which plays a very vital role for the power consumption in the circuit. Adiabatic logic aims to decrease the power in the logic circuit. Although there are many other techniques like pass transistor logic who helps to reduce the power but adiabatic logic is one of the most prominent technique which is used for the consumption of power. In VLSI, another most prominent technique which is used to reduce the power (i.e) Domino Logic. In Very Large Scale Integration Circuit, performance plays a very vital role for the architecture of low power and high speed in the circuit.. It is the combination of the

Transmission Gate (TG) logic and C-CMOS (Complementary Metal Oxide Semiconductor) logic [12-15].

In this study, the proposed technique using an approximate adder design style gives more freedom to the designer to select different modules in a circuit depending upon the applications. The simulation results show that the proposed hybrid full adder circuits have better performance in terms of power, delay as well as PDP with a supply voltage ranging from 1.0 V to 2.4 V than most of the standard full-adder cells owing to the novels design modules proposed in this paper. Therefore, it remains one of the best contenders for designing large arithmetic circuits with low power consumption and reduced energy consumption while keeping the increase in area to a minimum.

II. PROPOSED METHODOLOGY

In approximation adders, the input carry is propagated in an opposition manner, with the propagation carry from the most significant bit (MSB) to the lower significant bit (LSB) generating the carry output (LSB). For the propagation during which the carry weight diminishes, RCPFA introduces an output signal that is a forecast signal. Additionally, RCPFA reduces energy usage and delay while being Unaffected by variations in delay.

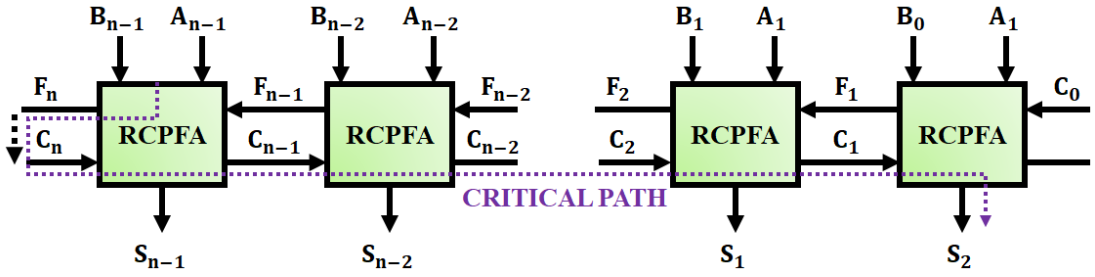

Figure: 1 Block diagram for the proposed work

A) REVERSE CARRY PROPAGATE FULL-ADDER

The reverse carry propagate adder have carry signal propagation from the most significant bit(MSB) to the least significant bit(LSB), which results in greater relevance to the input carry than the output carry. The technique of carry circulation in reverse order with delay variations increases the stability.

Cell each exact FA generates its carry output and sum signals using,

$$2C_{i+1} + S_i = A_i + B_i + C_i \quad (1)$$

Where Ai (Bi) is the i^{th} bit of the input A (B), Ci (Ci+1) is the carry input (output), and Si is the i^{th} bit of the sum. Based on this equation, the output signals in the i^{th} bit position depends on the i^{th} bits of the inputs A and B and the carry output of the previous position (C_i). By moving the term C_i (Ci+1) to the left (right) side of the equation

$$S_i - C_i = A_i + B_i - 2C_{i+1} \quad (2)$$

For this structure, the outputs are the sum and the carry signals with the same weights. Notice that the carry input of the ith bit position (Ci+1), should be generated by the FA in the (i + 1) st bit position

B) INTERNAL STRUCTURE OF RCPFA

To determine a structure for RCPFA, the Karnaugh maps of the summation result (Si) and carry (Ci) were drawn based on (4.3) and considering the forecast signal as an input. The Boolean relations between inputs for generating Si and Ci are obtained a

$$S_i = \overline{C_{i+1}}\,\overline{F_i} + \overline{C_{i+1}}\,A_i + \overline{C_{i+1}}\,B_i + A_i\,B_i \quad (3)$$

$$C_i = C_{i+1}\,F_i + C_{i+1}\,\overline{A_i} + C_{i+1}\,\overline{B_i} + \overline{A_i\,B_i} \quad (4)$$

An optimized gate-level structure for implementing RCPFA may be achieved by simplifying (4.5) and (4.6) as

$$S_i = F_i(\overline{C_{i+1}} + A_i\,B_i) + \overline{C_{i+1}}(A_i + B_i) = F_i\,\overline{X_i} + \overline{Y_i} \quad (5)$$

$$C_i = F_i\overline{(\overline{C_{i+1}}\,(A_i + B_i))} + \overline{(\overline{C_{i+1}} + A_i\,B_i)} = F_i\,Y_i + X_i \quad (6)$$

In this adder structure, the accuracy and performance of RCPFA depend on the signal F whose generation leads to some overheads. This means that optimizing the generation of the forecast signal may simplify (optimize) the general form of the RCPFA structure.

C) FIR FILTER

Two major filter forms are available, analogue and digital. Depending on the classification criterion, filters can be categorised in many categories. The two main forms of optical filters are digital filters for finite pulse response (FIR) and digital filtering (IIR).

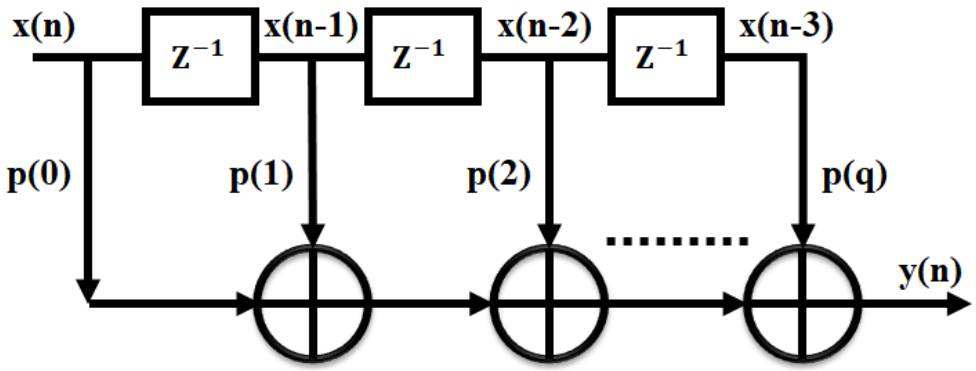

Figure: 2 Finite Impulse Response Filter

Digital Signal Processing filters are a predominant category of filter used. It's claimed that FIR filters are finite and they have no input. Most frequently the filter coefficients stay stable and established applications for signal processing.

$$out(n) = \sum_{i=0}^{N-1} x(n-i)h(i) \quad (7)$$

Where {h (i): i = 0… N-1} are the filter coefficients. A Filter conducts a convolution operation, mostly constructed on the premise of limitless signal lengths.

D) ERROR ANALYSIS

Analytical Expressions for the Mean Error, MED, and Variance of Error

$$\text{MRED} = \frac{1}{2^{2n}} \sum_{i=1}^{2^{2n}} \left| \frac{ED_i}{S_i} \right| \quad (8)$$

Where Si and ED_i are the exact result and the error distance for the i^{th} input set, respectively.

The mean error is one of the important parameters that capture the impact of the error on the functional correctness of the applications. The error in each bit is −1, 0, or 1. The difference between the probabilities of −1 and probability of 1 determines the mean error in each bit position. Hence, the mean error is defined as

$$\mu = \sum_{i=0}^{n-1} [P(e_i = 1) - P(e_i = -1)] \times 2^i \quad (9)$$

The error occurs when the right side of (2) becomes 2 or −2. Some other error conditions existed in the truth tables of RCPFA-II and RCPFA-III (items 4, 5, 7, and 8) while they were not happened in the chain of adders. One may use to obtain the mean error as,

$$\begin{aligned} \mu = \sum_{i=0}^{n=1} [& P\left(C_{i+1} = 0 \middle| (A_i = 1 \cap B_i = 1)\right) \\ & \times P(A_i = 1 \cap B_i = 1) \\ & - P(C_{i+1} = 1) \middle| (A_i = 0 \cap B_i = 0)\big) \\ & \times P(A_i = 0 \cap B_i = 0)] \times 2^i \end{aligned} \quad (10)$$

Therefore, in the same way, the conditional probabilities of the proposed RCPFAs are obtained as follows.

RCPFA-I

$$\begin{aligned} C_i &= F_i\overline{\left(\overline{C_{i+1}}(A_i + B_i)\right)} + \overline{\left(\overline{C_{i+1}}(A_i B_i)\right)} \\ & P\left(C_{i+1} = 0 \middle| (A_i = 1 \cap B_i = 1)\right) \\ & = \frac{1}{3} - \frac{4^i}{3 \times 4^{n-1}} \\ & P(C_{i+1} = 1) \middle| (A_i = 0 \cap B_i = 0)\big) \\ & = \frac{1}{3} - \frac{4^i}{3 \times 4^{n-1}} \quad i \in \{0,1, \dots, n-2\} \end{aligned} \quad (11)$$

RCPFA-II

$$\begin{aligned} C_i &= F_i\overline{\left(\overline{C_{i+1}}(A_i + B_i)\right)} \\ & P\left(C_{i+1} = 0 \middle| (A_i = 1 \cap B_i = 1)\right) \\ & = \frac{2}{3} - \frac{2 \times 4^i}{3 \times 4^{n-1}} \\ & P(C_{i+1} = 1) \middle| (A_i = 0 \cap B_i = 0)\big) \\ & = 0 \quad i \in \{0,1, \dots, n-2\} \end{aligned} \quad (12)$$

RCPFA-III

$$C_i = F_i\overline{\left(\overline{C_{i+1}}(A_iB_i)\right)}$$
$$P\left(C_{i+1} = 0 \middle| (A_i = 1 \cap B_i = 1)\right) = 0$$
$$P\left(C_{i+1} = 1 \middle| (A_i = 0 \cap B_i = 0)\right) = \frac{2}{3} - \frac{2\times4^i}{3\times4^{n-1}} \quad i \in \{0,1,\dots,n-2\} \tag{13}$$

To obtain analytical expressions for the mean errors, the following theorems may be utilized.

III. RESULTS AND DISCUSSION

The simulations were performed with the supply voltage V_{dd} = 1.2 V and frequency of 100MHz. A comparison is included with existing or already reported designs, which demonstrates the benefit of the proposed 1-bit adders, good power delay product.

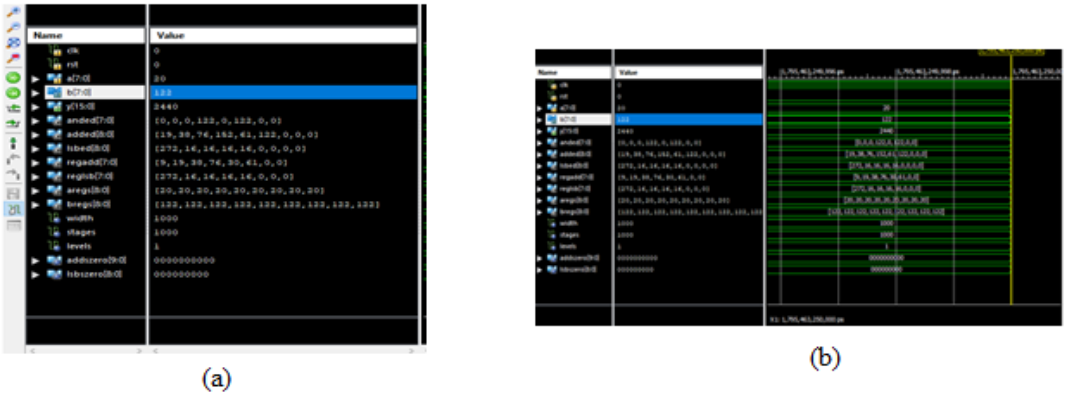

Figure: 3 (a) and (b) Simulation results

Figure 3 (a) and (b) shows the output waveform of proposed adder where it performed addition of 16 bit input data of a b c and c_{in} and gives the output.

Table 1 Comparison Table

Adders	Power	Delay	Area	Speed	EDP
CS3A	5.065	13.341ns	8.29	74.541mhz	5.780
FA	4.375	13.203 ns	7.224	75.744mhz	4.272
RCPFA I	5.521	12.731 ns	6.846	81.442mhz	4.092
RCPFA II	1.948	10.46 ns	5.705	92.32mhz	1.284
RCPFA II	3.542	10.461 ns	5.705	95.59mhz	1.896

The above table displays the comparison table of previously used different adders implemented with power, delay, Area, Speed and EDP of the adders.

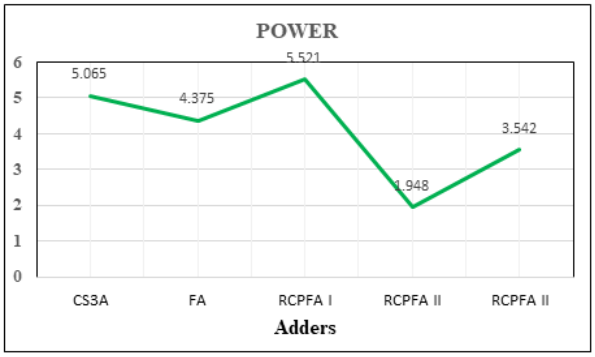

Figure: 4 Power of Adders

The above figure 4 displays the chart of power for different adders.

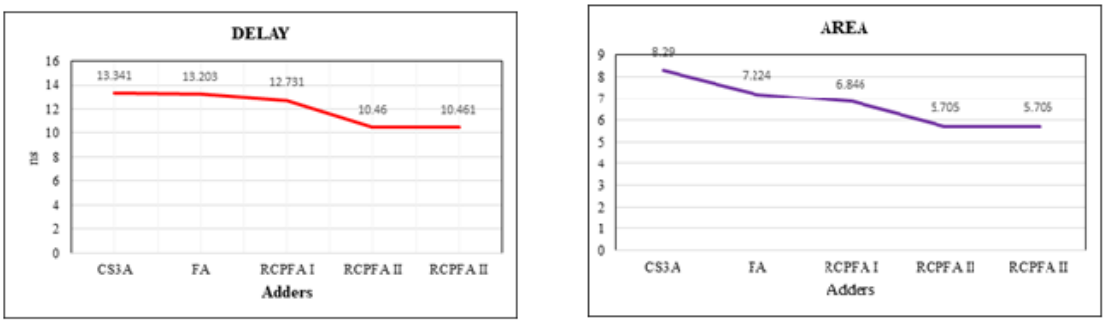

Figure: 5 (a) and (b) Delay of Adders

The above figure 5 (a) and (b) shows the delay for the different type of adders implemented.

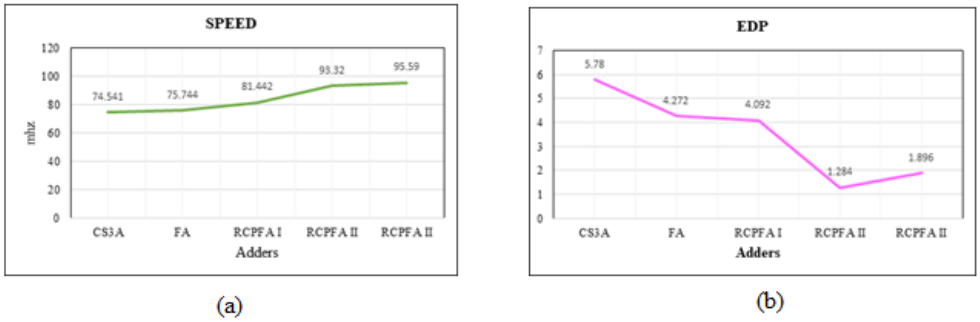

Figure: 6 (a) Speed of Adders and (b) EDP of adders

Figure 6 (a) and (b) displays the speed of the previously implemented adders.

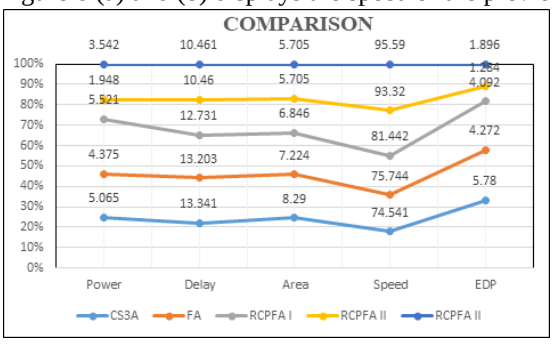

Figure: 8 Comparison Chart of Adders

Figure 8 displays the comparison chart of the implemented adders. Among all the full adder circuits, proposed full adder 1 has a minimum PDP, which proved significantly improved 52% with respect to CMOS & CPL implementations, 57% with respect to branch-based logic-pass transistor implementation and 62% with respect to TFA & TGA circuits.

IV. CONCLUSION

According to the research presented in this paper, utilising an approximate adder design style allows the designer more flexibility to choose different circuit modules depending on the application. In this study, RCPFA adders are suggested, and the design is expanded to include the 8-bit case. Because of the new design modules suggested in this article, the simulation results demonstrate that proposed hybrid full adder circuits perform better than most traditional full-adder cells with a supply voltage ranging from 1.0 V to 2.4 V in terms of power, delay and PDP. The new approximate full adder being suggested exceeds all others in terms of power, speed and energy saved (PDP). More stability in delay variation is offered by reverse carry propagation. The effectiveness of the suggested approximate FAs and the hybrid adders which implemented them have been researched. With a reverse carry propagate adder, the first filter is implemented. As a result, it continues to be one of the greatest options for creating big arithmetic circuits with little increase in area as well as minimal power and energy usage.

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