Fiber Optic Designs for Lidar Receiver and Its Signal Analysis Using Time-to-Digital Converter (TDC)

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Abstract-With the development of artificial intelligence, LiDAR finds significant applications in robotics and autonomous driving. Aiming at increasing the compactness and the integration of 2-D LiDAR, this work presents a highly digitally integrated 2-D LiDAR system implemented in a low-cost FPGA. The system is made of off-the-shelf components to limit the cost to USD 100. A laser transceiver with a symmetrical transmitting and receiving lens emits and collects laser pulses to range distance using the time-of-flight (ToF) method. As a key component in ToF, the FPGA-based time-to-digital converter (TDC) is adopted for counting the round-trip time of pulses, which is implemented in a low-cost FPGA of ZYNQ7010 with limited resources. The symmetrical structure of the delay line is used to design a more efficient TDC. The FPGA-TDC enables flexibility of design and integration with more functional logics and is microcontroller-free. All the digital logics including data processing and controlling are integrated into an FPGA with the TDC logics to realize fully digital integration and compact dimensions. The utilization of the whole architecture in the FPGA is about 15%. The experimental results demonstrated that the ranging accuracy of the LiDAR is about 2 cm, which is suitable for consumer electronics.

Keywords: LiDAR, FPGA, time-of-flight (ToF), time-to-digital converter (TDC)

1.INTRODUCTION

LiDAR is an acronym for light detection and ranging, which is the optical analog of radar. As an active sensor acquiring surrounding 3D information, LiDAR occupies key positions in remote sensing, defense, and autonomous driving [1–5]. A LiDAR generally consists of three key modules: transmitting, beam steering, and receiving modules. It obtains the distance of targets by illuminating laser signals at specific wavelengths on targets, and it obtains further 3D information by scanning the surface of the target in a mechanical or electromagnetic manner. Depending on different ranging principles, laser beams are modulated in time, frequency, or amplitude [6–9]. The ToF ranging principle that modulates laser beams in the time domain is a widely used distance measurement manner for LiDAR. The emitter illuminates a laser pulse to a target, and the receiver collects the reflected laser pulse. The ToF method measures distance by counting the round-trip flight time of emitted laser pulses between the LiDAR and the target. Timing is the key to distance measurement for a ToF LiDAR; its accuracy is crucial to the ranging accuracy of the LiDAR [10]. To reach accurate timing, a TDC is adopted to measure the time interval between the emission and the arrival of laser pulses.

In this work, we aim to demonstrate a fully FPGA-controlled and -processed low-cost digitally integrated LiDAR together with TDC implemented in a low-end FPGA chip with limited configurable logic block resource. For a LiDAR system, multiple MCU and ASIC chips are required to realize the control and processing functions of a 2-D LiDAR, including pulse control, motor control, ToF calculation, and data processing. With the capability of parallel and concurrent processing, an FPGA can realize high-speed computation in the form of a relatively low-cost coprocessor. This work integrates all logic functions of a 2-D LiDAR in a single low-end FPGA. Through the digital synthesis technique, the FPGA generates the narrow pulse to trigger the laser. The FPGA-TDC realizes the ToF calculation and eliminates wiring delay. To reduce the complexity of the timing architecture and the resource utilization in FPGA-based LiDAR, a lightweight architecture of the tapped delay line was adopted to realize the TDC for ToF measurement.

2. LITERATURE SURVEY

The All-Digital Phase Locked Loop (ADPLL) consists of full digital components which are used in advanced communication systems like frequency synthesizer, Carrier and clock recovery, modulator/demodulator etc. Hence the performance analysis of ADPLL becomes very necessary when designing these equipment's. The ADPLL contains phase detector, loop filter and digital controlled oscillator. The performance of ADPLL depends on various factors like combination of different components, power consumption, frequency resolution, jitter performance and locking speed etc. At present, the different combinations of components ADPLL are used to achieve fine resolution and fast lock-in time and it is appropriate for system-on chip applications. In this work the effects of various combinations of the internal components on the important parameters of ADPLL like frequency range, power and algorithms used have been compared.

This chapter presents the literature survey on the work carried out. Phase-locked loops were explained by semiconductor technology provides a powerful means for implementation of analog, digital and mixed signal circuits for high speed systems. The high speed systems, in turn depend on the clock generator circuits. A survey on the different types of phase locked loop architectures which can be used as a clock generator is carried out.

2.1 PROBLEM STATEMENT

From the review of PLL low power based converter architecture and methods in the literature part, the following issues are identified:

- However, the adjustment of PLL parameters impacts explicitly the effectiveness of the PLL.
- The PLL switches more often than working in a settled recurrence and alteration speed. After the reconfiguration of the direction reserve memory, for instance, the PLL can be distinctly insufficient, dispersing extra power or turning into a core bottleneck.
- The methods perform path finding in all the region of the network which increases the power in the hearts.
- The path finding time is higher and increases the overall latency. The power consumption increases due to retransmission and path finding reduce the lifetime of the network.

2.2 OBJECTIVES

- Moreover, by providing an easily extendable and flexible FPGA-based solution, multiple other sensors can be easily integrated within the platform with a low impact on energy consumption and computational cost due to the inherent parallelization of the HDL-based design.
- Therefore, the main CPU that runs mapping and localization or other algorithms can be freed from the load of reading data from multiple channels.

3. PROPOSED SYSTEM

3.1 FUNCTION OF PROPOSED SYSTEM

In this proposed work, the detailed power utilization of various segments in the TDC is investigated utilizing fast clocking strategy. Figure 3.1 demonstrates the block diagram of recommended ADPLL configuration. Time-to-digital converter is a crucial block used as the phase/frequency finder in an all-digital phase-locked loop. Phase frequency detector identified the phase and frequency confuse of the reference clock and isolated DCO clock. A feedback loop in the time field by the modeling TDC and DCO as an essential model in the state-space frame has proposed. At that point, a Model Prescient Control (MPC) technique for planning loop channel to make an ideal control signal is utilized.

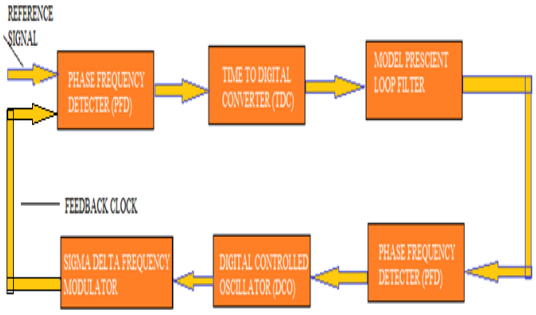

Figure 3.1. Block Diagram of the Proposed System

The proposed loop filter can defeat latency issue that exists in a significant portion of digital frameworks. Besides, the proposed MPC loop filter performs quick transient reaction time and empowers us to model other commotion sources came about because of oscillator pulling and glimmer clamor which is

fundamental issues in numerous new handsets and the impacts of which can be dramatically expelled without lessening the overall phase clamor execution. The simulation comes about affirm the capacity of the proposed plan and how it is fundamentally more power against these issues contrasted with ordinary digital PLL. The principal components and their execution will be examined in the accompanying segments.

3.2 Digital Phase/Frequency Detector:

The phase frequency detector is an essential part of the PLL because it decides if the reference clock and partitioned DCO check are in phase and are running at the identical rate. An altered D flip-flop was utilized because the D input doesn't change and stays high dependably. The yield of the changed D flip-flops enters a two-input NOR entryway that resets the flip-flops if the two timekeepers are high. The here and their signals demonstrate if the DCO clock should be expanded (up is valid) or diminished (down is accurate). The occasion and direction signal is essential to make them here and there empower signals for the TDC. Extra circuitry between the PFD and T2D is required for the signal change to happen. The block diagram of phase frequency detector appears in Figure 3.2.

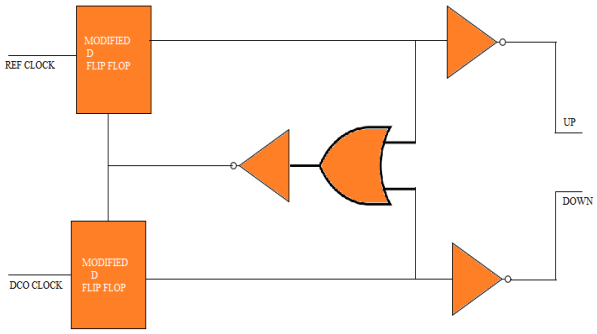

Figure 3.2. Block diagram of Phase Frequency Detector

Phase frequency detector is an asynchronous sequential logic circuit that keeps a "false bolt" condition. On the off chance that the Phase mistake is small, at that point, short yield beats are created. The underneath figure 3.3 shows the phase frequency detector schematic diagram utilizing Tanner EDA software

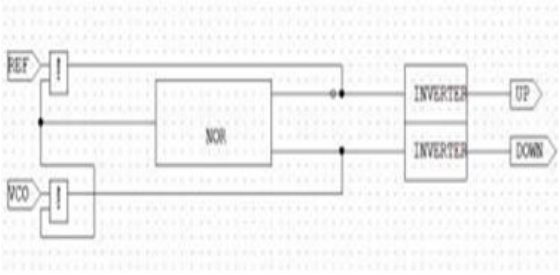

Figure 3.3. Phase frequency detector tanner design

3.3 Parallel Time to Digital Converter:

Time-to-digital converters unquestionably most architects interface this articulation with all-digital phase-locked loops where a TDC fills in as a phase detector. The time to digital converter has a 6 bit down counter, 6 bit up counter, and 6 bit convey swell adder. The phase detector controls the up counter and down counter by up and down actuating signals. The starting condition of the down counters is "111111', and up counter "000000". The up counter and down counter esteems are contributions to the six-piece adder, and the yield delivers the seven-piece control word for the DCO. The underneath given figure demonstrates the associations of the T2D converter. The six bits from the adder and the complete piece make the seven-piece control word. The converter ought to be empowered just if there is a phase and frequency crisscross. The underneath figure 3.4 exhibits the time to digital converter schematic diagram utilizing tanner EDA software.

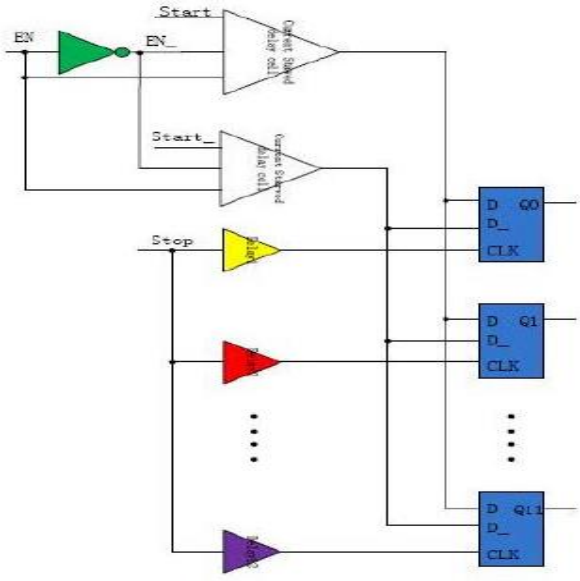

Figure 3.4. Time to digital converter tanner EDA design

3.4 Model Prescient Loop Filter:

In MPC the control goals are converted into an optimization issue, which is figured over a limited forecast skyline. The aftereffect of the optimization is an arrangement of ideal control moves which drive framework states towards a given reference point while thinking about framework requirements, (for example, upper and lower restrains on the data sources and countries) and enhancing a chose execution rule MPC controller is to drive the yield as near the set-point as conceivable in a minimum squares sense with the likelihood of the incorporation of a punishment term on the info moves. In this way, the controlled factors are limited a quadratic target work that can be viewed as the minimization of future blunders and control exertion. The accompanying Figure 3.5 appeared in a block diagram of the model prescient loop filter and Figure 3.6 show the schematic diagram of model prescient loop filter utilizing tanner EDA outline.

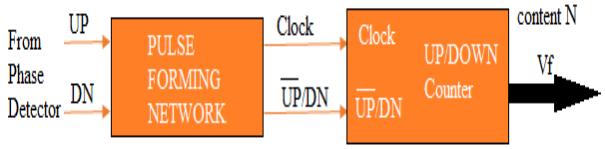

Figure 3.5. Model prescient loop filter block diagram

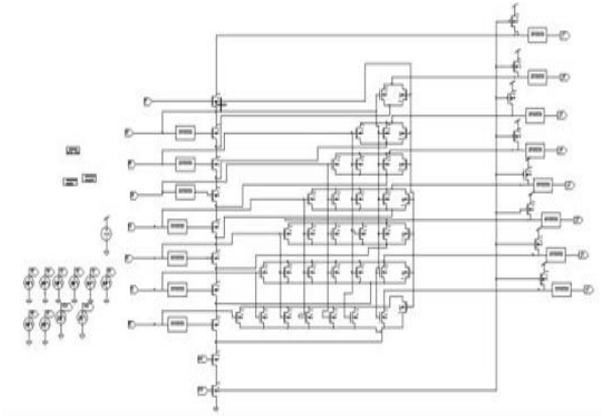

Figure 3.6: Model prescient loop filter tanner EDA design

3.5 Digitally Controlled Oscillator:

The controlled oscillator is a primary material in PLL, which is a substitution of the average voltage or current controlled oscillator in the all-digital PLL. They are more adaptable and usually much robust than the conventional VCO. Moreover, the planned trade-off for the frequency picks up in voltage, or current controlled oscillator isn't essential for DCOs because the invulnerability of their control input is high. In this work, DCO was actualized logically. The schematic diagram of DCO appears in figure 3.7. The oscillator produces a yield waveform having high and low heartbeats whose pulse width has decided by the control word from the decoder.

Figure 3.7: Schematic diagram of DCO

The underneath Figure 3.8 shows tanner EDA configuration diagram of DCO. Increment and Decrement (ID) counter is utilized for DCO in this plan. It has three information sources: a clock info, augmentation and decrement. At the point when there is no conveyor get beat; the ID counter gives yield beat on consistently ID clock. At the end when a convey beat shows up at the INC input then the next ID beat is progressed in time by one ID clock period, and when get hit shows up at the DEC input then the next ID beat is postponed in time by one ID clock period.

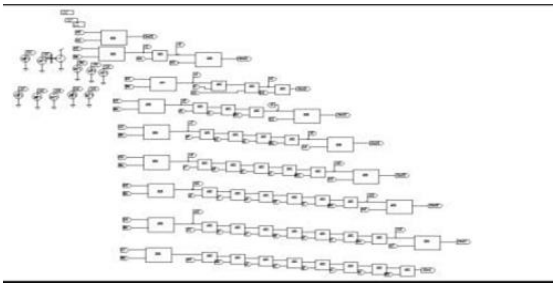

Figure 3.8: DCO increment and decrement counter tanner design

3.6 Sigma Delta Modulator Based Frequency Divider:

In this work, a first-order sigma-delta modulator is used instead of frequency divider part, and sigma-delta modulator just functions as a signal shaping circuit. Here output from the DCO is directly given to the modulator whose output has provided to the phase frequency detector. This correction in the phase locked loop circuit is done to make it more energy efficient and to produce fast lock time. The first step in a delta-sigma modulation. In delta modulation, the difference in the signal (its delta) is encoded, rather than the absolute value. The result is a stream of pulses, as opposed to a stream of numbers as is the case with

PCM. In delta-sigma modulation, the accuracy of the sound is improved by passing the digital output through a 1-bit DAC and adding (sigma) the resulting analog signal to the input signal, thereby reducing the error introduced by the delta-modulation.

4. SIMULATION RESULTS AND DISCUSSION

The proposed ADPLL is composed of using tanner EDA tool V14.1. This takes a gander at the power for various outlines of all digital phase locked loop with the proposed design. Here the simulation comes about come to fruition are gained for particular data close yield ADPLL. Following figures demonstrates the simulation results used to assess the proficiency of the proposed strategies

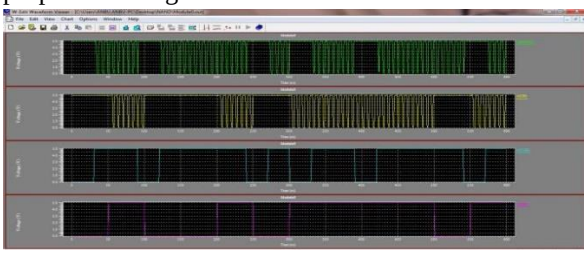

Figure 4.1. PFD simulation result

The above mentioned Figure 4.1 shows output waveform of the phase frequency detector in proposed ADPLL using tanner EDA.V 14.1

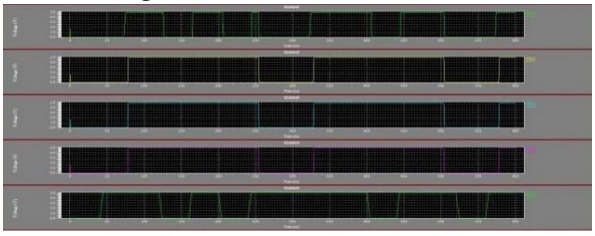

Figure 4.2: TDC simulation result

The above mentioned Figure 4.2 shows output waveform of the time to digital converter in proposed ADPLL using tanner EDA.V14.1

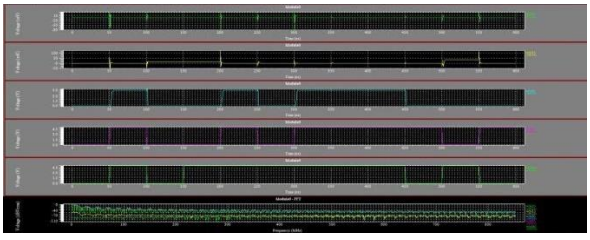

Figure 4.3: Model Prescient Loop filter simulation result

The above-mentioned figure 4.3 shows output waveform of the model prescient control loop filter in proposed ADPLL using tanner EDA.V 14.1

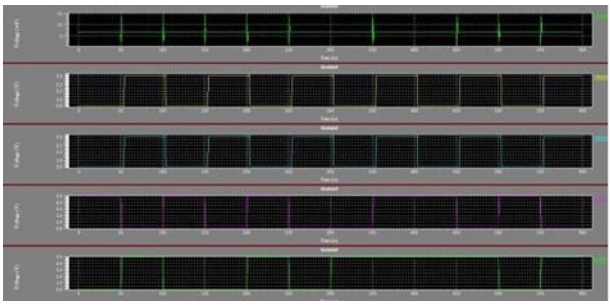

Figure 4.4: DCO simulation result

The above-mentioned Figure 4.4 shows output waveform of Digital Controller Oscillator in proposed ADPLL using tanner EDA.V 14.1

5. CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

In summary, a digitally integrated 2-D LiDAR system is implemented in a low-end FPGA together with a lightweight and resource-saving TDC based on a symmetrical tapped delay line. The LiDAR employs the ToF ranging method to measure distance. It is built with a homemade transceiver and a mechanical scanning structure with off-the-shelf components. To achieve high digital integration and compact dimensions, the LiDAR system integrates timing, controlling, and data processing logics together in ZYNQ7010 without the need for an MCU. Owing to the lightweight architecture, the average resource utilization of the whole architecture in the ZYNQ7010 is 15%. The scanning results of different targets with complex profiles prove that the ranging of the LiDAR and the timing of the TDC operate well and steadily. This structure greatly reduces the cost and dimensions of LiDAR, which would be of significance in consuming applications.

5.2 FUTURE WORK

Moreover, with low cost and high integration, in future the proposed digitally integrated LiDAR would find potential applications in smart cities, including robotic navigation, real-time pedestrian counting, truck overload monitoring, social distance detection, and traffic monitoring applications.

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