

Design and Analysis of sub-threshold base bridge style 64-bit Ripple Carry Adder at 32nm technology

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Abstract- A low power 64-bit ripple carry adder cells based on Sub-threshold logic is designed in this paper. Five different sub-thresholds based 64-bit ripple carry adders namely Bridge style (Bridge_V1, Bridge_V2, Bridge_V3), C/CMOS and LP adders are designed by using these different techniques. To compare these adders we have performed various simulations using HSPICE in a 32 nanometer (nm) standard CMOS technology at room temperature; with supply voltage variation from 200mV to 350mV with 50mV steps. Different performance parameters of the adder including average power, delay, Power-delay Product and noise margin are investigated. The best 64-bit ripple carry adder with the smallest power and power-delay product and the highest achievable frequency is determined. Simulations results show that 64-bit Bridge style Ripple carry adder using 32 nm technologies (Bridge_V2, Bridge_V3) gives better performance at frequency 20MHz, with supply voltage 250mV.

Index Terms- CMOS Circuit, VLSI, Sub-threshold region, full adder and low power.

1. INTRODUCTION

CMOS VLSI designs have been evolving into fast, cheap, low voltage and low power regimes. VLSI design has been focusing high performance for microprocessor and system component. CMOS VLSI circuits has been identified as a critical technological need in the recent years due to the high demand for low power consumption, lower delay, small area and low cost designs are increasing every day. In VLSI applications, arithmetic operations play an important role. Commonly used operations are addition, subtraction, multiplication and accumulation. Adder is one of the most important components of a CPU (central processing unit), Arithmetic logic unit (ALU), floating point unit and address generation like cache or memory access unit use it. In addition, adders are important components in other applications such as digital signal processors (DSP) architectures, microprocessors, and microcontroller and data processing units. Arithmetic functions such as addition, subtraction, multiplication and division are some examples, which use adder as a main building block [8]. The Role of Binary Adders in Microprocessors addition of two binary numbers is the fundamental and most often used arithmetic operation on microprocessors, and data-processing

application-specific integrated circuits (ASIC). Therefore, binary adders are main building blocks in very large-scale integrated (VLSI) circuits. Adders often appear in the integer execution unit, and sometimes in the address generation path. If a floating-point unit is present they appear in the significant adder, at the base of multiplier array, and in the divider. In electronic applications adders are most widely used. Due to device portability miniaturization of device, the adders must have high speed, lesser area and lower power consumption. Devices like Mobile, Laptops etc. require more battery backup. So, a VLSI designer has to optimize these three parameters in a design. Basically full Adder is one of the core components of microprocessor and other complex chips. So the performance of full adder would affect the system as a whole. Basically there are various types of full adders. But due to the superior speed and low power consumption bridge style full adders are used to design 64-bit RC Adder. Bridge style full adder design in sub-threshold region [2].

II. SUB-THRESHOLD VOLTAGE DESIGN

In the sub-threshold region, the supply voltage (V_{dd}) is less than the transistor threshold voltage (V_{th}). The operating current in the sub-threshold region is [6,7]

$$I_{DS} = I_S e^{\frac{V_{GS} + nV_{DS} - V_{th}}{nV_T}} (1 - e^{-\frac{V_{DS}}{V_T}}) \quad (1)$$

Where

$$I_S = u_n C_{ox} \frac{W}{L} (n-1) (V_{th})^2 \quad (2)$$

The parameters in (1) and (2) are defined as:
V_T = Thermal voltage ((KT / Q) = 26 mV at 300°K)

K = Boltzmann's constant (1.38 × 10⁻²³ J/K)

Q = electronic charge (1.602 × 10⁻¹⁹ C)

T = temperature

n = The sub-threshold slope parameter (n = 1 + C_{dep}/C_{ox})

μ_{n(p)} = The carrier mobility for n-(p-) channel device.

C_{ox} = The oxide capacitance.

C_{dep} = The depletion capacitance.

L = The Length of the channel.

W = Effective width of the channel.

This current is the leakage current which limit the maximum circuit performance, but because of using lower supply voltage, a circuit operating in sub threshold region consumes less power than the circuits which biased in strong inversion region. In sub-threshold designs, the sub-threshold current is used for necessary computation, providing a near ideal voltage transfer characteristics of the logic gates. Its impact on system design is an exponential reduction of power at the cost of performance degradation, in the sub-Vt region, as shown in the above Equations 1-2, the drain current I_{ds} is exponentially related to the gate voltage V_{gs} . This exponential relationship is expected to give an exponential reduction in power consumption, also an exponential increase in delay. In sub-threshold region, the reduction in power consumption outweighs the increase in delay. Thus the circuit has lower PDP when it operates in sub-threshold region. So in the same frequency, when the circuit operates in sub-threshold region, its energy consumption is less than when it exploit in supper-threshold. The adder is one of most commonly elements in many VLSI systems. Arithmetic operations such as addition, subtraction and multiplication. Thus, lowering the power consumption the adders is an important design objective for low power digital designs. One of the best methods of reducing full adder power consumption is obtained by using sub-threshold style design. Some different designs of 1-bit full adder cell operating in sub-threshold region have been proposed.

A. Applications Of Sub-Threshold Logic Design Structures

Sub-threshold digital circuits will be suitable only for specific applications which do not need high performance, but require extremely low power consumptions. This type of applications includes medical equipments such as hearing aids and pace-maker, wearable wrist-watch computation, and self-powered devices [3]. Sub-threshold circuits can also be applied to applications with bursts characteristics in which the circuits remain idle for an extended period of time.

III. A REVIEW ON FULL ADDER AND 64-BIT RC ADDER DESIGN

We have designed various 1-bit full Adder at sub-threshold region in order to design 64-bit ripple carry adder. 1-bit full Adders are Bridge style adder (Bridge_V1, Bridge_V2, and Bridge_V3), C/CMOS adder and Low Power adder. Some of these adders are based on CMOS logic with low power

consumption, good signal logic level, high driving ability and high noise margin. Other design is based on combination of CMOS and Pass transistors. All these adders are simulated simulations using HSPICE in a 32 nanometer (nm) standard CMOS technology at supply voltage variation from 200mV to 350mV with 50mV steps and different frequency like 5MHz, 10MHz, and 20MHz.

A. 1-BIT C/CMOS Full Adder

A basic cell in digital computing systems is the 1-bit full adder which has three 1-bit inputs (A, B, and C_{in}) and two 1-bit outputs (sum and carry).

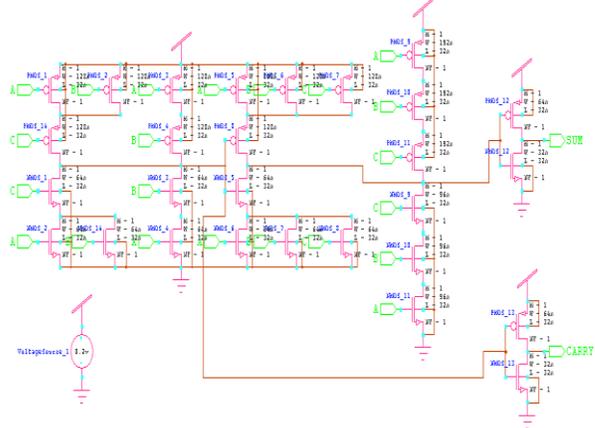


Figure 1:-Conventional CMOS FA Design

The relations between the inputs and the outputs are expressed as:

$$\text{Sum} = (A \text{ xor } B) \text{ xor } C_{in}$$

$$\text{Carry} = A \text{ and } B + C_{in} (A \text{ xor } B)$$

The 1-bit conventional CMOS full adder cell is shown in figure 1. The 1-bit full adder cell has 28 transistors. The CMOS structure combines PMOS pull-up and NMOS pull-down networks to produce considered outputs. In this style all transistors (either PMOS or NMOS) are arranged in completely separate branches, each may consist of several sub-branches. Mutually exclusiveness of pull-up and pull-down networks is of a great concern. Figure1. shows the conventional CMOS 28- transistor adder [4,6].

B. Bridge Style CMOS Circuits

Bridge style (Bridge_V1) 1-bit full adder which is operating in sub-Vt region . This full adder can be divided into two modules: sum module and carry module. Equations (1) and (2) show the logical functions of the full adder outputs

$$\text{Sum} = (A \text{ xor } B) \text{ xor } C \tag{1}$$

$$\text{Carry} = A \text{ and } B + C (A \text{ xor } B) \tag{2}$$

Based on equation (1) & (2) three implementation of full adder with bridge design are investigated. The Bridge_V1 full adder for Sum is show in figure 2. and Bridge_V1 full adder for Carry is show in figure 3. Bridge_V1 full adder design has more transistors against conventional CMOS full adder and should

have complementary inputs, so six transistors for inverting inputs are needed so bigger area is required for this design.

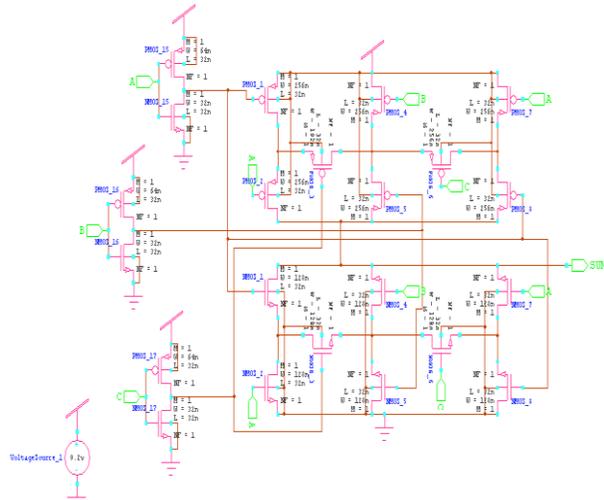


Figure 2:-Bridge_V1 FA Design for Sum

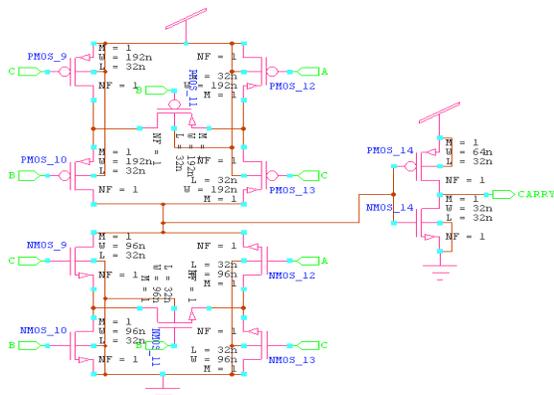


Figure 3:-Bridge_V1 FA Design for Carry

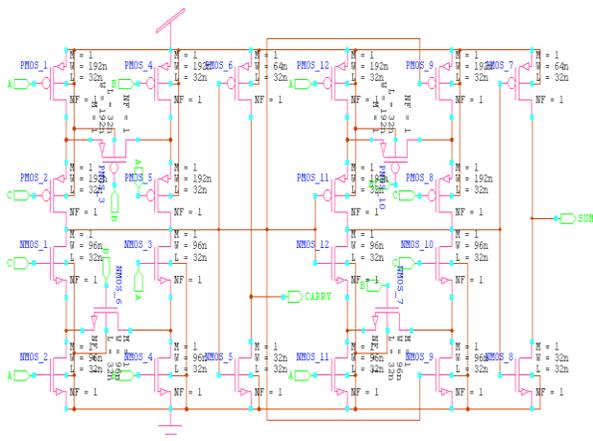


Figure 4:- Bridge_V2 Full Adder Design

Bridge_V2 full adder is shown in figure 4. It shares the path between carry and sum circuits with fully symmetric full adder structure. The area of Bridge_V2 full adder is about 5% less than conventional CMOS full adder but its delay is higher than conventional CMOS full adder in other side power consumption is lower so for solving delay problem, the carry part of the Bridge_V2 full adder design replaced with carry generator of the Conventional CMOS full adder in Bridge_V3 full adder [6]. Figure 5. Shows the Bridge_V3 full adder design.

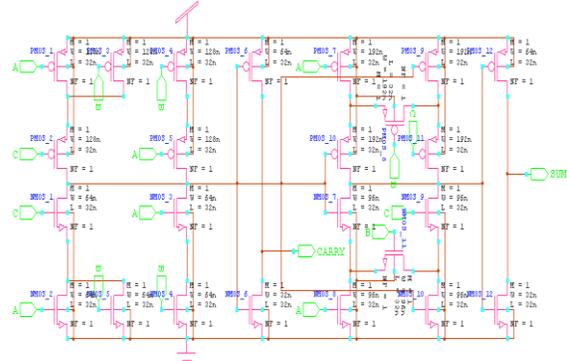


Figure 5:- Bridge_V3 Full Adder Design

C. Low Power Full Adder Design

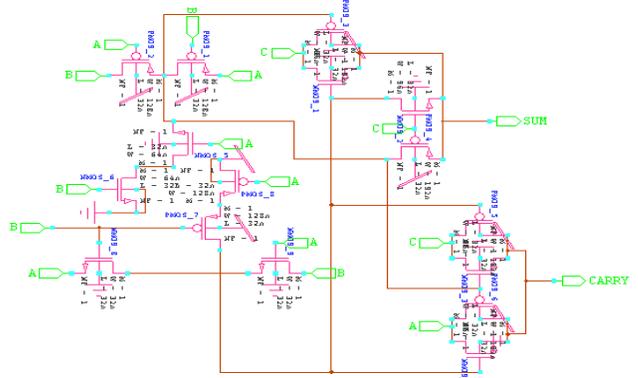


Figure 6:- Low Power Full Adder

Low Power full adder circuit that is designed by pass transistors and transmission gates for low power consumption [6]. Low Power full adder design is shown in Figure 6.

D. 64-bit Ripple Carry Adder design

64-bit ripple carry adder is designed by cascading full adder in series. In the ripple carry adder a carry from previous full adder is connected as input carry for the next stage. Full adder is a basic building block of Ripple carry adder. Therefore, to design 64-bit ripple carry adder, it requires 64 full adders. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full

adder. The 64-bit ripple carry full adders design is shown figure 7. In this way we have designed five different 64-bit ripple carry adder by using 1-bit full adder like Bridge_V1, Bridge_V2, Bridge_V3, C/CMOS and Low Power Adder [1].



Figure 7:- 64-Bit Ripple Carry Adder

IV. SIMULATION RESULTS

As we have designed various 1-bit full adder like Bridge styles full adder (Bridge_V1, Bridge_V2, Bridge_V3) C/CMOS full adder and low power full adder in order to design 64-bit ripple carry adder. After designing all these adder simulated results are performed using HSPICE in a 32 nanometer (nm) standard CMOS technology at supply voltage variation from 200mV to 350mV with 50mV steps and different frequency like 5MHz, 10MHz, and 20MHz.

A. Simulated Results of Different 64-Bit RC Adder Designs:-

Table 1. Analyses of different 64-bit RCA Vdd=200mV,f=5MHz, Input=A63,B63, C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	1.018	7.68	7.824	193.89	4.75
B_V2	0.752	9.00	6.773	197.94	2.94
B_V3	0.717	9.03	6.481	198.16	2.16
CCMOS	0.606	8.75	5.302	196.14	2.85
LP	0.166	2.54	0.423	195.80	2.19

Table 2. Analyses of different 64-bit RCA Vdd=200mV,f=10MH,Input= A63,B63,C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	0.9448	20.21	19.09	192.64	4.35
B_V2	0.6922	14.58	10.09	197.44	2.14
B_V3	0.6551	9.94	6.511	197.86	1.86
CCMOS	0.5451	9.66	5.265	196.64	2.45

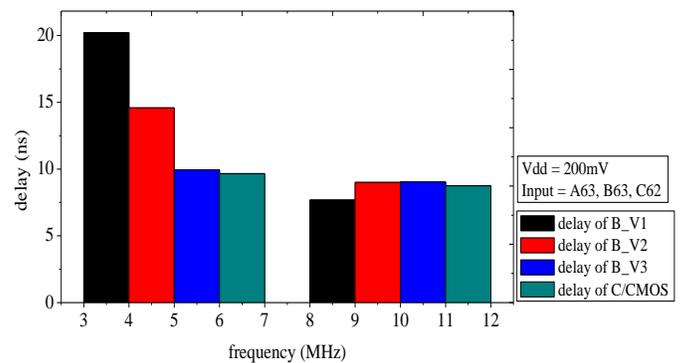


Figure 8:- Delay for Sum of 64-bit RC Adder at frequencies 5MHz and 10MHz

When we Compare different 64-bit ripple carry adders designs at frequency 5MHz, Vdd = 200mV, we find that the Bridge_V3 & C/CMOS adder has least and equal delays which is approximately 9.94ns (Bridge_V3), 9.66ns (C/CMOS) for last input (A63, B63, C62) respectively as compare to Bridge_V1 & Bridge_V2 adder as shown in the table 1.

At frequency 10 MHz, Vdd = 200mV, we find that the LP adder has least delays which is approximately 2.54ns for last input (A63, B63, C62) respectively as compare to Bridge_V1, Bridge_V2, Bridge_V3 & CCMOS adder as shown in the table 2. At frequency 20 MHz, Vdd = 200mV it is observed that distorted output has come because at this point transistor is not going to be triggered for 64-bit ripple carry adder because of low voltage and high frequency.

Table 3. Analyses of different 64-bit RCA Vdd=250mV,f=5MHz,Input = A63,B63,C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	1.450	12.51	18.14	245.65	4.56

B_V2	1.028	9.30	9.562	248.53	1.67
B_V3	0.991	6.48	6.421	248.55	1.45
CCMOS	0.807	6.32	5.100	247.86	2.21

Table 4:- Analyses of different 64-bit RCA
Vdd=250mV,f=10MHz,Input=A63,B63,C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	1.596	4.66	7.438	246.75	3.46
B_V2	1.134	7.91	8.977	248.89	1.27
B_V3	1.099	9.36	10.29	248.85	1.48
CCMOS	0.917	9.09	8.347	247.12	2.45

Table 5:- Analyses of different 64-bit RCA
Vdd=250mV,f=20MHz,Input=A63,B63,C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	2.114	9.51	20.11	241.65	5.84
B_V2	1.586	7.28	11.54	247.68	1.86
B_V3	1.530	8.68	13.28	247.79	1.67
CCMOS	1.368	9.70	13.27	247.24	2.12

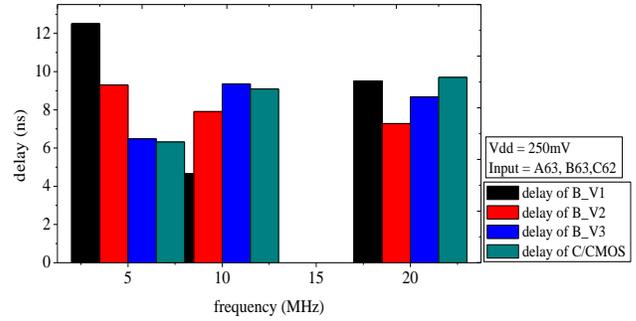


Figure 9:- Delay for Sum of 64-bit RCA at frequencies 5MHz, 10MHz and 20MHz

Comparison of different 64-bit ripple carry adders designs at frequency 5MHz, Vdd = 250mV it is found that the Bridge_V3 & C/CMOS has least delays which is approximately 6.48ns (Bridge_V3), 6.32ns (C/CMOS) for last input(A63, B63, C62) respectively as compare to Bridge_V1 & Bridge_V2 adder as shown in the table 3.

At frequency 10 MHz, Vdd = 250mV it is found that the Bridge_V1, has least delays which is approximately 4.66ns for last input(A63, B63, C62) respectively as compare to Bridge_V2, Bridge_V3 & C/CMOS adder as shown in the table 4.

At frequency 20 MHz Vdd = 250mV it is observed that Bridge_V2 works very well and it is also observed that it gives us least delay which is equals to 7.28ns for last input as shown in table 5.

Table 6:- Analyses of different 64-bit RCA
Vdd=300mV,f=5MHz,Input = A63,B63,C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	2.051	8.36	17.14	297.12	2.82
B_V2	1.431	6.53	9.349	299.27	0.88
B_V3	1.416	8.13	11.51	299.12	0.44
CCMOS	1.118	7.84	8.767	298.22	1.86

Table 7:- Analyses of different 64-bit RCA
Vdd=300mV,f=10MHz,Input = A63,B63,C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	2.27	6.79	15.42	297.67	2.82

B_V2	1.58	4.97	7.888	299.66	0.78
B_V3	1.57	6.55	10.29	299.72	0.64
CCMOS	1.28	6.37	8.157	298.82	1.66

Table 8:- Analyses of different 64-bit RCA
Vdd=300mV,f=20MHz,Input=A63,B63,C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	3.16	6.43	20.37	296.12	4.89
B_V2	2.30	4.29	9.881	299.39	0.84
B_V3	2.31	5.97	13.83	299.46	0.91
CCMOS	2.01	5.60	11.27	298.14	2.14

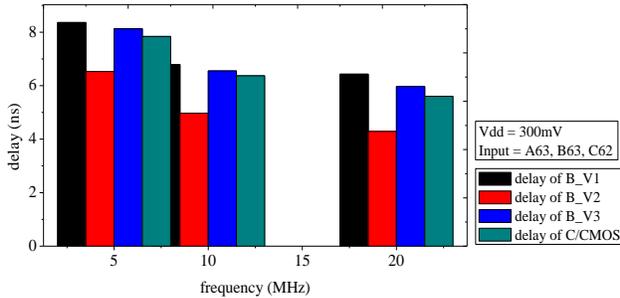


Figure 10:- Delay for Sum of 64-bit RCA at frequencies 5MHz, 10MHz and 20MHz

Comparison of different 64-bit ripple carry adders designs at frequency 5MHz, Vdd = 300mV it is found that the Bridge_V2 has least delays which is approximately 6.53ns for last input (A63, B63, C62).as shown in table 4.6.

At frequency 10 MHz, Vdd = 300mV it is found that the Bridge_V2 has least delays which is approximately 4.97ns for last input (A63,B63.C62) respectively as shown in table 4.7.

At frequency 20 MHz Vdd = 300mV it is observed that Bridge_V2 works very well and it is also observed that it gives us least delay of Sum and Carry for (A63, B63,C62) for last input as shown in table 4.8.

Table 9. Analyses of different 64-bit RCA
Vdd=350mV,f=5MHz,Input = A63,B63,C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	2.76	6.18	17.09	348.23	1.87
B_V2	1.92	5.29	10.16	348.95	0.77
B_V3	1.98	6.23	12.38	349.23	0.65
CCMOS	1.49	5.93	8.856	348.34	0.89

Table 10:- Analyses of different 64-bit RCA
Vdd=350mV,f=10MHz,Input =A63,B63,C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	3.066	4.52	13.86	348.23	1.87
B_V2	2.126	3.47	7.380	349.13	0.70
B_V3	2.183	4.36	9.519	349.73	0.25
CCMOS	1.709	4.26	7.283	348.64	0.79

Table 11. Analyses of different 64-bit RCA
Vdd=350mV,f=20MHz,Input=A63,B63,C62

Cells	Power (uw)	Delay (ns)	PDP (fJ)	V _{OH} (mV)	V _{OL} (mV)
B_V1	4.333	3.94	17.07	346.14	2.97
B_V2	3.134	2.68	8.399	349.12	0.74
B_V3	3.331	3.67	12.22	349.62	0.71
CCMOS	2.736	3.44	9.414	348.18	1.94

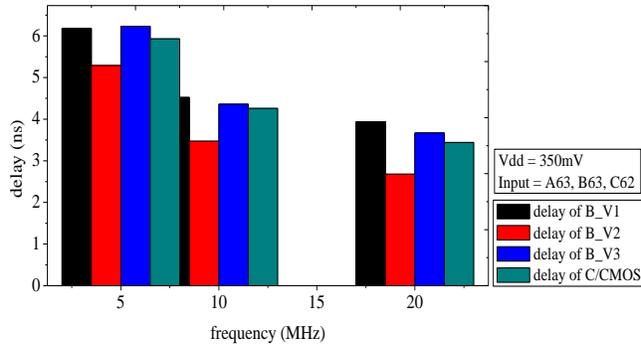


Figure 11:- Delay for Sum of 64-bit RCA at frequencies 5MHz, 10MHz and 20MHz

Comparison of different 64-bit ripple carry adders designs at frequency 5MHz, Vdd = 350mV it is found that the Bridge_V2 and has least delays which is approximately 5.29ns (Bridge_V2), for last input as shown in table 9.

At frequency 10 MHz, Vdd = 350mV the same results occurs as in case when frequency is 5 MHz i.e. Bridge_V2 has least delay which is approximately 3.47ns for last input (A63, B63, C62) as shown in table 10.

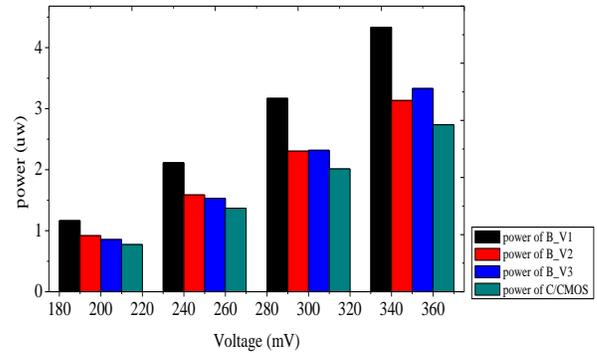
At frequency 20 MHz Vdd = 350mV it is observed that Bridge_V2 has least delays which equals to 2.68 ns for last input as shown in table 11.

- 64-bit ripple carry adder using bridge style techniques (B_V1, B_V2, B_V3), CCMOS adder and LP adder. All these ripple carry adder simulated by HSPICE in 32 nm CMOS process technology and different supply voltages 200mV, 250 mV, 300 mV, 350 mV and different frequency like 5MHz, 10MHz, and 20MHz in order to make comparison for better results. As base paper 1-bit adder (B_V1,B_V2,B_V3), CCMOS adder and LP adder are simulated.
- But when all these 64-bit ripple carry adder are simulated at frequency 20MHz, Vdd=200 mV it does not give desired results (Sum, Carry) because transistors are not triggered. But when we increase Vdd = 250mV up to 350mV which is under sub-threshold voltage (0.42252v) these adder gives proper results. The adders (B_V1, B_V2, B_V3), CCMOS operated at voltage Vdd=200mV, frequency 5MHz and 10MHz gives proper results.
- 64-bit Low Power ripple carry adder give proper results only at frequency 10MHz, Vdd=200mV to 350mV which is under sub-threshold voltage.
- Comparison of all adders are shown in above tables in terms of Power, Delay, PDP (Sum and Carry) which shows that all adders at 20 MHz operates with minimum 250mV, that means if

Vdd is below 250 mV transistors will not trigger for 64-bit ripple carry adders.

- LP-ADDER give proper output at frequency 10 MHz Vdd=200mV up to 350mV. It cannot give proper output at frequency 5 MHz and 20 MHz for 64 bit ripple carry adder.

B. Comparison of Power Consumption at Frequency 20mhz and Supply Voltage (Vdd = 200mV, 250mV, 300mV, 350mV)



Graphical illustrations of different 64-bit ripple carry adder results show that power consumption increase with increase in the supply voltage. But delays get decrease with increase in the supply voltage.

V. CONCLUSION

In this thesis we have presented work, low power 64-bit Ripple carry adder based on sub-threshold logic styles. Five different sub-thresholds based 64-bit ripple carry adders namely Bridge style (Bridge_V1, Bridge_V2, Bridge_V3), CCMOS and LP adders are designed by using different techniques. The study included the effect of changing the supply voltage, sizing of the transistors (W/L), frequency. To compare these adders we have performed various simulations using HSPICE in a 32 nanometer (nm) standard CMOS technology at room temperature; with supply voltage variation from 200mV to 350mV with 50mV steps and different frequency like 5MHz, 10MHz, and 20MHz. Different performance parameters of the adder including power, delay, Power-delay Product and noise margin are investigated. The best 64-bit ripple carry adder with the smallest power and power-delay product and the highest achievable frequency is determined. Simulations results show that 64-bit Bridge style ripple carry adder using 32 nm technology (bridge_V2,Bridge_V3) gives better improvement in power consumption and delay at frequency 20MHz,

V_{dd} = 250mV as compares to conventional adders, Bridge_V1 adder and LP adder.

VI. FUTURE SCOPE

Designers can further design the 128-bit ripple carry adders by using present design. Moreover, a slight improvement in, average power dissipation, and propagation delay, power delay product and noise margin can create huge impact on the overall performance. As different application can be generated using this different modules, designers should take a good look at the power consumption at different input voltage. Another important concern for designing circuits is leakage power and delay. Decrease of delay and low input voltage might have an impact on the speed of overall circuits. Due to this reason delay is another area where designer can work in future.

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