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QPSK MODULATOR BASED ON INJECTION LOCKED RING VCO IN 250nm CMOS

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Abstract **- In proposed design, a Quadrature phase shift keying modulator is implemented using injection locking for the phase modulation based on ring voltage controlled oscillator. The proposed design reduces the area of fabrication and power consumption of VCO, by eliminating the blocks in the traditional QPSK modulator and by using injection locking.**
The proposed QPSK modulator is implemented and simulated in 0.25µm with an output frequency of 1.1GHz. The total power consumption of proposed design is 13.1mw using a 2.5 volt supply.

Keywords:- Quadrature phase shift keying (QPSK), injection locking, ring voltage-controlled oscillator (VCO)

I. INTRODUCTION

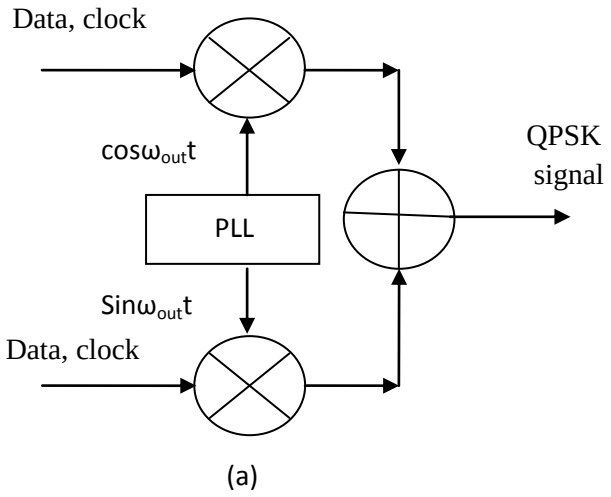
Injection locking is used widely in digital and analog communication for clock generation. Injection locking leads to decrease in phase noise of oscillators with a very simple circuit topology. This work proposes a injection locked QPSK modulator without using a conventional PLL. Injection locking is used for the purpose of phase modulation and phase locking.

As in conventional QPSK modulator, it contains a number of RF blocks like filters, mixers, charge pumps and phase frequency detectors etc. which requires large area and consumes more power to generate quadrature output.

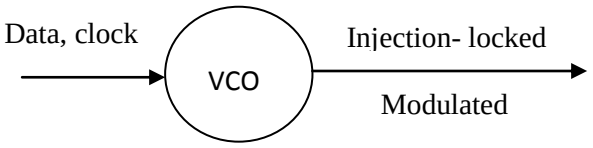
A PLL is a closed-loop feedback system that sets fixed phase relationship between its output clock phase and the phase of a reference clock. A PLL tracks the phase changes that are within the bandwidth of the PLL. A PLL also multiplies a low-frequency reference clock, to produce a high- frequency clock. A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals.

The overall goal of the PLL is to match the reference and feedback signals in phase, this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant.

By using a injection locking scheme, the need of PLL block and inductor for QPSK modulator have been eliminated
and a simple QPSK modulator can be achieved with minimum area requirement for fabrication. This paper proposes generation of accurate high frequency quadrature signal from a single phase input at the same frequency i.e. 90 degree phase difference and identical amplitude.fig1. shows the difference between conventional QPSK modulator and proposed modulator.



(a)



(b)

fig.1 (a) Block diagram of conventional QPSK modulator (b)Proposed direct injection locked QPSK modulator.

II. INJECTION LOCKED QPSK MODULATOR

In injection locked oscillator, an external source injects a signal with a frequency higher, lower or equal to the oscillator free running frequency. The oscillator locks onto the injected signal changing the free running frequency of the oscillator.

By using injection locking, phase locking and mixing can be achieved. In proposed paper phase locking and modulation are achieved by pulses from the clock and by using the data which is synchronized with the clock, respectively. The proposed work requires simple circuit topology and small area, since proposed QPSK modulator only uses a ring VCO with phase modulated injection pulse.

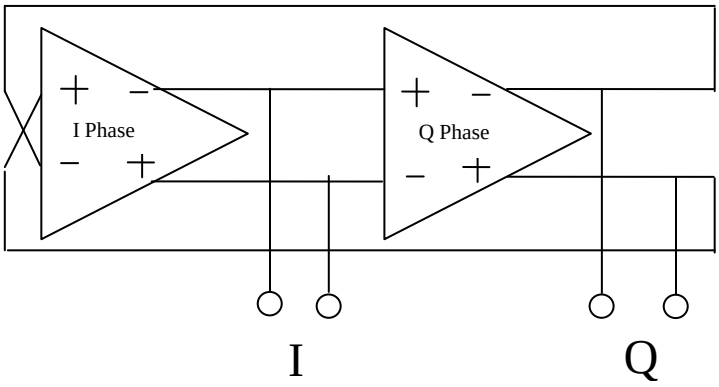


fig.2 Proposed two stage differential ring VCO

Fig 2. Shows the block diagram of proposed two stage quadrature ring VCO. The injection signal is generated by a xor gate or nand gate based pulser, which generates pulses of narrow width used as injection signal for locking. These pulses are injected to both the I phase and Q phase delay cell for injection locking. The width of pulses or injection signal can be controlled with the help of pulser.

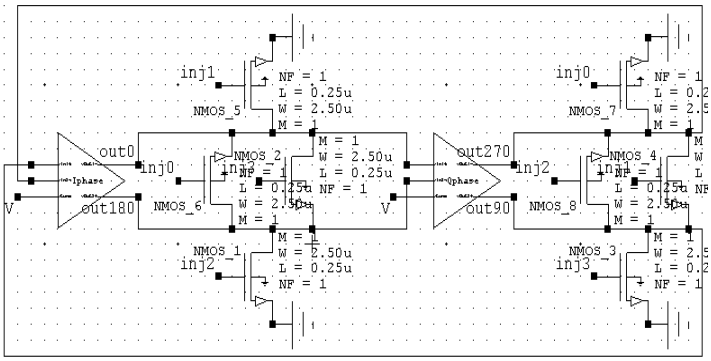
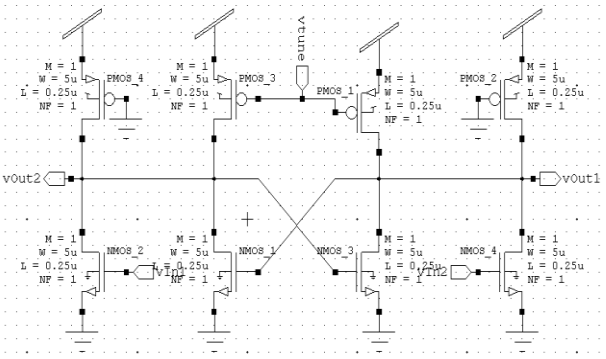


fig.3 proposed two stage ring vco using injection locking

Fig.4 shows the delay cell (I phase or Q phase) of proposed two stage ring VCO with two differential input vin1 and vin2 and two output, vout1 and vout2. In the proposed delay cell the positive feedback applied in the cell satisfies the oscillation condition and oscillates even with the I/Q pulse injection.

fig.4 Delay cell of differential ring vco

The output response of this delay cell by performing DC analysis on Tanner EDA tool is obtained as shown in figure5.



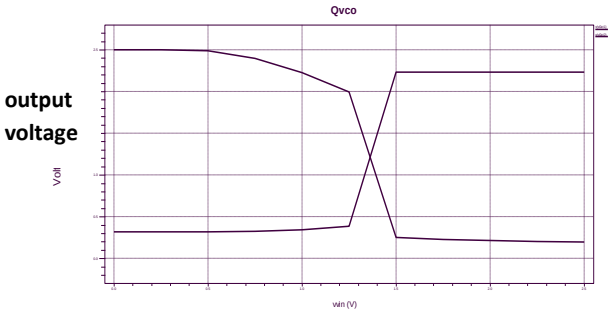


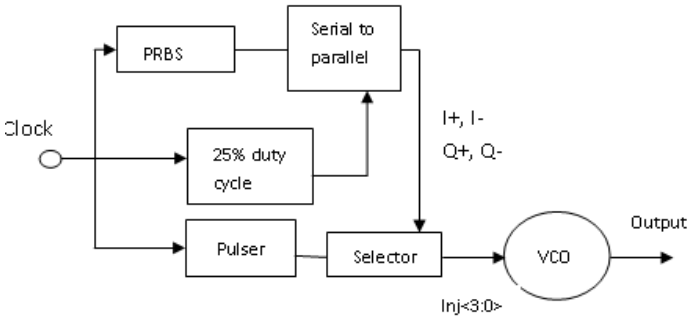
fig.5 DC characteristics of V_{in} cell

Fig.6 depicts the block diagram of proposed QPSK modulator. The PRBS block generates the random bit sequence of length 2^7-1 taking clock as input. With the help of serial to parallel converter as a demultiplexer with two 25% duty cycle clocks acting as a select lines to the demultiplexer. These two 25% duty cycle are generated from the same clock, given to PRBS as input .A pulser generates a pulse from the clock, which act as a injection to the proposed VCO.

The pulse selector selects injection pulses according to the parallel data sequence (I+, Q+, I+, I-). When I+ is high inj<0>

Block diagram of proposed QPSK modulator

gets activated. When I- is high inj<3> is activated. When Q+ is high inj<2> is enable, and inj0<1> is activated if Q- is high. Therefore, as a result phase modulated pulses are injected into the VCO. Fig.7 showing the pulse generating



circuit.

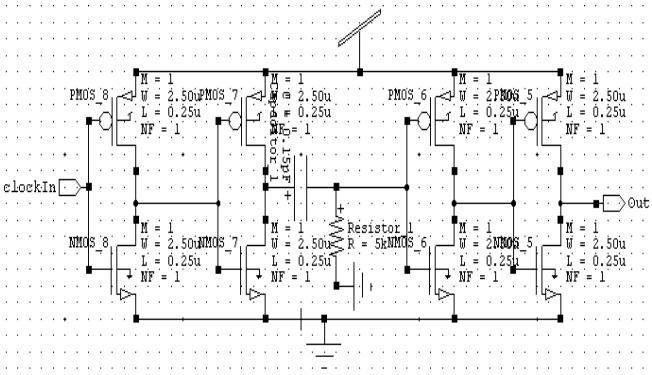
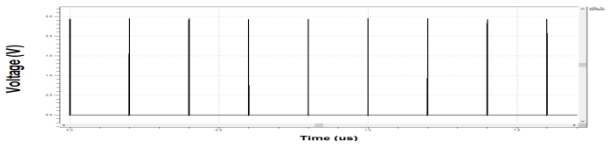


fig.6 Pulse generator circuit



The pulse generated by the pulser on the rising edge of clock, are shown in fig.7.

In the proposed ring VCO, in order to provide phase shift with injection pulse to I- and Q- phase output simultaneously, the NMOS switches are connected between the differential outputs and between the ground and output node as shown in fig 3.

III. SIMULATION AND WORKING

The fig.8 shows the waveforms of different blocks of proposed QPSK modulator e.g. the clock input, which is used to generate pulses and parallel data sequence(in the form of I+,I-,Q+,Q-) with the injection pulses from inj<0:3> and the output of proposed VCO i.e. out0,out 180,out270,out90 are shown.

In the proposed injection locking mechanism, injection signal are injected to VCO, according to the I phase and Q phase signal level. The injection inj<0> and inj<2> are activated according to I+ and Q+ respectively and injection inj<3> and inj<1> are activated according to I- and Q- respectively on the rising edge of the clock as shown in waveform figure.

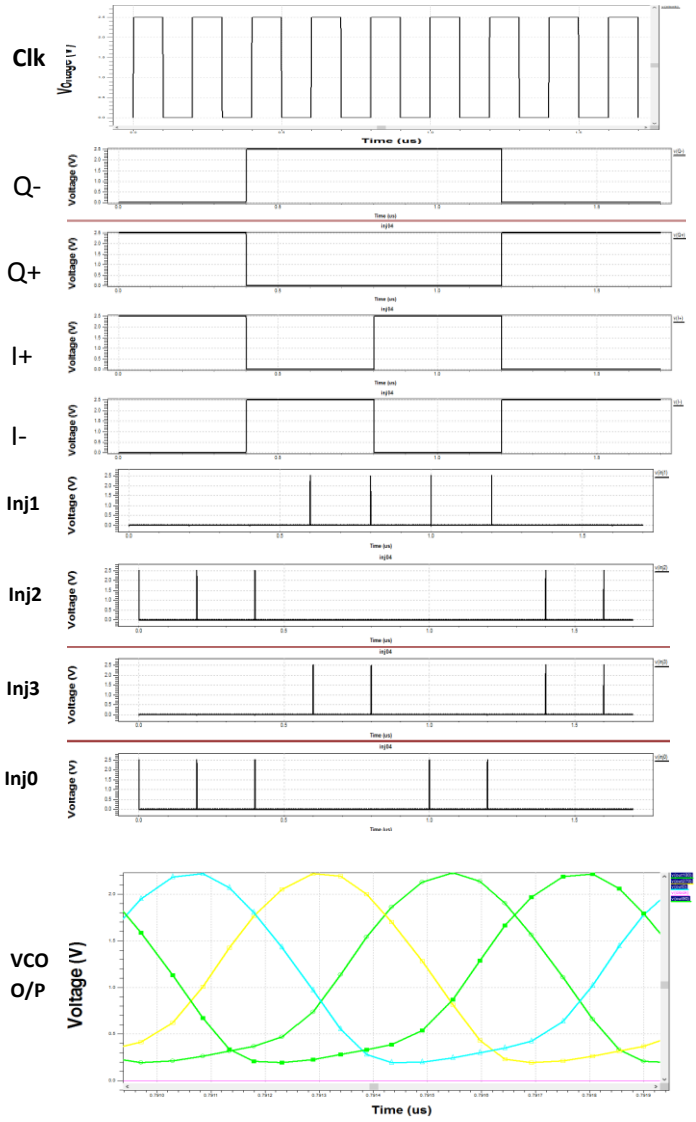


fig.7 Waveforms in the QPSK Modulator

Two injection signals are simultaneously applied to the two stage differential ring VCO to both I phase and Q phase delay cell, in order to achieve efficient locking to data sequence in both stage on the rising edge of the clock

The above response describes the combined response of I phase and Q phase outputs. The individual responses of I+, I-,Q+ and Q- are shown below with corresponding phase difference between them.

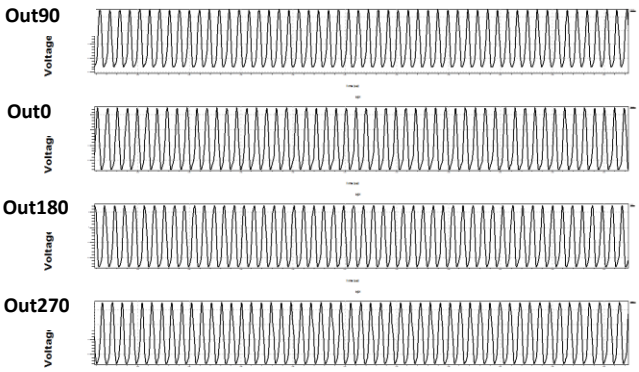


fig.8 Waveforms of I and Q phase signal.

The detailed view of the output is shown in fig10. This figure is describing how the phase of I phase and Q phase output is changing ,when the corresponding injection pulse is inject ed at the risin g edge of the clock .

Out180

Out270

Out0

1.

Out90

11.

clock

fig.10 output waveform at rising edge of clock.

IV. CONCLUSION

According to injection pulse which in turn depends on level of I and Q signal, the phase of output signal changes according to the quadrature phase shift keying modulation. Hence, employing the proposed injection locking mechanism leads to shifting of phase of output, making it convenient to use ring VCO for QPSK modulation.

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