All Digital Phase Locked Loop design for different applications: A Review

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Abstract- **In this Brief, a review of various approaches to design the blocks of all digital phase locked loop (ADPLL) for specific application are presented. Today the most challenging task for designing the phase locked loop (PLL) is to achieve fast locking time and low jitter. In analog design the design complexity is increased. In this paper, advantages of all digital phase locked loop over analog phase locked loop is presented.**

Index Terms- **All digital phase locked loop (ADPLL), Phase locked loop (PLL)**

I. INTRODUCTION

Nowadays the phase-locked loops (PLLs) are widely used in various applications. For example, a chip embedded with its own clock generator to provide the high-speed clock signal, clock recovery, and synchronization of chips and jitter and phase noise reduction. Traditionally, the PLL is composed of some analog blocks, e.g., charge pump and voltage-controlled oscillator (VCO). The leakage problem will become increasingly serious in advanced CMOS processes. As a result, the difficulty and the complexity of designing an analog PLL increase as the technology process advances [2].

There are many advantages of the all-digital phase locked loop (ADPLL) over analog PLL. ADPLLs have better noise immunity, better testability, programmability, stability, and portability over different processes [7], [8], [9] and they can reduce the system turnaround time. The analog PLL suffers from reduced supply voltage and increased gate leakage as the CMOS scaling in nanometer. Also the difficulty and complexity of analog PLL increases as the technology process advances. The ADPLL reduce the sensitivity to process voltage temperature variations, area and power consumption.

In this brief section II describes the basic architecture of ADPLL. Section III describes various approaches of design of ADPLL and section IV compares this approaches and section V discuss the conclusions.

II. DESIGNS OF ADPLL

The basic architecture of ADPLL consists of phase frequency detector, digital loop filter, digital controlled oscillator and frequency divider in the feedback loop. The major component of ADPLL is the digital controlled oscillator. For the different applications the design of digital controlled oscillator has to be changed. The parameters of digital controlled oscillator are the operating frequency range, maximum operating frequency, frequency resolution. General block diagram of ADPLL is shown in Fig.1[6].Various techniques used to design these blocks for specific application are describe as below.

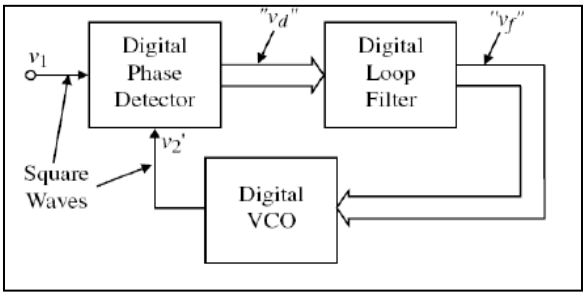

Fig.1 Basic block diagram of ADPLL[6]

A. Design of ADPLL for frequency synthesis

The architecture is to frequency synthesis application in the frequency range of 45-510MHz. In this approach [1] two DCO'S are used to reduce the output clock jitter. One DCO is used for tracking the reference clock and the other is used for generating the output clock. The adaptive search step is algorithm is used to find out target frequency. Loop filter is used to filter out the noise for further

improving jitter performance. Inner DCO has divided into two parts coarse tuning block and fine tuning block to increase the frequency resolution of the DCO. The DCO resolution is 5ps and rms jitter is near to 22ps and the power dissipation is 100mw in this approach.

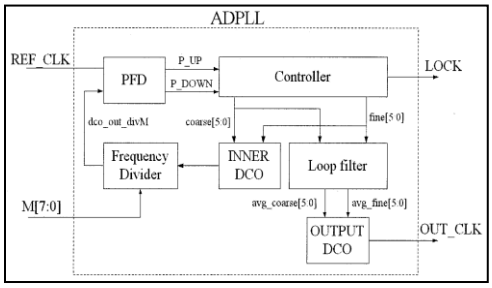

Fig.2 ADPLL for frequency synthesis [1]

B. Design of ADPLL for Wireless communication

In the wireless communication application the PLL has the large Phase error at the instant of frequency hopping, the loop is unable to compensate large phase error and output frequency is slowly updated. So this approach [2] is used to compensate this problem using dynamic phase controlled technique. In this technique to limit the growth of accumulated error, when phase error exceeds certain threshold, it is compensated by temporally changing divided ratio. This approach is to reduce the TDC noise without narrowing bandwidth and higher frequency locking time by using the KI controller. There are two TDC auxiliary and main, responsible for coarse and fine phase error detection. The frequency resolution of DCO can be increased by using delta sigma modulator at the input of DCO.

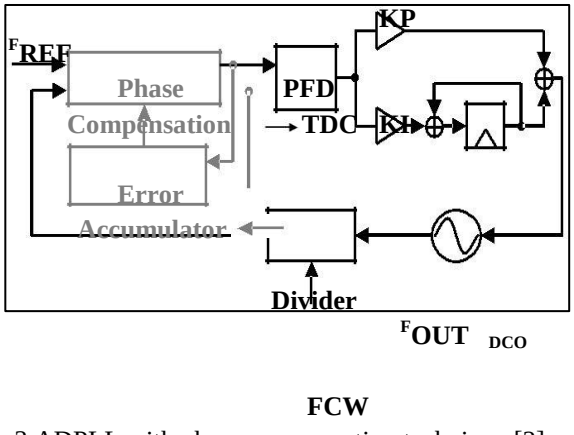

Fig.3 ADPLL with phase compensation technique [2]

C. Design of ADPLL for clock generator of multiple data rate

A clock generator for of MIPI M-PHY transmitter is presented in this approach [3]. In this, the low power with fine frequency resolution DCO is presented. The oscillator runs at the lower frequency range and higher frequency is obtained by using programmable low power frequency multiplier. Also quantization noise is reduce if the DCO frequency step size is minimized while the reference frequency constant.

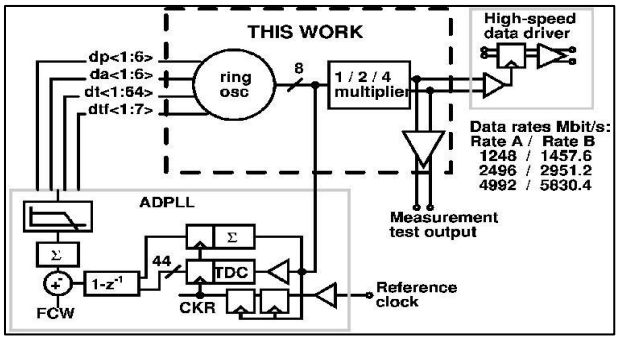

Fig.4 ADPLL with frequency multiplier [3]

D. Design of ADPLL for high speed clock generator

In this approach [4] the proposed parameterized DCO. The parameterized DCO can provide the maximum output frequency more than 1GHz and a wide operating frequency range. Also they developed an ADPLL compiler. By using this ADPLL compiler we could find out a low cost and low power DCO that meets user defined specification.

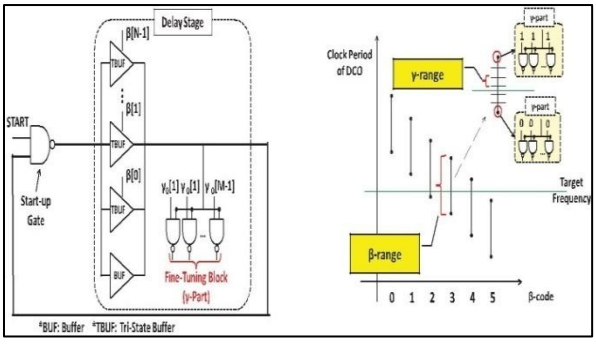

Fig.5 Parameterized DCO [4]

Parameterized DCO is formed with a loop including two parts the coarse tuning block (β-part) and the fine tuning block (γ-part). During frequency acquisition β-code selects the frequency and during phase acquisition γ-code decides the final output.

E. Design of ADPLL for distributed clock generator

This paper [5] developed an ADPLL for the distributed clock generator based on networks of ADPLL. The architecture has a digital multi bit phase frequency detector. This digital PFD is required for synchronized operation of the ADPLL network in the context of distributed clock generator. Digital PFD has bang-bang PFD with time to digital converter and arithmetic block to produce the sign binary phase error.

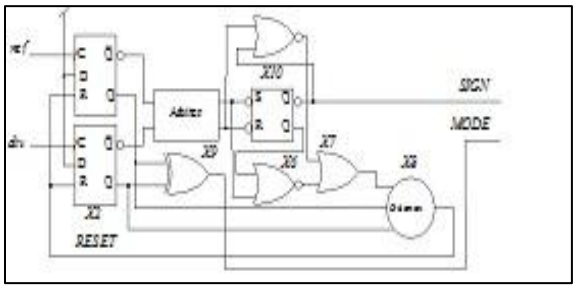

Fig.6 Digital multi bit PFD [5]

III. SUMMERY AND COMPARISON

	[1]	[2]	[3]	[4]
Process	0.35µm CMOS	180nm CMOS	40nm CMOS	180nm CMOS
Area	0.71mm^2	--	0.012mm^2	0.084mm^2
Power Dissipation	100mW	18.6mW	3.9mW	7.2mW
Frequency range	45-510MHz	2.49GHz	1.248-5.83GHz	96.1-1014.6MHz
Output jitter	70ps	13.78ps	--	35.6ps
Lock time	<46 cycles	5µs	--	--

IV. CONCLUSIONS

In this paper the review of ADPLL is presented. Using two DCO we can increase the DCO resolution with wide frequency range. For large phase error detection with less locking time, phase compensation with error accumulation technique is used. Parameterized DCO which can generate more than 1GHz frequency is also presented. For low power reduction in DCO the frequency multiplier is used with lower operating frequency range DCO. High precision PFD for ADPLL network is also presented.

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