Design and analysis Of Sub-Threshold 8-bit ripple carry adder using: Transmission gate at 32_{nm} technology

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***Abstract*- A low power 8-bit Transmission logic ripple carry adder cell based on sub-threshold logic is designed in this paper. Three different sub-threshold low power 8bit adders namely TFA, transmission gate adder and the conventional CMOS adder is designed using different techniques. To compare these adders all simulation is performed using 32nm technology in T-SPICE at voltage varies from the 0.25mv to 0.35mv and the frequency at 10MHZ and 20MHZ. Three different performance parameter like average power consumption, delay of sum and delay of carry and power delay product are calculated and compare with the conventional CMOS. Simulation result shows that the transmission Ripple carry adder shows the better performance at supply voltage 250mv and operating frequency at 10mhz and 20mhz.**

***Index Terms*- sub-threshold logic , low power, VLSI,CMOS circuit, T-SPICE.**

I. INTRODUCTION

CMOS VLSI design have been evolving into low voltage and low power regime. The main focus of the VLSI is to improve the performance of the microprocessor and the system design. The demand of the low power consumption, high speed and low delay is increasing day by day. Arithmetic operations play an important role in modern processing systems to fulfill these requirments. Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as microprocessors and application specific **DSP** architectures. In addition to its main task, which is adding two numbers, it participates in many other useful operations such **as** subtraction, multiplication, division, address calculation etc. In most of these systems the adder lies in the critical path that determines the overall speed **of** the system. **So** enhancing the performance of the Full adder cell (the building block of the adder) is a significant goal.(13) With the increasing demand of portable and mobile computing systems, power consumption has become one of the major design concerns. Numerous circuit design techniques, such **as:** power supply reduction, clock gating, etc have been successfully used in digital circuits to reduce power consumption.(14)

For battery-operated portable applications such as cell phones, PDAs and laptop computers, as well as low-intensity applications such as distributed sensor networks, the need for power sensitive design has grown significantly. It has been shown that reducing the supply voltage is the most direct means of reducing dissipated power, and operating CMOS devices in the sub-threshold region is considered to be the most energy-efficient solution for low-performance applications(15). Full adder is the main core component of the microprocessor and the other complex circuits and the performance of the full adder affect the whole system. There are various type of full adder but due to superior speed and low power consumption the TFA and the transmission gate adder are used in 8bit as the ripple carry adder in sub-threshold region.

II. SUB-THRESHOLD REGION

In sub threshold region the input supply voltage(V_{dd}) is less than the transistor threshold voltage(V_{th}). Portable system such as laptop, wrist watches, pacemaker and cell phones require low power consumption and high density integrated circuits. By running the digital circuits in the sub threshold region low power design of the circuit can be achieved. The sub threshold leakage current can be used as the operating drive current. The sub-threshold drive current is exponentionally related to the gate voltage. By using this exponential relation exponential reduction in power consumption can be achieved, But with this an increase in delay is achieved. So the circuit is used in sub-threshold region where power is main

concern and large delay can be tolerable. The operating current in sub-threshold region is

$I_{ds=Is}\, e^{\frac{Vgs+nVds-Vth}{nVt}} (1-e^{\frac{-Vds}{Vt}})$ …..(1)

where

$Is=\mu n\, Cox \frac{w}{l} (n-1) (Vth)^2$ …..(2)

The parameter in equation(1) and (2) is describe as:-

Vt=thermal voltage($(^{KT}/_{Q})$ =26mv at 300°k)

K=boltzman's constant($1.38\times10^{-23}\ j/k$)

Q=electronic charge(1.602×10^{-19}c)

T=temperature

n=sub-threshold parameter ($n=1+\frac{Cdep}{Cox}$)

$\mu_{n(p)=}$ the carrier mobility for n-(p-) channel device.

C_{ox} = oxide capacitance.

C_{dep} = depletion capacitance.

L=length of the channel.

W=effective width of the channel.

This current is the leakage current which limit the circuit performance but because of using lower supply voltage the circuit operate in sub-threshold region consume less power than the voltage in the strong inversion region. The leakage voltage in the strong inversion region is used as the supply voltage in the sub threshold region. The leakage current provides near ideal voltage characteristic when used for the necessary computation. The motivation for using sub-threshold circuits is the ability to exploit the sub- threshold leakage current as the operating drive current. In sub-threshold region, as shown in the Equation, the drain current Ids is exponentially related to the gate voltage Vgs. The exponential relationship in eq.(1) and (2) is expected to give an exponential reduction in power consumption, also an exponential increase in delay. The delay is out weighted because the power consumption is lower so the power delay product is also lower. The energy consumption is also lower in sub-threshold region as compare to the strong inversion region. Adder is the main objective of the low power digital design. There are many type of adder and the ripple carry adder is used in the sub-threshold region for the lower power consumption.

2.1 Area of application

- The lower power consumption devices such as wrist watch, wireless sensor nodes, RFID tags, medical equipment and self powered devices.
- Many burst mode applications that require high performance for brief time periods between extended sections of low performance operation. Sub-Vt circuits can minimize power consumption for computations executed during the low performance intervals.

III. REVIEW OF 1BIT FULL ADDER CIRCUIT AND 8BIT RIPPLE CARRY ADDER

Three 1bit as well as 8bit Transmission ripple carry full adder. The design of 8 bit adder is done after designing the 1bit adder. The CCMOS is considered as the base adder and all other adders are compared with the CCMOS adder. We have designed 8bit conventional CMOS, TFA and transmission gate adder. The transmission adders have lower power consumption and lower PDP as compare with the CCMOS adder. All the simulation are done using TSPICE in 32nm technology at supply voltage 2.5mv to 3.5mv and the operating frequency at 10mhz and 20mhz.

3.1 1bit conventional CMOS full adder circuit

A basic cell in the circuit computation is the 1bit CCMOS full adder which has three input namely(A, B, Cin) and two output namely (sum, carry). Fig.1 shows the 1bit conventional full adder which is the building blocks of the CMOS circuits. It is based on the regular structure of the CMOS logic and have equal rise and fall time. This design is the benchmark for all the proposed design. All the comparison is done with this design. Figure 1. Shows the 1bit conventional full adder operating in sub threshold region. The adder is divided in two separate equation i.e sum and carry. The sum and carry is 1 when the two input is 1 Otherwise the carry is 0. When all the input is 0 then sum is 0 and carry is also 0.

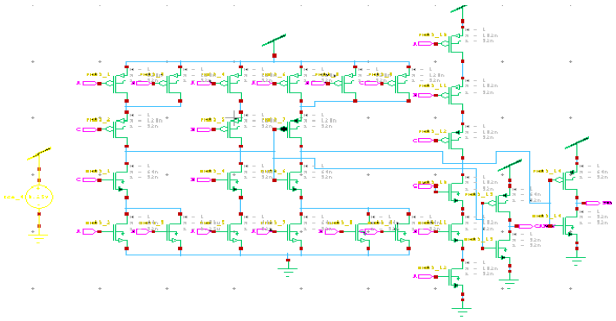

Figure1. 1bit conventional CMOS ripple carry adder

The relation between input and output is shown as:-

Sum= (A xor B) xor Cin

Carry=(A and B) + Cin(A xor B)

The 1bit conventional CMOS ripple carry adder has 28transistors. The CMOS structure combine PMOS (pull up) and NMOS (pull down) transistors. The PMOS and the NMOS are combine in the same and the reverse manner to obtain the desired output. The mutual exclusiveness of the PMOS and the NMOS is of great concern.

3.2 1bit Transmission function full adder circuit

1bit transmission function full adder is shown in figure2. The transmission function full adder is operated in sub threshold region i.e below threshold voltage. The full adder work on the following two equations:-

Sum= (A xor B) xor C_{in}

Carry=(A and B) + C_{in}(A xor B)

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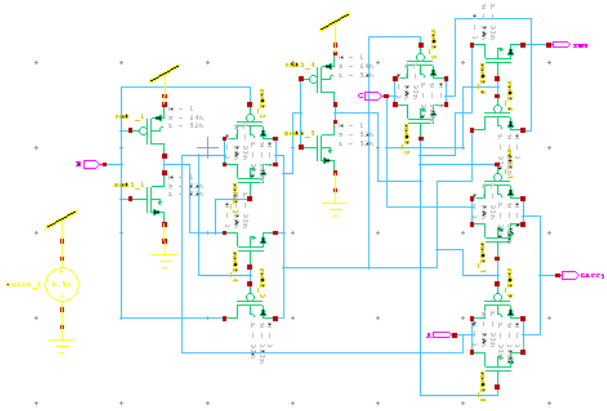

Figure2. 1bit transmission function ripple carry adder.

The circuit which is implemented is based on these equations.

The number of transistor used in the transmission function full adder(TFA) is 16 which is much less than the conventional CMOS full adder. So the area of the circuit is lower than the conventional CMOS. As the area of TFA is less than CMOS then the average power consumption is also less comparatively.

3.3 1bit Transmission gate full adder

Transmission gate full adder is shown in figure 3. In the transmission gate full adder the number of transistor used is 20 which is slightly more than TFA but less than the CCMOS. So the area of the Transmission gate adder is less than the CCMOS full adder but slightly larger than the TFA.

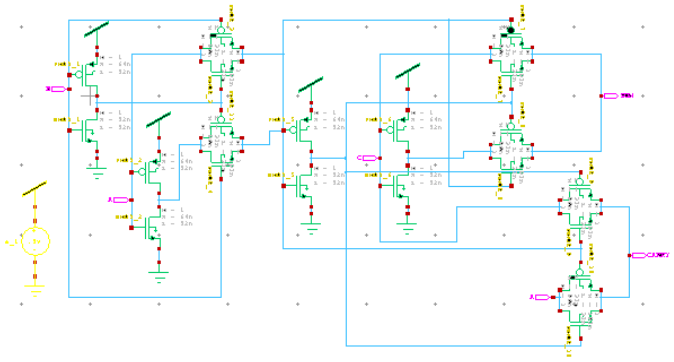

Figure3. 1bit transmission gate ripple carry adder

IV. EXPERIMENTAL RESULT

8bit ripple carry adder is designed by cascading 8 different 1bit full adder in series. In the ripple carry adder the previous carry is connected to the input carry for the next stage. This full adder is called the ripple carry adder because the each carry bit "ripple" to the next stage full adder. The 8bit ripple carry adder is shown in figure4. In the same way we will designed TFA and TGA 8bit full adder.

4.1 Experimental result of 8bit ripple carry adder

We have designed different 8bit ripple carry full adder. After designing the circuits all the simulation is performed in the T-SPICE 32nm CMOS technology standard at the supply voltage varies from 2.5mv to 3.5mv and the operating frequency at 10mhz and 20mhz.

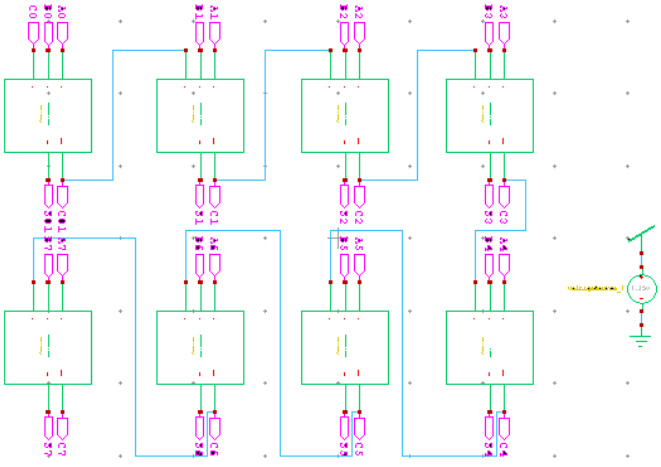

Figure4 8bit Ripple carry adder

Table1 Analysis of different 8bit RCA Vdd=250mv, F=10mhz, Input= A7,B7,C6

Cell name	Power (pw)	Delay Sum (ns)	Delay Carry (ns)	PDP sum (aj)	PDP carry (aj)
CCMOS	0.2380	6.992	5.370	0.001664	0.001278
TFA	0.2021	9.034	2.844	0.001825	0.000574
TGA	0.2908	7.972	3.116	0.002314	0.000906

When we compare different 8bit adder at supply voltage 250mv and operating frequency at 10mhz then we find that TFA consumes less power than the CCMOS and TGA and the delay of the CCMOS is 6.992ns and 7.972ns for TGA for the last input A7,B7 and C_{in6}.

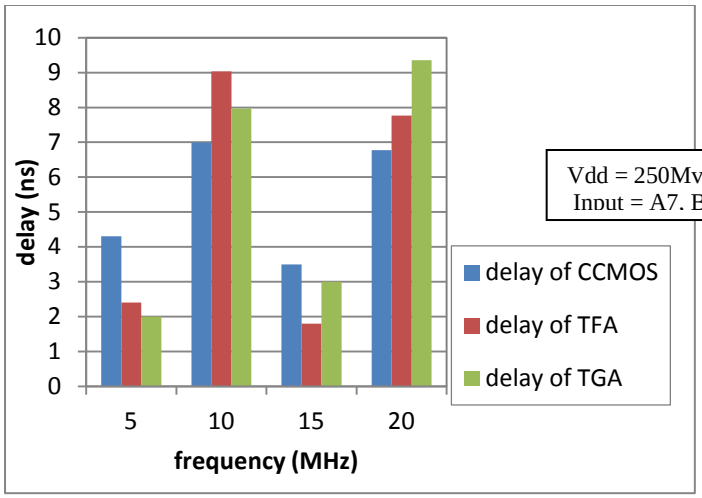

Figure5. Graph of frequency vs delay at V_{dd} 250 mv

Table2. Analysis of different 8bit RCA Vdd=300mv, F=10mhz, Input= A7,B7,C6

Cell name	Power (pw)	Delay Sum (ns)	Delay Carry (ns)	PDP sum (aj)	PDP carry (aj)
CCMOS	0.2541	9.725	6.711	0.00247	0.00171
TFA	0.2350	6.086	2.488	0.00143	0.000584
TGA	0.3476	8.535	2.680	0.00296	0.000931

At supply voltage 300mv and frequency - at 10mhz the delay and power consumption of the TFA is lowest and then of CCMOS and TGA has the highest delay.

Table3. Analysis of different 8bit RCA Vdd=350mv, F=10mhz, Input= A7,B7,C6

Cell name	Power (pw)	Delay Sum (ns)	Delay Carry (ns)	PDP sum (aj)	PDP carry (aj)
CCMOS	0.3126	6.665	4.404	0.002083	0.00137
TFA	0.2662	4.265	2.272	0.001135	0.000604
TGA	0.4044	5.403	2.405	0.002185	0.000972

At supply voltage 350mv and the operating frequency at 10mhz again the delay of the TFA is lowest and then TGA and CCMOS.

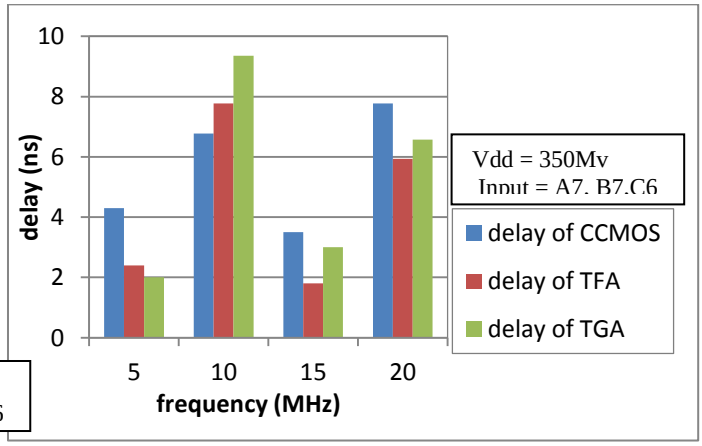

Figure6. Graph of frequency vs delay at Vdd 350mv

At the operating frequency at 20mhz and 10mhz and Supply voltage is 250mv the circuit give lower power consumption and lower PDP as compare to the other frequency and the other supply voltage. The delay is considerably large as compare to the others but the large delay is tolerable because the power consumption and the power delay product is lower. So the the circuit gives good and proper result at the supply voltge250mv and the operating frequency at 10mhz and 20mhz.

Table4. Analysis of different 8bit RCA Vdd=250mv, F=20mhz, Input= A7,B7,C6

Cell name	Power (pw)	Delay Sum (ns)	Delay Carry (ns)	PDP sum (aj)	PDP carry (aj)
CCMOS	0.3856	6.772	6.299	0.002611	0.002428
TFA	0.3528	7.769	4.630	0.002741	0.001633
TGA	0.4962	9.352	5.179	0.004641	0.002569

Table5. Analysis of different 8bit RCA Vdd=300mv, F=20mhz, Input= A7,B7,C6

Cell name	Power (pw)	Delay Sum (ns)	Delay Carry (ns)	PDP sum (aj)	PDP carry (aj)
CCMOS	0.4504	8.327	8.165	0.003751	0.003677
TFA	0.4135	7.672	4.256	0.003173	0.001759
TGA	0.5958	9.748	4.705	0.005808	0.002803

Table6. Analysis of different 8bit RCA Vdd=350mv, F=20mhz, Input= A7,B7,C6

Cell name	Power (pw)	Delay Sum (ns)	Delay Carry (ns)	PDP sum (aj)	PDP carry (aj)
CCMOS	0.5224	7.769	6.007	0.004058	0.003138
TFA	0.4740	5.933	3.928	0.002812	0.001861
TGA	0.6981	6.571	4.176	0.004587	0.002915

V. CONCLUSION

In this paper we proposed design based on the transmission gate in sub- threshold region. CCMOS, Transmission gate adder and Transmission function full adder are designed by using T-SPICE 32nm technology. This study also includes the change in the supply voltage, width to length ratio and the frequency. The simulation is done at the supply frequency varies from 2.5v to 3.5v and the operating frequency at 10mhz and 20mhz. The parameter Average power, Delay and Power delay product is investigated. The 8 bit Transmission ripple carry adder with low power consumption, acceptable delay and lower PDP is achieved. Simulation result shows that the circuit simulated in TSPICE 32nm technology give good result at 10mhz and 20mhz frequency and at 250mv voltage supply.

VI. FUTURE SCOPE

Designer can design 16 bit transmission based adder based on the present design. and the further work can be done on the average power and delay improvement by using some other techniques. Delay and average power consumption gives a good impact on the circuit performance. so more work can be done on these two factors and other factor of work can be noise margin. Researcher can co work on noise margin.

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