

Design of the High Frequency Synthesizer with In-Phase Coupled VCO

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Abstract-- In this paper we proposed high performance frequency synthesizer system which includes a fully integrated optimized current starved voltage controlled oscillator (CSVCO) circuit with VCO compact inductor-less cascaded frequency divider chain. The frequency divider consists of a modified divide-by-4 dynamic current-mode logic (DCML) divider, a divide-by-4 multi-phase injection-locked frequency divider (ILFD), and a multi-modulus true-single-phase-clock (TSPC) divider. The operation frequency of the divider is greatly increased by using low threshold CMOS circuits with differential amplifier pair. In all the three cascaded structures are inductor less and it will lead significant power reductions over all other inductance based high speed frequency synthesizers. Multiphase clock injections with balanced and high conductance global circuitries are used for maximum performance levels. This multiphase nature of frequency dividing chain can improve the locking range. Finally the performance metrics of this cascaded structure will be proved through SPICE based simulation using CMOS library.

Index Terms—CMOS, frequency synthesizer, current starved VCO (CSVCO), PLL, 5GHz, feedback divider path.

I.INTRODUCTION

The recent exponential growth in wireless communication has increased the demand for more available channels in mobile communication applications. As we defined in the high frequency standards, such as in various wireless communications which includes WiGig, WirelessHD etc., To achieve a higher data rate, complex modulations such as CSVCO is adopted, which increases the requirements of the oscillator's phase noise and phase error. In recent years, it has already been demonstrated that advanced CMOS technology has the capability of realizing different wave integrated circuits. CMOS implementation can

reduce cost and improve yield, since RF front-end can be integrated with analog and digital baseband circuits.

Phase locked-loop (PLL) is an important block in a transceiver. Design of the wide range, low phase noise, low phase error and low power CMOS PLL. In this work, we have presented the most important and complex method for the implementation of PLL which includes various stages to achieve the high frequency synthesizer with in-phase coupled VCO. Here we are going to describe the entire PLL structure in 3 sections. Mainly the PLL consists of a feedback path which includes the serial cascaded inductor less frequency divider[1]. Here the inductor less frequency divider which is used to divide the multiple frequency available from the VCO and later in the serial cascaded frequency divider consists of a DCML (Dynamic Current Mode Logic) which takes the VCO output as input and divides the frequency into multiple ranges such that we can achieve a low propagation delay along with multiple phase shifted outputs. After getting the outputs from the DCML stage further we will proceed to the next stage i.e., 2/3 counter which is used to get the pulses, which are required for the next stage i.e. Phase Frequency Detector. In PFD fig.1 only pulses are accepted as input so we have to maintain that in order to acquire pulse waveform. Charge pump which is used to generate the voltage, from which we will develop the sine wave by using the CSVCO.

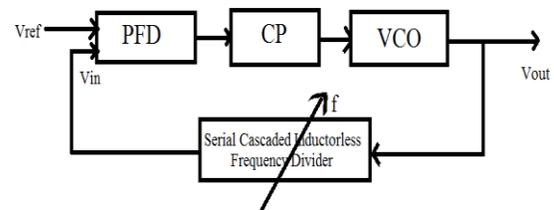


Fig.1 Basic diagram of PLL

From this PLL method we are going to achieve a high frequency of 5 GHz, which is required for the current generation for the long distance

communication. A high frequency synthesizer is always a challenging one to design and implement, in that case we have chosen some different method for the construction of PLL. In PLL the main module is VCO. Here we have equipped a new method for the construction of VCO. Generally for the perfect sine wave outcome it depends only on the aspect ratios of the transistors, in this case for the perfect outcome we are employing a genetic algorithm which provides you the required aspect ratios. The genetic algorithm is carried out in MATLAB. The low power inductorless frequency divider chain consists of a modified divide-by-4 dynamic current-mode logic (DCML) divider, a divide-by-4 multi-phase injection-locked frequency divider (ILFD), and a multi-modulus true-single-phase-clock (TSPC) divider.

The paper is organized as follows. Section II discusses the proposed CSVCO, including architecture, analysis, and circuit design. Section III describes the frequency divider chain and charge pump design. Experimental results are provided in Section IV and conclusions are drawn in Section V.

II. DEISGN OF CSVCO

A ring oscillator is comprised of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. This current starved VCO is designed using ring oscillator and its operation is also similar to that. From the schematic circuit shown in the Figure 1, it is observed that MOSFETs M2 and M3 operate as an inverter, while MOSFETs M1 and M4 operate as current sources. The current sources, M1 and M4, limit the current available to the inverter, M2 and M3; in other words, the inverter is starved for the current. The MOSFETs M5 and M6 drain currents are the same and are set by input control voltage. The currents in M5 and M6 are mirrored in each inverter/current source stage. The upper PMOS transistors are connected to the gate of M6 and source voltage is applied to the gates of all lower NMOS transistors.

A. Frequency Calculations

The drain current of a short channel MOSFET operating in saturation region is given by:

$$I_d = W \cdot V_{sat} \cdot C_{ox} (V_{GS} - V_{THN} - V_{DS,sat})$$

From this equation we can write the equation for the width of NMOS, which is given by:

$$W_n = \frac{I_d}{V_{sat} \cdot C_{ox} (V_{gs} - V_{th} \cdot V_{ds,sat})}$$

By putting the values of these parameters in the equation of W_n , we get the value W_n in 45nm technology, which is given by:

$$W_n = 180nm$$

For the Ratio of W/L ,

$$(W/L)_p = 2.5(W/L)_n$$

Now, we know that the values of L for NMOS and PMOS are same in 45 nm technology, so we get

$$L_p = L_n = 45nm$$

So, the ratio will be

$$W_p = 2.5W_n$$

By putting the values of W_n in above equation, we get $W_p = 450nm$

Finally we get the ratio of W/L for NMOS & PMOS in 45nm technology:

□ For NMOS: $W_n = 180nm, L_n = 45nm$.

□ For PMOS: $W_p = 450nm, L_p = 45nm$

To determine the design equations for use with the current-starved VCO, the total capacitance on the drains of M2 and M3 is given by

$$C_{tot} = C_{out} + C_{in}$$

$$C_{tot} = \frac{5}{2} C_{ox} (w_p l_p + W_n l_n)$$

The oscillation frequency of the current starved VCO for N (an odd number ≥ 5) of stages is

□ □ □

$$F_{osc} = \frac{1}{N \cdot C_{tot} \cdot V_{DD}}$$

Where N is number of stages

V_{DD} Is supply voltage

The operation of current starved VCO is similar to the ring oscillator. Middle PMOSM1 and NMOSM2 operate as inverter, while upper PMOSM13 and lower NMOSM14 operate as current sources. The current sources limit the current available to the inverter. In other words, the inverter is starved for current. The current in the first NMOS and PMOS are mirrored in each inverter/current source stage. PMOSM11 and NMOSM11 drain currents are the same and are set by the input control voltage.

The phase frequency detector (comparator) produces an error output signal based on the phase difference between the phase of the feedback clock and the phase of the reference clock. Over time, small frequency differences accumulate as an increasing phase error. If there is a phase difference between the

two signals, it generates up or down synchronized signals to the charge pump/ low pass filter. If the error signal from the PFD is an up fig.2 signal, then the charge pump pumps charge onto the LPF capacitor which increases the control voltage control V_c .

The following figure shows the block diagram of 13 stage CSVCO:

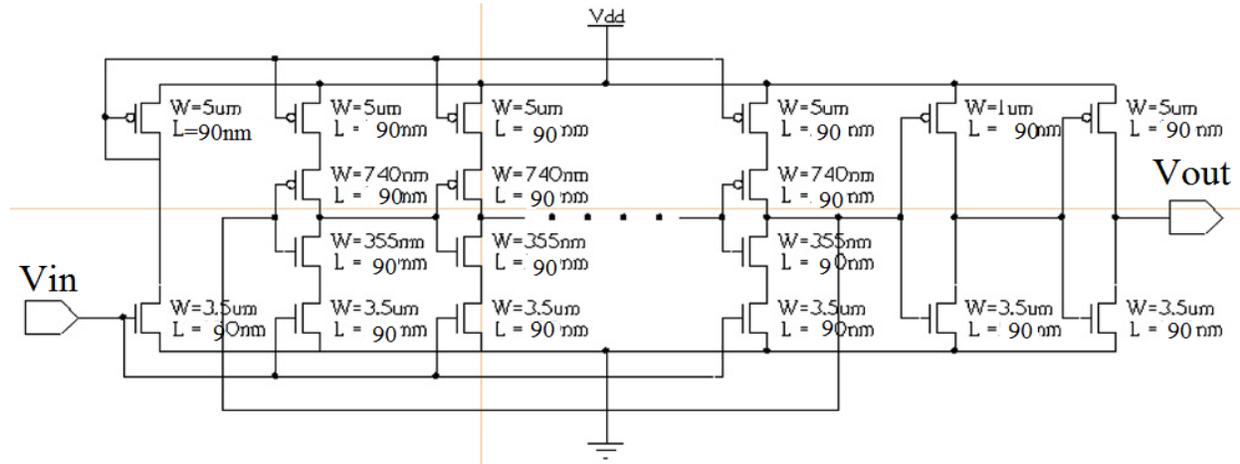


Fig. 2 Block diagram of CSVCO

To calculate the frequency for 13 stage CSVCO, we use the formula

$$F_{osc} = \frac{1}{N \cdot C_{tot} \cdot V_{DD}}$$

B. Infeasibility Driven Evolutionary Algorithm

Infeasibility Driven Evolutionary Algorithm (IDEA) was proposed by Singh *et al.* It differs from the conventional EAs significantly in the terms of ranking and selection of the solutions. While most EAs rank feasible solutions above infeasible solutions, IDEA ranks solutions based on the original objectives along with additional objective representing constraint violation measure. IDEA explicitly maintains a few infeasible solutions during the search. In addition, “good” infeasible solutions are ranked higher than the feasible solutions, and thereby the search proceeds through both feasible and infeasible regions, resulting in greater rate of convergence to optimal solutions. The concept of using “good” infeasible solutions during the search for constraint handling has also been explored by a few other researchers in the past for constraint handling Algorithm.

However, the method of exploitation of infeasible solution differs for each of these approaches. For example, Hamida and Shoenuer used adaptive

penalty to control the proportion of feasible solutions in the population. Vieira *et al* treated constraints as objectives during the search. Coello Coello proposed to split the population into various sub-populations, each sub-population using either objective or one of the constraints as fitness function. Isaacs, Ray and Smith proposed Constraint Handling Evolutionary Algorithm (CHEA), where they treated the number of constraint violations as an additional objective, to obtain constrained and unconstrained optimum for a problem simultaneously.

III. CASCADED INDUCTOR-LESS FREQUENCY DIVIDER

A. Phase Modulated Reference Signals

Designing frequency dividers is challenging in PLL since they may consume substantial power. Large area is another issue due to the use of inductors. In this work, the inductor-less DCML divider, ILFD, and TSPC divider are implemented in cascade. By using these divider topologies, the low power and small area can be achieved simultaneously. We will describe them separately. Fig. depicts the schematic

of the modified DCML divide-by-4 frequency divider. Compared with a traditional CML divider, the DCML divider uses the parasitic capacitor in differential amplifier pair, instead of a static cross-coupled latch, to store the data. By removing the cross-coupled pairs, the maximum operation frequency of the divider is increased, making it suitable for mm-wave frequency. To further improve its performance, two methods have been adopted. Firstly, low threshold voltage (low-V_t) devices are used to increase the maximum operation frequency for their higher F_t. Secondly, we merge the switches of the same input clock of the DCML divider i.e., node X_a and node X_b are connected together. By connecting and, we now present a balanced and high conductance point at the input frequency. Therefore, the injection currents of the modified DCML divider are larger than that of the conventional DCML divider/ from the point of view of injection locking, the locked bandwidth of the modified DCML divider is enlarged. In order to balance the output loadings, all the eight-phase outputs of the DCML divider serve as the inputs of the next divider. By using DCML divider, we have generated 8 multi-phase sine waves within a range of 400 MHz for each sub-band. The DCML divider works in the range of 3 to 5 GHz.

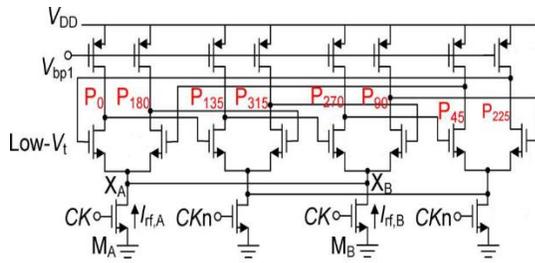


Fig. 3 Dynamic Current Mode Logic (DCML) divider

The multiphase injection with proper sequence can improve the locking range of the divide-by-4 ILFD. Fig. Shows its post-layout simulation results with different bias voltages. With about 300 mV peak-to-peak input voltage, the divider works from 8 GHz to 28 GHz. The locking rang of each sub-band is large enough to cover about 5 GHz input range. The simulated power consumption is less than 3.2 mW with a 1.2 V supply.

A free-running oscillator which has a small amount of a higher-frequency signal fed to it will tend to oscillate in step with the input signal. Such frequency dividers were essential in the development of television. It operates similarly to an injection

locked oscillator. In an injection locked frequency divider, the frequency of the input signal is a multiple (or fraction) of the free-running frequency of the oscillator. While these frequency dividers tend to be lower power than broadband static (or flip-flop based) frequency dividers, the drawback is their low locking range. The ILFD locking range is inversely proportional to the quality factor (Q) of the oscillator tank. In integrated circuit designs, this makes an ILFD sensitive to process variations. Care must be taken to ensure the tuning range of the driving circuit (for example, a voltage-controlled oscillator) must fall within the input locking range of the ILFD.

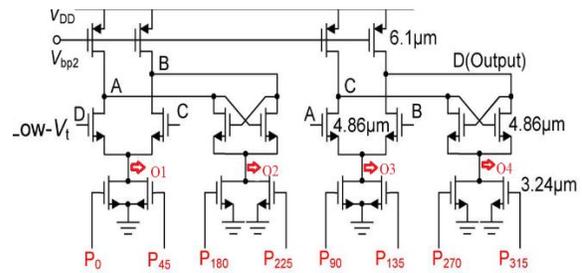


Fig. 4 Injection Locked Frequency Divider(ILFD)

A fractional-n frequency synthesizer can be constructed using two integer dividers, a divide-by-n and a divide-by-(n + 1) frequency divider. With a modulus controller, n is toggled between the two values so that the VCO alternates between one locked frequency and the other. The VCO stabilizes at a frequency that is the time average of the two locked frequencies. By varying the percentage of time the frequency divider spends at the two divider values, the frequency of the locked VCO can be selected with very fine granularity.

B. 2/3 Counter

The proposed frequency divider attains programmable division ratios from 481 to 512, which realizes all available channels in IEEE 802.11b/g communication systems. The 5-bit mode input control determines the number of times to perform phase-switching in each cycle, from 0 to 31 times (which corresponds to division ratios from 512 to 481 respectively). The phase switching control circuitry consists of an 8-bit shift register to select the correct output phase and combinational logic to trigger the

shift register to the next state during phase-switching.

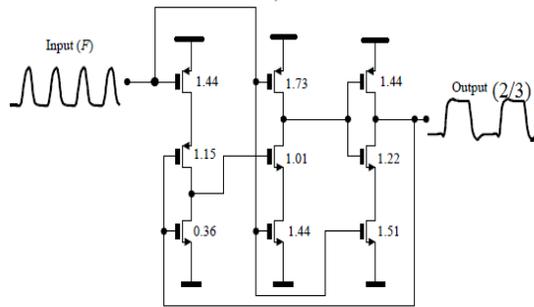


Fig. : 2/3 counter

The novel quadrature-input divide-by-8 ILFD consists of four-stage D-latches connected in a ring configuration, as depicted in Fig. 2. The last stage differential output is connected, in reversed polarity, to the differential input of the first stage to obtain an additional 180° phase shift for oscillation. Each latch is triggered by the same clocking signals. When the CLK is high, the oscillation signal propagates by one stage. The latches then hold the current state when the CLK is low. Eight input clock cycles are needed for the oscillation signal to return to the original state. As such, it acts as a divide-by-8 frequency divider.

IV. PHASE FREQUENCY DETECTOR AND CHARGE PUMP

A phase frequency detector (PFD), in electronics, is a device which compares the phase of two input signals. It has two inputs which correspond to two different input signals, usually one from a voltage-controlled oscillator (VCO) and another from some external source. It has two outputs which instruct subsequent circuitry on how to adjust to lock onto the phase. To form a Phase-locked loop (PLL) the PFD phase error output is fed to a loop filter which integrates the signal to smooth it. This smoothed signal is fed to a voltage-controlled oscillator which generates an output signal with a frequency that is proportional to the input voltage. The VCO output is also fed back to the PFD to form the PLL circuit. The PFD is an improvement over the phase comparators of early PLLs in that it also provides a frequency error output as well as a phase error signal.

A phase-frequency detector is an asynchronous sequential logic circuit originally made of four flip-flops (i.e., the phase-frequency detectors found in both the RCA CD4046 and the motorola MC4344 ICs introduced in the 1970s). The logic determines which of the two signals has a zero-

crossing earlier or more often. When used in a PLL application, lock can be achieved even when it is off frequency and is known as a Phase Frequency Detector. Such a detector has the advantage of producing an output even when the two signals being compared differ not only in phase but in frequency. A phase frequency detector prevents a "false lock" condition in PLL applications, in which the PLL synchronizes with the wrong phase of the input signal or with the wrong frequency (e.g., a harmonic of the input signal).

A bang-bang charge pump phase detector supplies current pulses with fixed total charge, either positive or negative, to the capacitor acting as an integrator. A phase detector for a bang-bang charge pump must always have a dead band where the phases of inputs are close enough that the detector fires either

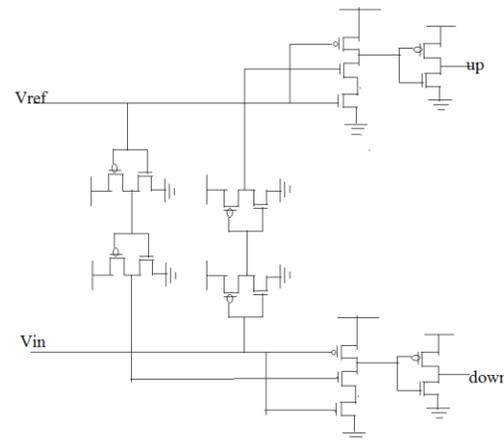


Fig.5 Phase Frequency Detector

both or neither of the charge pumps, for no total effect. Bang-bang phase detectors are simple, but are associated with significant minimum peak-to-peak jitter, because of drift within the dead band. In 1976 it was shown that by using a three-state phase detector configuration (using only two flip-flops) instead of the original RCA/Motorola twelve-state configurations, this problem could be elegantly overcome. For other types of phase-frequency detectors other, though possibly less-elegant, solutions exist to the dead zone phenomenon. Other solutions are necessary since the three-state phase-frequency detector does not work for certain applications involving randomized signal

degradation, which can be found on the inputs to some signal regeneration systems (e.g., clock recovery (designs) A proportional phase detector employs a charge pump that supplies charge amounts in proportion to the phase error detected. Some have dead bands and some do not. Specifically, some designs produce both "up" and "down" control pulses even when the phase difference is zero. These pulses are small, nominally the same duration, and cause the charge pump to produce equal-charge positive and negative current pulses when the phase is perfectly matched. Phase detectors with this kind of control system don't exhibit a dead band and typically have lower minimum peak-to-peak jitter when used in PLLs. In PLL applications it is frequently required to know when the loop is out of lock. The more complex digital phase-frequency detectors usually have an output that allows a reliable indication of an out of lock condition.

B. Charge Pump

A charge pump is a kind of DC to DC converter that uses capacitors as energy storage elements to create either a higher or lower voltage power source. Charge pump circuits are capable of high efficiencies, sometimes as high as 90–95% while being electrically simple circuits. Charge pumps use some form of switching device(s) to control the connection of voltages to the capacitor. For instance, a two-stage cycle can be used to generate a higher pulsed voltage from a lower-voltage supply. In the first stage of the cycle, a capacitor is connected across the supply, charging it to that same voltage. In the second stage of the cycle, the circuit is reconfigured so that the capacitor is in series with the supply to the load. Ignoring leakage effects, this effectively provides double the supply voltage to the load (the sum of the original supply and the capacitor). The pulsing nature of the higher voltage output is typically smoothed by the use of an output capacitor. An external or secondary circuit drives the switching, typically at tens of kilohertz up to several megahertz. The high frequency minimizes the amount of capacitance required as less charge needs to be stored and dumped in a shorter cycle. The capacitor used as the charge pump is typically known as the "flying capacitor". Another way to explain the operation of a charge pump is to consider it as the combination of a DC to AC converter (the switches) followed by a voltage multiplier. The voltage is load-dependent; higher loads result in lower average voltages. Charge pumps can double voltages, triple voltages, halve

voltages, invert voltages, fractionally multiply or scale voltages (such as $\times 3/2$, $\times 4/3$, $\times 2/3$, etc.) and generate arbitrary voltages by quickly alternating between modes, depending on the controller and circuit topology. The term 'charge pump' is also commonly used in phase-locked loop (PLL) circuits even though there is no pumping action involved unlike in the circuit discussed above. A PLL charge pump is merely a bipolar switched current source. This means that it can output positive and negative current pulses into the loop filter of the PLL. It cannot produce higher or lower voltages than its power and ground supply levels.

V. SIMULATION RESULTS

The output of the CSVCO is shown in the following figure. Here the peak to peak voltage is 1 V and the frequency is varies from 3 GHz to 4 GHz

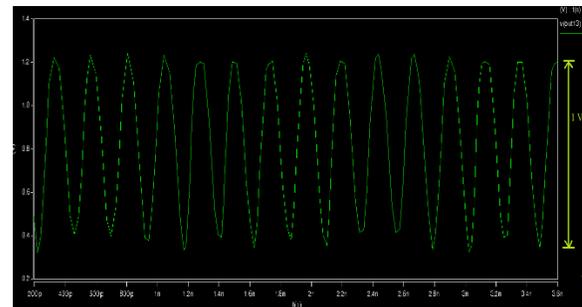


Fig.6 Output of CSVCO

The output of the cascaded frequency divider is shown below and the division of frequency is carried between 800 MHz for each band.

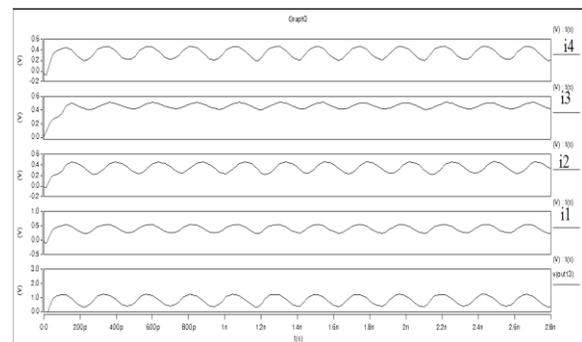


Fig. Serial Cascaded Inductorless output

The forward path consists of PFD and a LPF, the output of the PFD is shown below. In the output we

are getting two outputs which are UP and Down waveforms from which we are going to obtain the dc

S.no	Control Voltage (V)	Frequencies
1	1.0	3.32 GHz
2	1.1	3.85 GHz
3	1.2	4.29 GHz
4	1.3	4.32 GHz
5	1.4	4.56 GHz

voltage which is again given as input to the CSVCO.

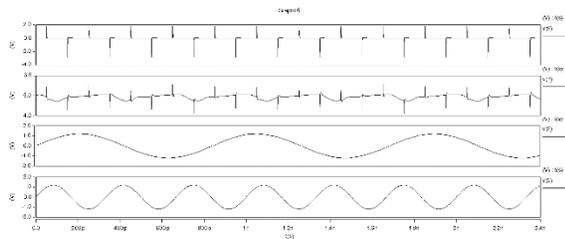


Fig.7 Output of PFD & LPF

The output frequency for different control voltages

Table. 1 Frequencies at Different voltages

S.No	Parameter	Control Voltage(1.2V)
1.	Propagation Delay	3.307 x10 ⁻¹⁰
2.	Leakage Current	0.841 mA
2.	Average Power	0.2838 mW
3.	Peak Power	0.3996 mW

Table. 2 PLL parameters

VI. CONCLUSION

A 4 GHz frequency synthesizer is designed and proposed for the support of various wireless equipments like WirelessHD, Transceivers etc. This high frequency synthesizer design is different from all other designs due to its complex design consideration like the feedback path is constructed without any inductor which means it doesn't depend on the frequency. If there is any change in frequency we don't need to change the feedback path. Finally we are going to achieve a frequency range of 3.5 to 4.2 GHz at 1.2 V control voltage.

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