

Implementation of Delay Measurement Technique Using Signature Analysis

Supriya Thorat¹, Snehal Bhosale²

¹Savitribai Phule Pune University, Department of E & TC, R.M.D Sinhadgad School of Engineering Pune 411052, India

²Savitribai Phule Pune University, HOD, Department of E & TC, R.M.D Sinhadgad School of Engineering Pune 411052, India

Abstract- This paper presents scan based delay measurement technique using signature register and scan flip-flop to detect small delay defect. Small delays are occur due to resistive short, resistive-open, or resistive-via become serious problems. Large scale integration of LSI has resulted in an increase in small delay defects. Small delay variations are induced by process variation, power supply noise as well as resistive opens and shorts. In this paper we use flip-flop design which is used in performing internal path-delay test and measurement using scan path technique. The proposed method measures delay of the explicitly sensitized paths using on chip variable clock generator. The proposed scan design realizes complete on-chip delay measurement in short measurement time using the proposed delay measurement technique and extra latches for storing the test vectors.

Index terms- Very large scale integration (VLSI), signature register, design for testability (DFT), Scan flip-flop.

I. INTRODUCTION

Semiconductor process technology has developed rapidly to improve the performance of modern VLSI chips. As a continuous process scaling produces large-scale chips. With the rapid development of semiconductor technology, delay testing has become a critical problem. The major types of delays are occurred because of resistive-shorts, resistive-open and resistive-vias. These small delays can cause a fail of a system if they are activated for a longer time. Furthermore their life time become very short. Therefore to overcome these drawbacks some embedded delay measurement techniques have been proposed. Scan-based delay measurement technique with variable clock generator is one of these on-chip delay measurement techniques. The delay of path is measured by continuous sensitization of path under measurement with test clock width reduced gradually. The advantage of this technique is its high accuracy. This technique has some drawbacks. Therefore we present a scan-based delay measurement technique which uses signature registers.

A.EXISTING SYSTEM

These days, various methods for small-delay defect detection have been proposed. Scan-based delay measurement technique with variable clock generator is most widely used. In this technique the delay of path is measured by continuous sensitization of path under measurement with test clock width reduced gradually by resolution. In this technique the accuracy is high. The reason of the high accuracy is that the technique measures just the period between the time when a transition is launched to the measured path and the time when the transition is captured by the flip flop connected to the path, directly. The variation of the measured value just depends on the variation of the clock frequency of the clock generator. Therefore, if the clock generator is compensated the influence of the process variation, the measured value does not depend on the process variation.

B. Drawbacks of Existing System

- The gap between the functional clock and scan clock frequency increases. Therefore the measurement time becomes too long to make it practical.
- Area reduction technique of the self testing scan-FFs is also proposed. The flip flop reduces the required number of scan operations, which makes the measurement time practical.

We present a scan-based delay measurement technique using signature registers for small-delay defect detection. The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The overall area cost is of the order of conventional scan designs for design for test (DFT).

C. PROPOSED SYSTEM

We present a scan-based delay measurement technique using signature registers for small-delay defect detection. The proposed method does not require the expected test vector because the test responses are analyzed by the signature registers. The overall area cost is of the order of conventional scan designs for

design for test (DFT). The measurement time of the proposed technique is smaller than conventional scan-based delay measurement. The extra signature registers can be reused for testing, diagnosis, and silicon debugging.

D. ADVANTAGES OF PROPOSED SYSTEM

The proposed method does not use the large-sized multiplexers but use scan chain and limited length extra wires. Therefore it has less probability of degradation of the performance of normal operation. The embedded delay measurement approach can measure a path per a test vector. Therefore the measurement time increases as the number of the measured path.

E. PULSE GENERATOR

In the proposed method, the clock width should be reduced continuously by a constant interval. It is complex for an external tester to control this clock operation. Therefore an on-chip variable clock generator is used for the proposed method. In this paper, we use the on-chip variable clock generator. Figure1 illustrates the circuit. The circuit consists of the arbitrary clock frequency generator and the 2-pulse generator. The arbitrary clock frequency generator generates an arbitrary clock width. The 2-pulse generator generates 2-pulse test clocks with arbitrary timing in response to a trigger signal.

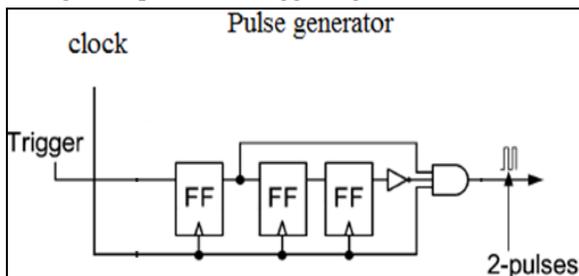


Figure 1: variable clock generator

II. DELAY MEASUREMENT TECHNIQUE USING SIGNATURE REGISTER

The proposed measurement is scan-based delay measurement. The difference from the existing one is use of signature registers and additional latches. In this measurement latches are used to store test vector after scan-in operation.

A. SCAN FLIP FLOPS

An important flip-flop function for ASIC testing is so-called scan capability. The idea is be able to drive the flip-flop’s D input with an alternate source of data during device testing. When all of the flip-flops are put into testing mode, a test pattern can be “scanned in” to

the ASIC using the flip-flops’ alternate data inputs. After the test pattern is loaded, the flip-flops are put back into “normal” mode, and all of the flip-flops are clocked normally. After one or more clock ticks, the flip-flops are put back into test mode, and the test results are “scanned out. Figure2 shows the gate level description of scan flip flop. The lines D, Q, and clk are the input, output, and clock lines, respectively. When se0=0, the flip flop is in normal operation mode. When se0=1 and se1=1, the flip flop is in scan operation mode. When se0=1, se1=0, the flip flop loads the value stored in the latch connected to the latch line. The lines si and s0 are the input and output for constructing the scan path.

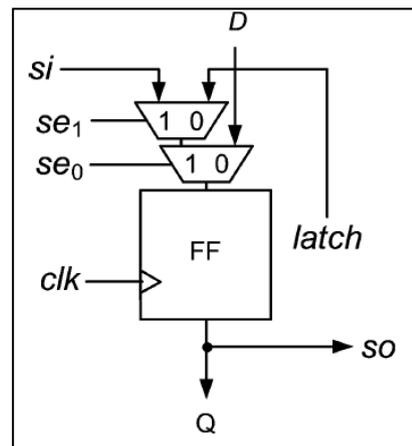


Figure 2: scan flip flop

B. RECONFIGURABLE SIGNATURE REGISTER

This applet demonstrates a so-called signature analysis register. The circuit is based on the standard linear feedback shift register (see the previous applet), but with extra XOR-gates between the flip-flops. Each such XOR-gate provides one data input to the signature analysis register.

The choice where to add such extra inputs to the basic linear-feedback shift register is completely arbitrary, and up to two n extra inputs can be used to an n-stage LFSR. In the applet, only the first and fourth stage of the linear-feedback shift-register is modified to include those extra XOR gates, for a total of two data inputs. Signature analysis registers are often used in combination with standard LFSRs for on-chip self test of VLSI circuits. The signature register for the proposed measurement requires the following functions.

- Capturing the test response in arbitrary timing.
- Shifting out the signature data in arbitrary timing.

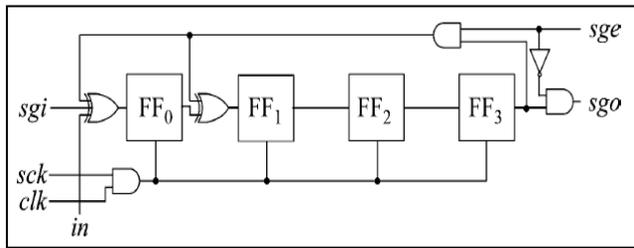


Figure 3: Architecture of Signature Register.

Figure 3. shows the architecture of the signature register for the proposed measurement. It has four flip flops FF0, FF1, FF2, and FF3. . When $sge=1$, it works as a signature register. When $sge=0$, it works as a shift register. The line in is the input of the signature register. The clock line is controlled by sck . When $sck=0$, the signature register does not capture the input value. When $sck=1$, the signature register captures the input value synchronizing with the positive edge of clk . By controlling sck, the signature registers capture only the target test response. The output is sg0. The measurement system requires multiple signature registers generally.

III. DELAY MEASUREMENT SYSTEM

Delay measurement system is shown figure 4. The proposed system consists of the low cost tester and the chip with the variable clock generator (VCG) explained in and a BCD decoder.

The chip is assumed to have single functional clock in the proposed method, and the chip has two reset lines for initializing the flip flops and the signature registers independently. The reset operations are controlled by the tester. The low cost tester controls the whole measurement sequence. The clock frequency tck is slower than the functional clock. The line sg0 retrieves the signature data from the signature registers to estimate the measured delay. The line sci sends the test vectors to the scan input of the chip. The line sc0 gets the data of the flip flops from the scan output of the chip. In the proposed measurement sequence, sc0 is not used. However, it is used to check the flip flops or the additional latches before the measurement. The line cs is the clock control line. The proposed measurement uses both the slow tester clock tck and the fast double pulse generated by on-chip VCG. The line selects the slow and fast clock. If cs is 1, the fast clock is sent to the clock line clk of the components. Otherwise the slow tester clock tck is sent. The lines trg and cnt are the input lines for VCG. The fast double pulse is launched synchronizing with the positive edge of trg . The line cnt controls the width of the double pulse. The line se controls the scan flip flops. The line lck controls the latches for storing test vectors. The lines scj0,

scj1.....scj*l*-1 are the inputs for the encoded data to control the capture operation of the signature registers. The BCD decoder decodes the encoded input data to the control data of the signature registers sck0...sck*m*-1. As explained later, the decoder is used to reduce the input lines for the control data of the signature registers. The sge is the enable signal for the signature registers. The control lines of the signature registers are connected to the BCD decoder.

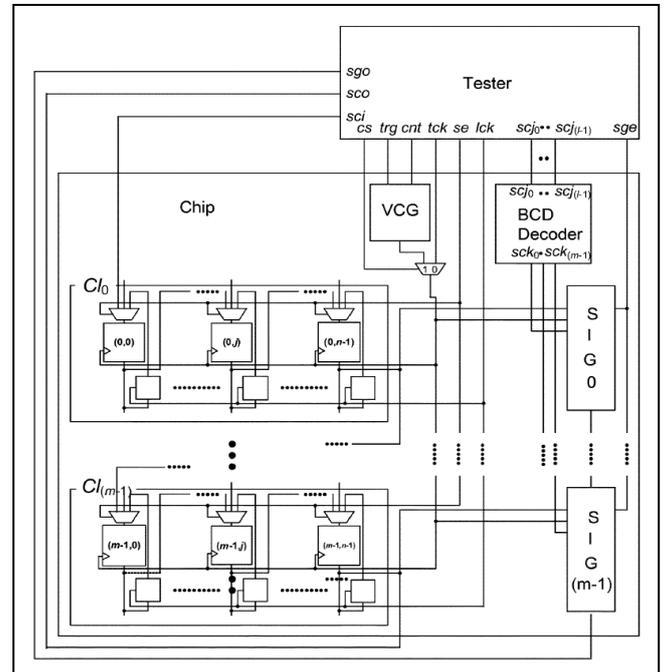


Figure 4: measurement system

Whole Measurement Technique

Assume that the test set for measurement TS has NTV test vectors tv_0, \dots, tv_{NTV-1} . The number of stages of tv_i is $N(i)$. Before measurement, we have to check if the flip flops, the latches, and the clock generator work correctly by applying test vectors. After that the following measurement sequence is executed.

- Step 1:** Initialize the variable $i=0$.
- Step 2:** if i is equal to NTV , finish, otherwise initialize the variable j to 0, and set tv_i to the flip flops with scan-in operation.
- Step 3:** send the values of flip flops to the latches.
- Step 4:** the paths included in STG_j are measured simultaneously. After that, j is updated to $(j+1)$.
- Step 5:** if j equal to $N(i)$, go to step 6, otherwise load the test vector from the latches to flip flops, and go to step 4.
- Step 6:** i is updated to $i+1$, and go to step 2.

IV. SIMULATION RESULTS

1. Variable Clock Generator

The Variable Clock Generator Generates 2 Pulse Signal Output, which is applied to Signature Registers & Scan

Flip Flop for operation. The simulated out put waveform is as shown in below Figure 5.

2. Scan Flip Flops

The Scan Flip Flop uses a D-Flip Flop with Two 2 x 1 Multiplexers. When $Se0 = 1$ and $Se1 = 1$ it sends input Si to output So as shown in Figure 6.

3. Signature Registers

The signature register can be configured to a shift register. The line sge controls the configuration. When $sge = 1$, it works as a signature register. When $sge = 0$, it works as a shift register. The line in is the input of the signature register. During measurement, test responses are sent to in . The line clk is clock line. The clock line is controlled by sck . The following Figure 7 shows the output waveforms for Signature Register.

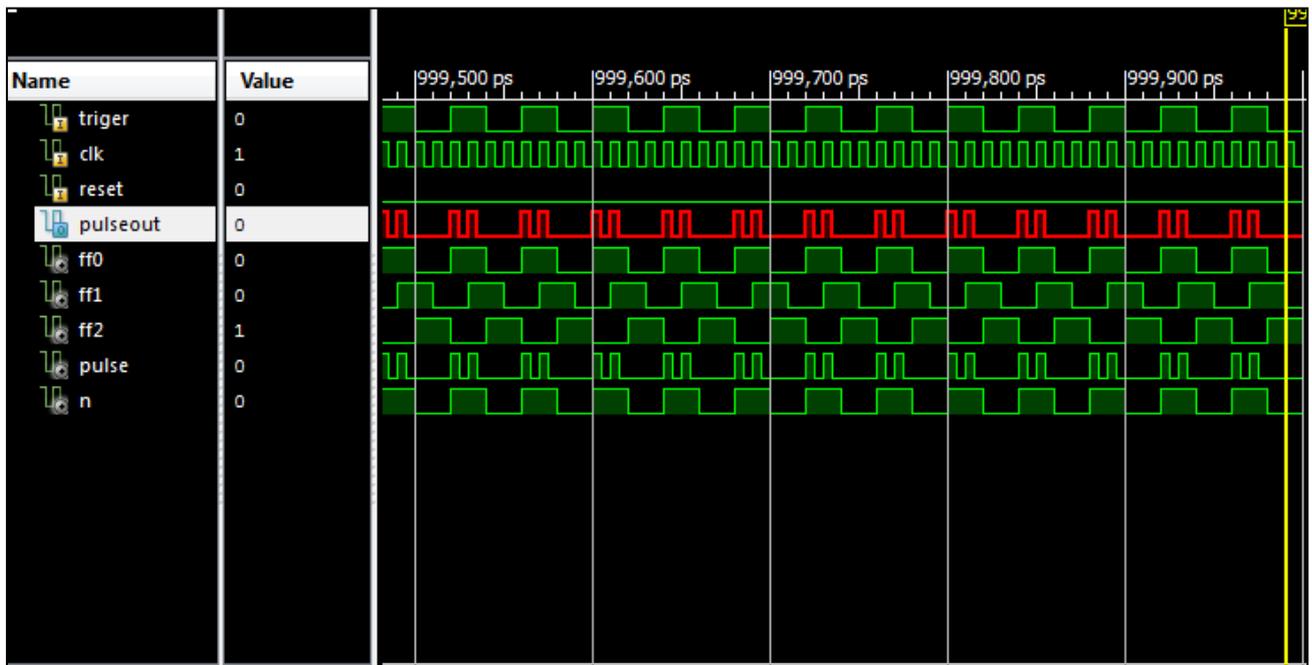


Figure 5: Simulation Output Waveform of Pulse Generator

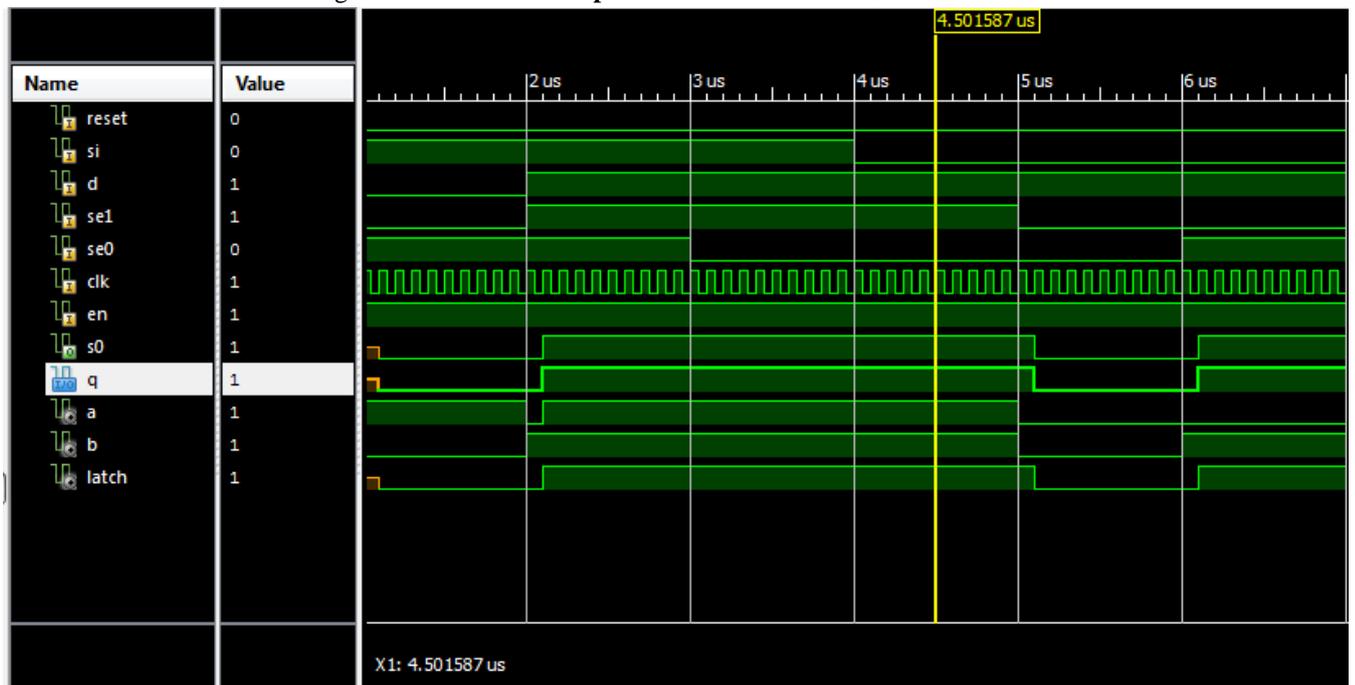


Figure 6: Simulation Output Waveform of Scan Flip-flop

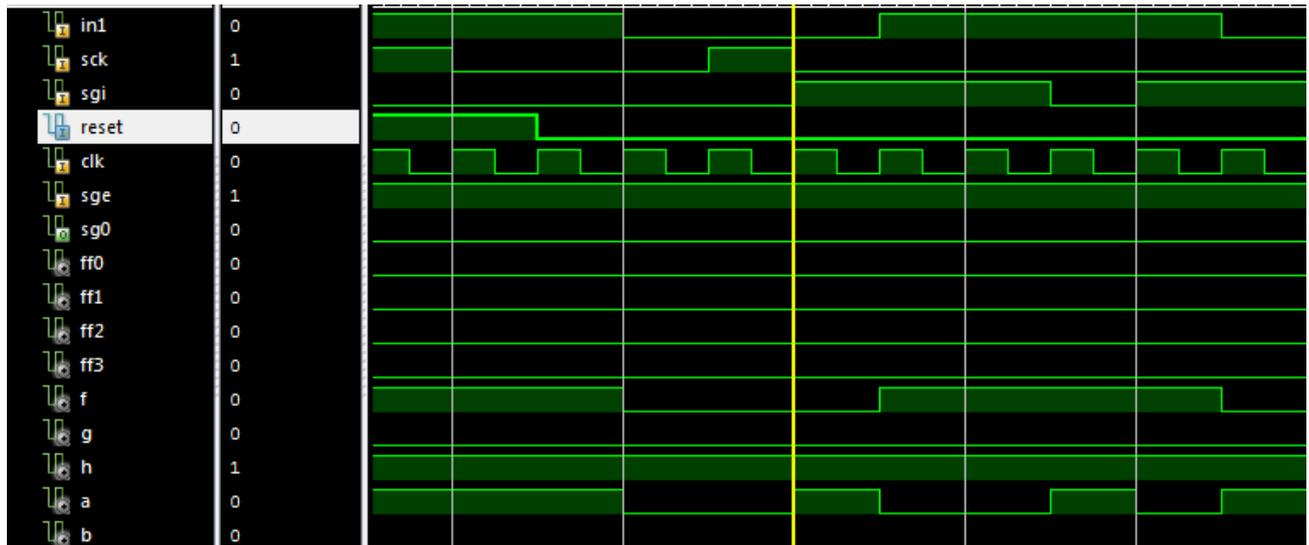


Figure 7: Simulation Output Waveform of signature register

V. CONCLUSION

We have presented measurement technique based on signature analysis, for screening small-delay defects and we also generated an on-chip variable clock generator for double pulse width and latches for short measurement time in scan design and compared with standard scan design. A future work is extension of cluster and implementation of FPGA with low cost application.

REFERANCES

- [1] K. Noguchi, K. Nose, T. Ono, and M. Mizuno, "An area reduction technique of self-testing FFs for small-delay defects detection," *The Inst. Electron., Inf. Commun. Eng. (IEICE), Tech. Rep. DC2009-16*, 2009.
- [2] N. Ahmed and M. Tehranipoor, *Nanometer Technology Designs: High-Quality Delay Tests*. New York: Springer, 2007.
- [3] K. Noguchi, K. Nose, T. Ono, and M. Mizuno, "A small-delay defect detection technique for dependable LSIs," in *Proc. IEEE Symp. VLSI Circuits*, 2008, pp. 64–65.
- [4] Dervisoglu and G. E. Stong, "Design for testability: Using scan-path techniques for path-delay test and measurement," in *Proc. IEEE Int. Test Conf. (ITC)*, 1991, pp. 365–374.
- [5] K. Noguchi, K. Nose, T. Ono, and M. Mizuno, "An area reduction technique of self-testing FFs for small-delay defects detection," *The Inst. Electron., Inf. Common. Eng. (IEICE), Tech. Rep. DC2009-16*, 2009.