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Design and analysis of efficient Class-E power amplifier: an application for 2.4GHz band communication

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Abstract- **In present days use of wireless communication devices are increasing drastically for communication. Because of huge wireless communication there are chances for loss of signal strength. To increase the strength of weak signal, power amplifier plays important role in wireless communication. The people are demanding for high quality, low cost and low power consumption wireless devices. From referred IEEE papers and journals it has been observed that, the power amplifier design suffers from high power consumption to achieve wide bandwidth and efficiency. This paper aims to design and verify the different performance parameters of power amplifier to improve efficiency. This paper is proposing a design of Class-E power amplifier to achieve high efficiency at low power consumption. Either by reducing the input DC power level or by scaling the MOS device. In this paper efficient class-E power amplifier is designed by using 180nm technology. The wireless communication devices with our designed Class-E power amplifier will give better performance and high efficiency at low power consumption. For the applications such as Bluetooth and Wi-Fi.**

Index Terms **- Class-E, CMOS, power amplifiers (PA), PAE.**

I. INTRODUCTION

In present days demand for high quality, low cost and low power wireless devices has drastically increased. The researches for low power wireless devices shows high demand in competitive market. By using 180nm Technology there is lot of wireless devices are available, but these devices consumes more power. So as to design 180nm wireless devices at low power consumption we designed Class-E power amplifier. The devices with Class-E power amplifier will give better performance and high efficiency.

The main objective of this paper is to design an efficient power amplifier to be used in 2.4GHz Band Communication. To achieve low power consumption and also to understand the design of matching network and how matching network is helpful in the design of power amplifier.

From the study of existing papers it has been observed that power amplifier design suffers from high power consumption to achieve wide bandwidth over large Geographical area and efficiency. This project aims to design and verify different performance parameters of power amplifier to improve the efficiency specifically in 2.4GHz band.

The proposed system is designed for achieving low power consumption for wide bandwidth and to improve efficiency of PA by either of following methods:

1. By scaling of MOS device (W/L ratio).
2. By decreasing the input DC power Level.

II. DESIGN OF CLASS-E POWER AMPLIFIER

Design of Class-E PA is depends how we choose Inductor and Capacitor. For Class-E design, biasing of Transistor is important and is biased such that, before current start flow through the Transistor, voltage goes to zero. It means there is no overlap between voltage and current. To do this we are using higher order reactance. So we should use very large Inductor and very large Capacitor.

The basic configuration of Class-E power amplifier is shown in below Fig 1.

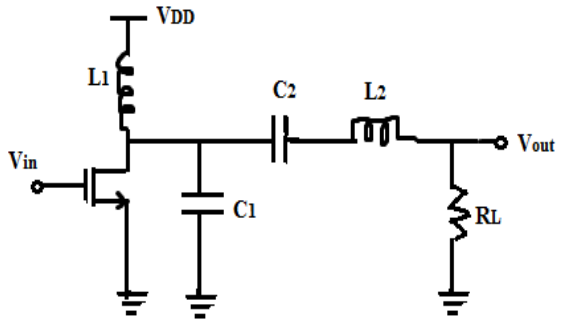

Figure 1: Basic configuration of class-E PA

- Large Inductor (BFL), L1 – Helps in constant current flows through transistor. BFL acts as current source. Advantage of using BFL is it biases the output to Vdd.

- Large Capacitor (BFC), C1 – Use of BFC avoids DC current flowing through the load RL.
- LC Resonant circuit – At Resonance LC resonant circuit has high impedance. So some current flows through the load and remaining current is bypassed.
- Load resistance R – The value of load is 50 ohm. Since the antenna is pure resistor which has 50 ohm. We can change this value by using impedance matching, depending on what power we have to deliver.
- Advantages of using BFC and BFL –
  1. The transistor output capacitance can be absorbed into tank circuit.
  2. These helps in filtering which reduce the frequency on out of band.

III. DESIGN EQUATIONS

For Analog design, before designing, we have to consider some design constraints. In this project I am designing power amplifier for the output power of 15dBm, at frequency 2.4 GHz under 1.8V supply voltage. A non-linear power amplifier can be used to achieve high efficiency. Among all classes of non-linear power amplifiers, the class-E power amplifier is the best Power Amplifier which is sophisticated to design and has high efficiency performance.

The Drain current equation for Transistor, which is in saturation region is given by:

$I_D = ½\ \mu_n C_{ox} (W/L) (Vgs – Vth)^2$ …….... (1)

Maximum output power is calculated as i.e.

$$Pout(max) = \frac{0.577\ Vdd^2}{R} \quad \text{……...….. (2)}$$

The output matching network is designed to match the output signal of amplifying circuit with antenna. In this LC tank circuit is used for matching. The tank circuit is mainly for tuning the output part of the circuit to the operating frequency of 2.4 GHz. The values of tank circuit is calculated from below equations

$\omega = 2\pi f$ ……... (3)

$$L_2 = \frac{\pi Vdd^2}{2\omega Pout}\ \frac{\pi^2-4}{\pi^2+4} \quad \text{……..(4)}$$

$$\omega = \frac{1}{\sqrt{L_2 C_2}} \quad \text{……(5)}$$

$$\sqrt{L_2 C_2} = \frac{1}{\omega}$$

Then,

$$C_1 = \frac{Pout}{\pi\omega Vdd^2} \quad \text{……. (6)}$$

For design of perfect input matching an inductors is connected between the drain and supply. The drain inductance L1 value is varied accordingly to be tuned resonance frequency of 2.4GHz.

The reactance of L_1 is larger than ten times the reactance of C_1:

$$X_{L1} > 10X_{C1}$$

Every circuit has its own input and output impedances. Before applying matching networks to any circuit, the input and output side were terminated by impedances of 50 ohms. The transistor should be in saturation region for conducting the current.

IV. RESULTS AND DISCUSSION

The technology used for this paper is 180nm technology. The maximum power added efficiency achieved in this paper is 66.11% and output power is 15dBm for the supply of 1.8v, at frequency 2.4 GHz. The comparison is shown in below Table 1.The schematic diagram of proposed class-E power amplifier is shown in fig 1.

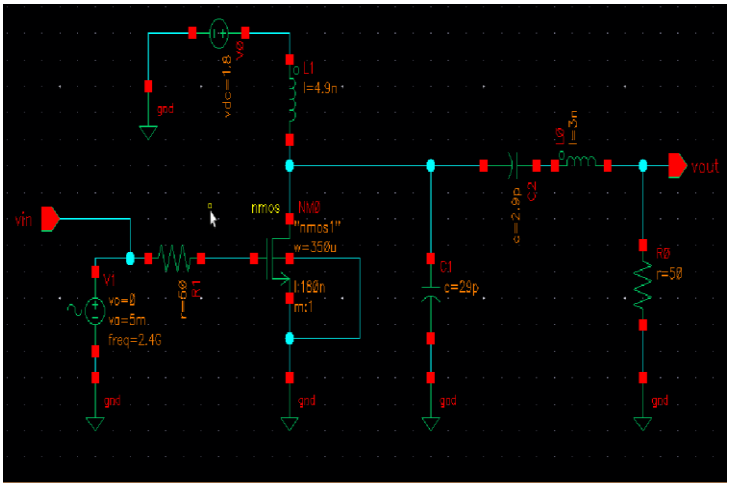

Figure 2: Schematic of proposed Class-E PA

The transient analysis of proposed system is shown in fig 3. In this we are observing the output voltage.

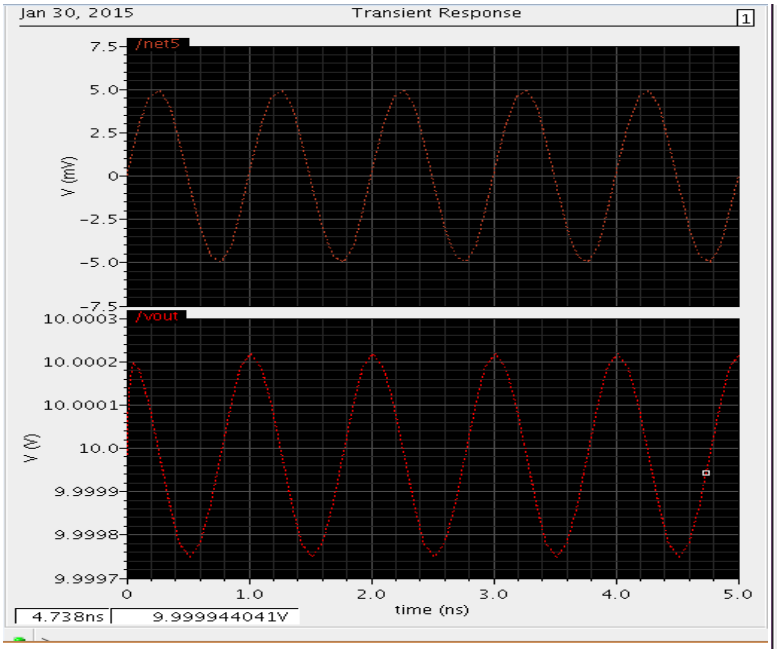

Figure 3: Input and Output waveforms of proposed class-E PA

The AC response gives the graph of output voltage vs. frequency. The AC response of proposed system is shown in fig 4.

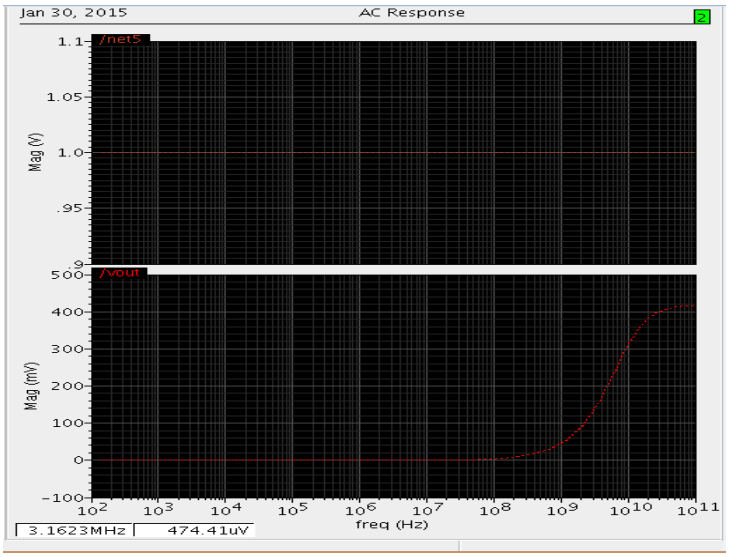

Figure 4: AC response of proposed Class-E PA

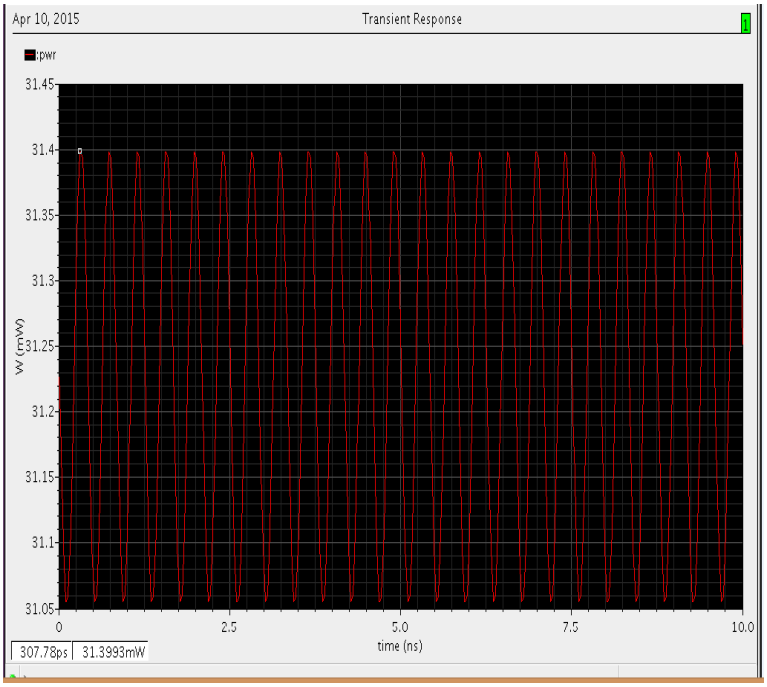

Figure 5: Output Power waveform of proposed Class-E PA

Power analysis of proposed system shown in fig 5. From the waveform we are observing the output power is about 31.399mw. Which is shown on y-axis in fig 5.

Table 1: Comparison of proposed system with referred paper

Year	2005	2007	2009	2010	2015
Reference	[7]	[8]	[2]	[1]	This work
Technology (nm)	180	180	180	180	180
Supply voltage (v)	1.8	1.8	1.8	3.3	1.8
Frequency (GHz)	2.4	1.9	2.4	1.8	2.4
Output power	22dBm	1.6w	20dBm	2w	15dBm
Efficiency (%)	44	40	62	31	66.11

V. CONCLUSION

This paper is designed for efficient power amplifier to get output power of 15dbm (32mw) and efficiency of about 70% from input sine wave of amplitude 10mv, at frequency of 2.4 GHz. But obtained result of output power is 14.96dbm

(31.39mw) and efficiency is about 66.11% and possible applications of the paper in short distance communication like Wi-Fi, Bluetooth. The main aim of this paper is to improve the efficiency.

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REFERENCES

[1] Ockgoo Lee et al., "*Analysis and design of fully integrated high-power parallel-circuit class-E CMOS power amplifiers"*, IEEE Transactions on circuits and systems-I: Regular papers, vol. 57, No.3, pp. 724-734 March 2010.

[2] Donald Y.C. Lie et al., *"Highly efficient monolithicclass-E SiGe power amplifier design at 900 and 2400 MHz"*, IEEE Transactions on circuits and systems-I: regular papers, vol. 56, No.7, pp. 1455-1466, July 2009.

[3] N. Sokal and A. Sokal, *"Class E – A New Class of High-Efficiency, Tuned Single-Ended Switching Power Amplifier"*. IEEE J. Solid-State Circuits, vol. Sc-10, no. 3, pp. 168-176, June 1975.

[4] Jun Tan, Chun-Huat Heng, and Yong Lian, *"Design of Efficient Class-E Power Amplifiers for Short-Distance communications"*, IEEE Transactions on circuits and systems – I: Regular papers, Vol. 59, No.10, and October 2012.

[5] T.Sowlati and D.Leenaerts, *"A 2.4 GHz 0.18-um CMOS self-biased cascade power amplifier"*, IEEE Journal of solid-state Circuits, vol. 38, issue 8, 2003, pp. 1318-1324.

[7] Y.Ding and R.Harjani, *"A high-efficiency CMOS +22-dBm linear power amplifier"*, IEEE Journal on Solid-state Circuits, vol. 40, No.9, pp. 1895-1900, Sep. 2005.

[8] Park et al., *"A 1.9-GHz CMOS power amplifier using three-port asymmetric transmission line transformer for a polar transmitter"*, IEEE Transactions on Microwave theory technology, vol. 55, No.2, pp. 230-238, Feb. 2007.

[9] Thomas H Lee –"The design of CMOS Radio Frequency Integrated Circuits", New York: Cambridge University, Press, 2004.

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