Area-Delay Efficient Binary Adders in QCA

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***Abstract*- As transistors decrease in size more and more of them can be accommodated in a single die, thus increasing chip computational capabilities. However, transistors cannot get much smaller than their current size. The quantum-dot cellular automata (QCA) approach represents one of the possible solutions in overcoming this physical limit, even though the design of logic modules in QCA is not always straightforward. In this brief, we propose a new adder that outperforms all state-of-the art competitors and achieves the best area-delay tradeoff.**

***Index Terms*- Adders, nanocomputing, quantum-dot cellular automata (QCA).**

I. INTRODUCTION

In this paper, a new QCA adder design is implemented thatreduces the number of QCA cells when compared toexistingreported designs. We demonstrate that it is possible to design aCLA QCA one-bit adder, with the same reducedhardware asthe bit-serial adder, as retaining the simpler clockingscheme and parallel structure of the novel CLAapproach.The proposed design is based on a new algorithm thatrequires only three majority gates and two inverters fortheQCA addition. It is noted that the bit-serial QCA adder uses avariant of the proposed one-bit QCA adder. Byconnectnproposed one-bit QCA adders.

Quantum-dot cellular automata (QCA) is an attractiveemerging technology suitable for the development ofultra dense low-power high-performance digitalcircuits. For this reason, in the last few years, thedesign of efficient logic circuits in QCA has receiveda great deal of attention. Special efforts are directedto arithmetic circuits, with the main interest focusedon the binary addition that is the basic operation ofany digital system. Of course, the architecturescommonly employed in traditional CMOS designs areconsidered a first reference for the new designenvironment. Ripple-carry (RCA), carry look-ahead(CLA), and conditional sum adders were presented.

Theoreticalformulations demonstrated for CLA and parallel-prefixadders are here exploited for the realization of a novel 2-bitaddition slice as shown in Fig.1. The latter allows the carry tobe propagated through two subsequent bit-positions with thedelay of just one majority gate (MG).In addition, the clever top level architecture leads to verycompact layouts, thus avoiding unnecessary clock phases dueto long interconnections. An adder designed as proposed runsin the RCA fashion, but it exhibits a computational delaylower than all state-of the-art competitors and achieves thelowest area-delay product (ADP).

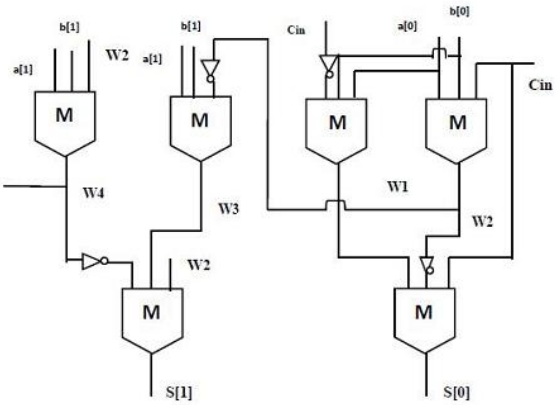


Fig 1 Novel 2-bit basic module

Parallel-prefix architectures,including Brent–Kung (BKA), Kogge–Stone, Ladner–Fischer, and Han–Carlson adders, were analyzed andimplemented in QCA. Recently, further efficient designs were proposed for the CLA and the BKA, and for the CLAand the CFA. In this brief, an innovative technique is presented to implement high-speed low-area adders into QCA.Theoretical formulations established for CLA and parallel-prefix adders are here exploited for the realization of a novel2-bit

addition slice. The latter allows the carry to be propagated through two subsequent bit-positions with the delay ofjust one majority gate (MG). In addition, the clever top level architecture leads to very compact layouts, thus avoidingunnecessary clock phases due to lengthy interconnections.

II. RELATED WORKS

QCA is based on the interface of bi-stable QCA cellsconstructed from four quantum-dots. A high-level design of two polarized QCA cells is shown in Fig. 2. Each cell isconstructed from four quantum dots arranged in a squarepattern. The cell is charged with two electrons, which are free of chargeto tunnel between adjacent dots. These electrons tend totake up antipodal sites as a result of their mutual electrostaticrepulsion. Thus, there exist two equalenergeticallyminimal arrangements of the two electrons in the QCA cell asshown in Fig. 2. These two arrangements are denoted as cellpolarization P = +1 and P = -1 correspondingly. By using cellpolarization P = +1 to represent logic "1" and P = -1 torepresent logic "0", binary information can be encoded.

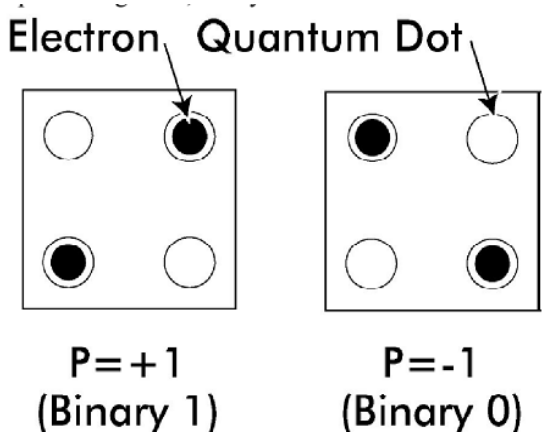


Figure 2 QCA cells

Arrays of QCA cells can be set to perform all logicfunctions. This is owed to the Columbic interactions,whichinfluences the polarization of neighboring cells. QCAdesigns have been proposed with potential barriersbetweenthe dots that can be controlled and used to clock QCAdesigns. The fundamental QCA logic devices are the QCA wire,majority gate and inverter.

QCA wire: In a QCA wire, the binary signal propagatesfrom input to output because of theColumbicconnectionsbetween cells. This is a result of the system attempting to settleto a ground state. Any cells alongthe wire that are anti-polarizedto the input would be at a high energy level, andwould soon settle to the correct groundstate. The propagationin a 90-degree QCA wire is shown in Fig. 4. Other than the 90-degree QCA wire, a 45-dgreeQCA wire can also be used. Inthis case, the propagation of the binary signal alternatesbetween the two polarizations.

Advance, there exists a so-callednon-linear QCA wire, in which cells with 90-degree orientationcan be placed next toone more, but off center.

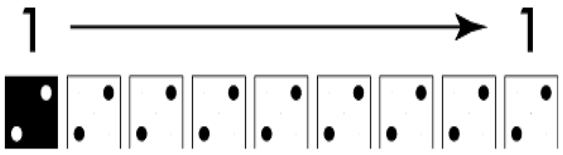


Figure 3 A QCA wire (90-degree)

Structure of Majority gate: Themajoritygate performs a three-input logic function. Assumingthe inputs are A, B and C, the logic function of the majoritygate is

m(A, B,C) = A|B + B|C + A|C …….(1)

By fixing the polarization of one input as logic "1" or "0", wecan get an OR gate and an AND gate respectively.Morecomplex logic circuits can then be designed from OR andAND gates.

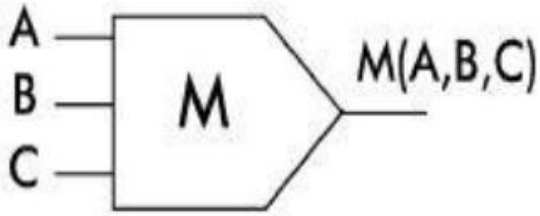
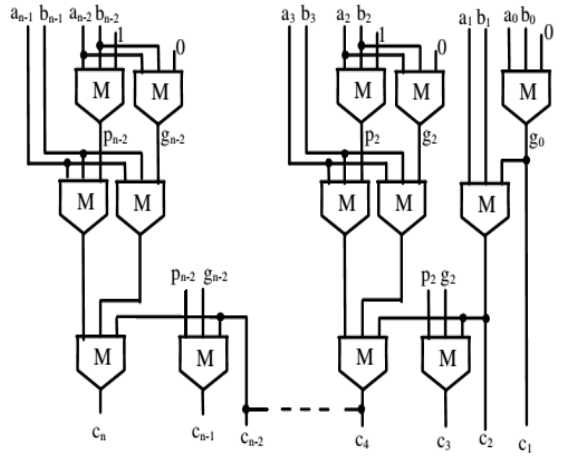


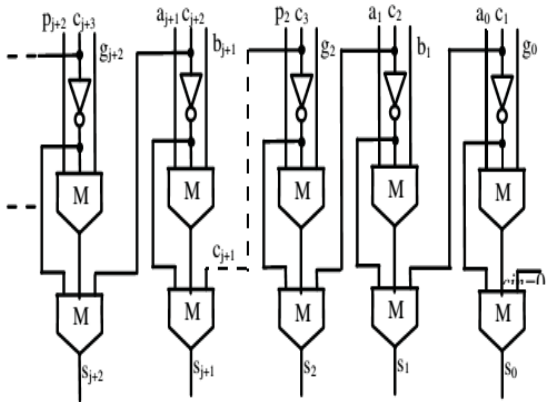
Fig: Structure of Majority gate

In this brief, an innovative technique is presented toimplement high-speed low-area adders in QCA. CLAand parallel-prefix adders are here exploited for therealization of a novel 2-bit addition slice. The latterallows the carry to be propagated through twosubsequent bit-positions with the delay of just onemajority gate (MG). In addition, the clever top levelarchitecture leads to very compact layouts, thusavoiding unnecessary clock phases due to longinterconnections. An adder designed as proposed runsin the RCA fashion, but it exhibits a computationaldelay lower than all state-of the- art competitors andachieves the lowest area-delay product (ADP).

Several designs of adders in QCA exist in literature.The RCA [11], [13] and the CFA [12] process n-bitoperands by cascading n full-adders (FAs).



(a)



(b)

Fig. 2. Novel n-bit adder (a) carry chain and (b) sum block.

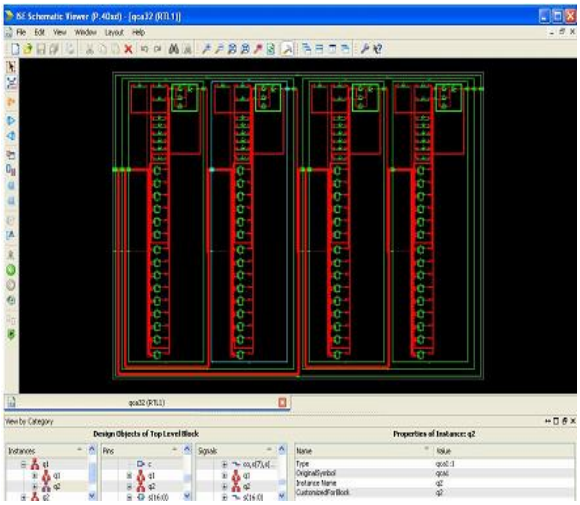
Even thoughthese addition circuits use different topologies of the genericFA, they have a carry-in to carry-out path consistingof one MG, and a carry-in to sum bit path containing two MGs plus one inverter. As a consequence, theworst case computational paths of the n-bit RCA and then-bit CFA consist of (n+2) MGs and one inverter.

III. PROPOSED SYSTEM STRUCTURE

To introduce the novel design proposed for implementing ripple adders in QCA, let consider two n-bit addends $A = a_{n-1}, \ldots . a_0$ and $B = b_{n-1}, \ldots . b_0$and suppose that for the i th bit position (with i = n − 1, . . . , 0) the auxiliarypropagate and generate signals, namely$p_i = a_i + b_i$ and $g_i = a_i, b_i$ are computed c_i being the carry produced at the generic (i−1)th bit position, the carry signal ci+2, furnished atthe (i+1)th bit location, can be computed using the conventional CLA logic reported in (2). The latter canbe rewritten as given in (3), by exploiting Theorems 1 and 2demonstrated in [15]. In this way, the RCA action, neededto propagate the carry ci through the two subsequent bitpositions, requires only one MG. Conversely, conventionalcircuits operating in the RCA fashion, namely the RCA andthe CFA, require two cascaded MGs to perform the sameoperation.

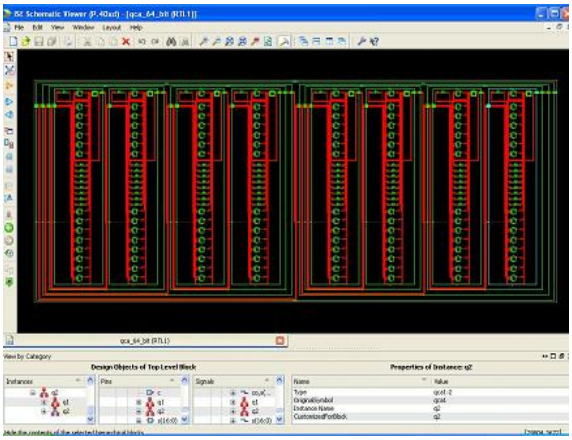
ci+2 = gi+1 + pi+1 · gi + pi+1 · pi · ci…… (2)

ci+2 = M(M (ai+1, bi+1, gi) M (ai+1, bi+1, pi) ci). ……(3)



Novel 32-bit adder

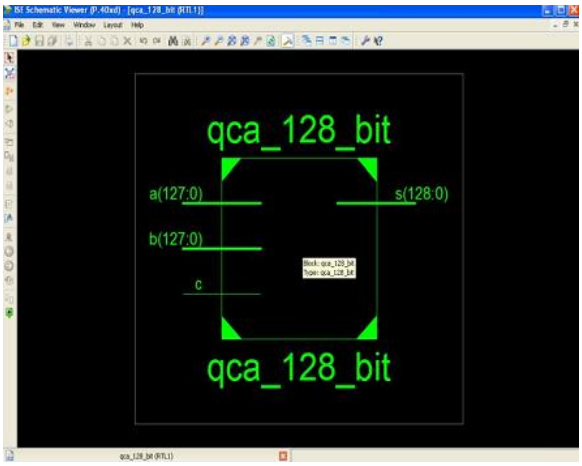
It must be noted that the time critical addition is performed when a carry is generated at the least significant bit positionand then it is propagated through the subsequent bit positions to the most significant one. In this case, the first 2-bitmodule computes c_2, causal to the worst case computational path with two cascaded MGs. The subsequent 2-bitmodules contribute with only one MG each, thus introducing a total number of cascaded MGs equal to (n − 2)/2.Considering that additional two MGs and one inverter are required to compute the sum bits, the worst case path of thenovel adder consists of (n/2) + 3 MGs and one inverter.



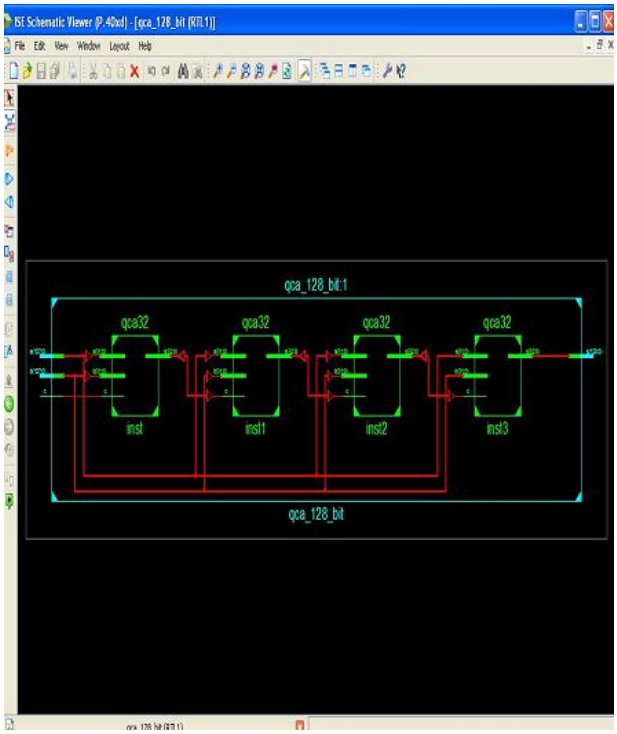
Novel 64-bit adder

IV. SIMULATION RESULTS

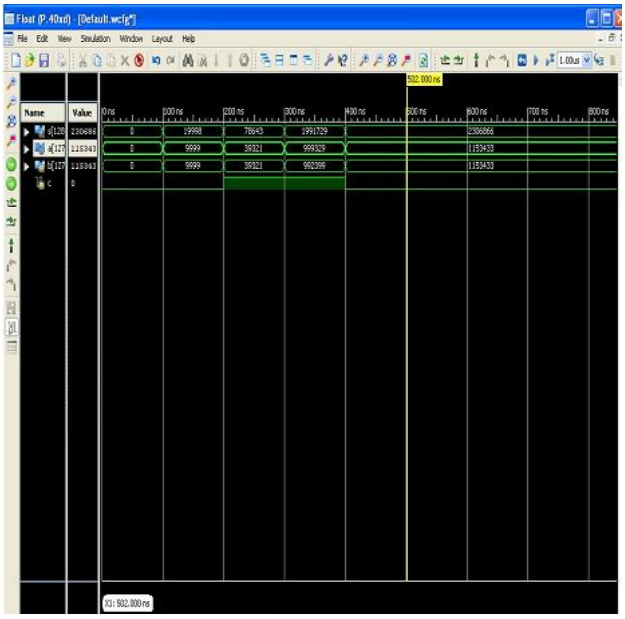
The proposed addition design is implemented for several operands word lengths using the QCA Designer tooladopting the same rules and simulation settings used.



Block diagram



RTL schematic



Simulation output

V. CONCLUSION

A new adder designed in QCA was presented. It achievedspeed performances higher than all the existing QCA adders,with an area requirement comparable with the cheap RCAand CFA demonstrated. The novel adder operated in theRCA fashion, but it could propagate a carry signal through anumber of cascaded MGs significantly lower

thanconventional RCA adders. In addition, because of theadopted basic logic and layout strategy, the number of clockcycles required for completing the elaboration was limited.

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