DESIGN OF COMPARATOR USING DIFFERENT LOGIC STYLES OF FULL ADDER

K. Tharun Teja[1], Satya Pratiksh Reddy Cheruku[2], Chinthareddy Sri Sai Ravali[3]
[1]*B.Tech Student, Dept. Of ECE, CVR College Of Engineering, Hyderabad.*
[2]*B.Tech Student, Dept. Of ECE, Sreyas Institute Of Engineering&Technology, Hyderabad.*
[3]*B.Tech Student, Dept. Of ECE, CVR College Of Engineering, Hyderabad.*

***Abstract*- In this paper, a new design of comparator is described with the help of Full adders which are the integrated blocks of an ALU in this 21st century and ALU is a basic functional unit of the Microprocessor and Digital Signal Processing. In the world of technology, it has become very essential to develop new design methodologies to reduce the power consumption. In this paper, comparator is developed using various design styles of full adder. We have also calculated and compared the power consumption by different logic styles implemented.**

***Index Terms*- Full Adder, Comparator, Inverter, Half Adder, XOR, MUX.**

I.INTRODUCTION

The Comparator is a very basic and the most useful arithmetic component of any digital circuit or a system. There are many approaches of designing CMOS comparator, each with different operating speed, power consumption, and circuit complexity. We can implement a comparator by flattening the logic function directly. A full adder is one of the basic building blocks of most of the digital VLSI circuits. Several improvements have been made regarding its structure since it has been first designed. The main aim of these modifications is to reduce the number of transistors to be used to perform a required logic function, reduce the power consumption and increase the speed of operation. One of the ways to reduce the power consumption is to explore new ways of designing circuits in order to find better circuit techniques for energy savings. In this paper, we implement 8 bit comparator in 3 different logic styles. They are:-

- Logic style 1:- It is a basic full adder constructed using 2 half adders.
- Logic style 2:- It is a hybrid full adder constructed using a mux.
- Logic style 3:- It is a full adder designed using logic.

Finally, we conclude the paper by comparing power consumption using the three logic styles and provide the most efficient technique

II.MAGNITUDE COMPARATOR

Magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitude [1]. The outcome of comparison is specified by three binary variables that indicate whether B>A, A=B. If there is a high (logic 1) output at B>A then the number B is greater, similarly if there is a high (logic 1) output at A=B then both the numbers A and B are equal. If both the outputs are low (logic 0) then A>B.

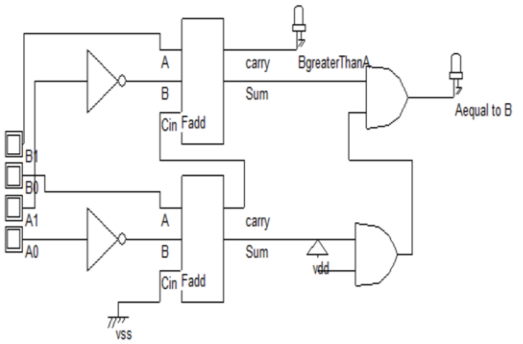

Fig 2.1: Basic Structure of Magnitude Comparator

III. 8-BIT FULL ADDER

A 2-bit full adder based comparator consists of 2 full adders, 2 inverters at one of the input and 2 AND gates at the output side. There are two outputs. One shows A=B and another shows B>A. Similarly, an 8 bit comparator consists of 8 full adders, 8 inverters at one of the input and 8 AND gates at the output side. There are two outputs, A=B and B>A. For 8 bit comparator the carry of the 2nd full adder is given to the input 'Cin' of the 3rd full adder ,similarly the output of

the 2nd AND gate is given to the input of the 3rd AND gate and so on. Finally the outputs A=B is obtained at 8th AND gate and B>A is obtained at carry of the 8th full adder.

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig 3.1: Truth Table of Full Adder

A. Logic style 1

This is a basic full adder. In this style the full adder is constructed using 2 half adders [2]. Half adder has 2 inputs bits and sum, carry as outputs. The logical circuit of half adders is shown if fig 3.2.

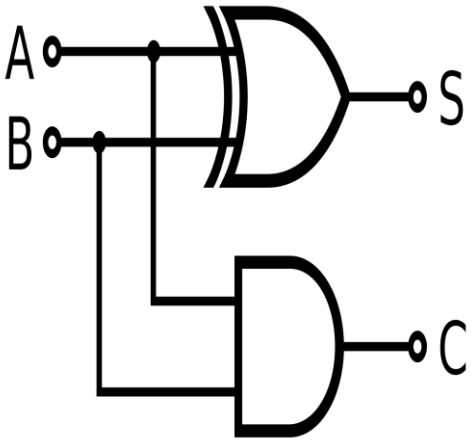

Fig3.2: Half adder Logic circuit

The half adder consists of 1 XOR gate and 1 AND gate. Sum is obtained but performing XOR operation between the inputs A, B and carry is obtained by performing AND operation between the inputs A, B.

The output equations of sum and carry are given by:

Sum= A (XOR) B

Carry=A.B

B. Logic Style 2

The Hybrid full adder consists of a 2 XOR gates, 1 2*1MUX [1]. Sum is calculated by performing XOR operation between the 3 inputs and carry is obtained by selecting one of the inputs A or C depending on the output of XOR of A, B.

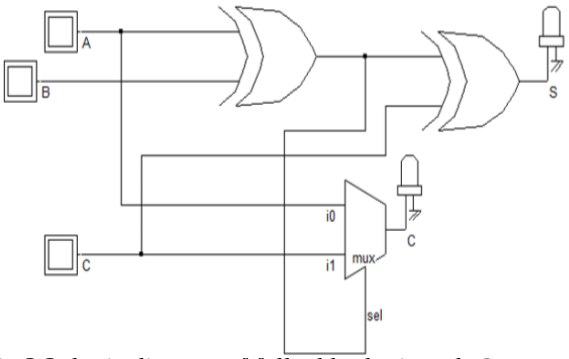

Fig 3.3: logic diagram of full adder logic style 2

The equations are as follows:

Sum = A (XOR) B (XOR) C

S = A (XOR) B = AB'+A'B

Hence C=A.(AB'+A'B)'+C(AB'+A'B)

C=A(AB+A'B')+C(AB'+A'B)

Carry=AB+ C(A (XOR) B)

C. Logic Style 3

This logic style consists of 2 XOR gates, 3 AND gates, 1 OR gate [1]. Sum is obtained by performing XOR operation on all the inputs and carry is obtained by performing AND operation on every two combinations of inputs and finally they are given to a OR gate.

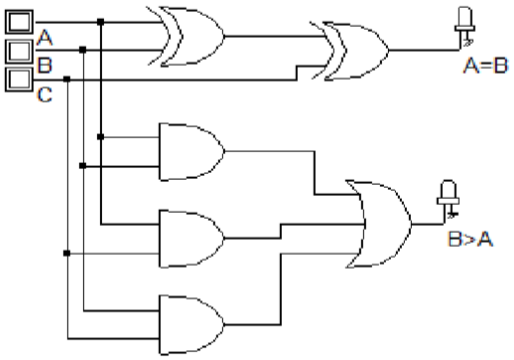

Fig 3.4: logic diagram of full adder logic style 3

IV. IMPLEMENTATION OF FULL ADDER

The implementation of the circuit is shown in fig 4.1. This circuit is verified by a test bench circuit in fig 4.2. Various inputs (in form of pulses) are provided at the input pins and the outputs of the circuit are obtained and verified. In the left of the circuit we have the input pins A(a0,a1,a2,a3,a4,a5,a6,a7) and B(b0,b1,b2,b3,b4,b5,b6,b7). On the top right we have output pins B>A, B=A.

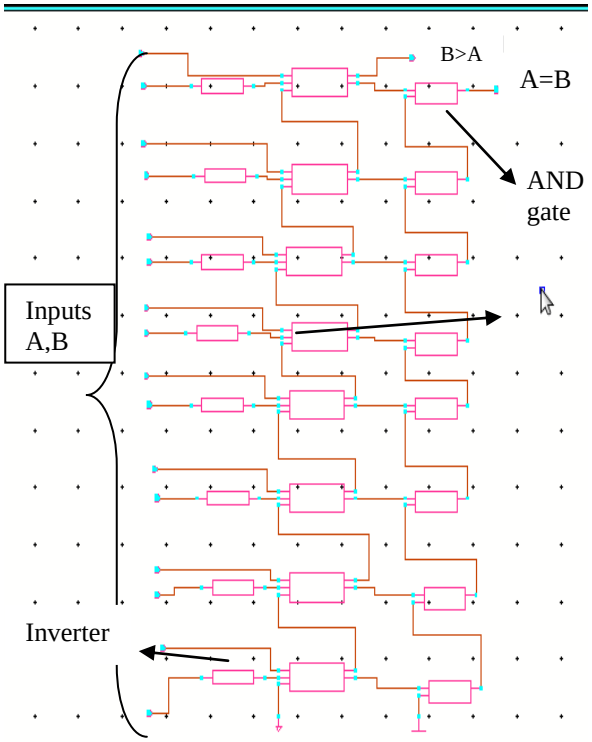

Fig 4.1 Comparator using Full Adder

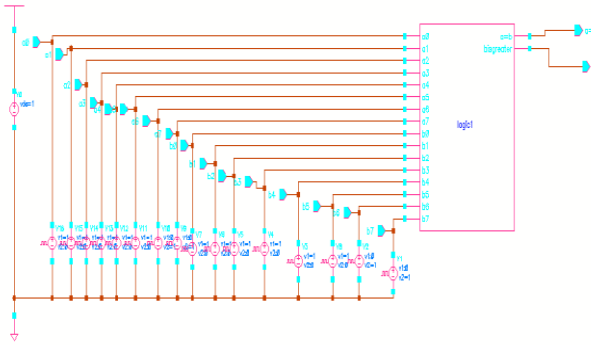

Fig 4.2: Test bench for comparator using full adder

The Waveforms obtained when the test bench of comparator using different logic styles of the Full adder is shown below. The output is verified and it is declared that all the logic styles work accurately.

The Waveforms are as shown below:

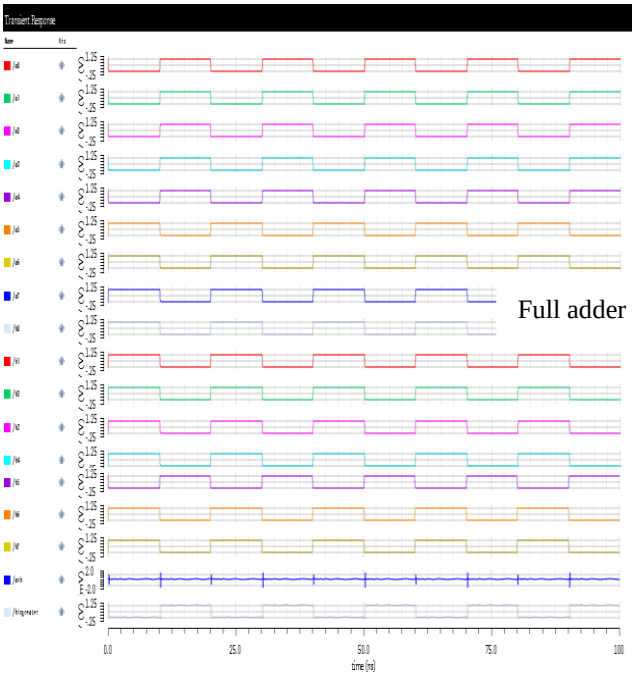

Fig 4.3 Waveforms of Comparator

A. Logic Style 1

Full Adder Logic Style 1 is designed using 2 half adders and OR gate. The circuit is as follows:

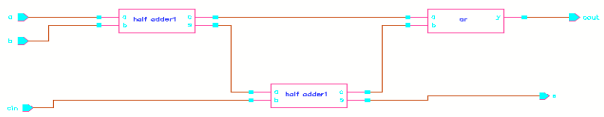

Fig 4.4.1: Full Adder using logic style 1

The power consumed is obtained as 2.63E-6 milliWatts.

Fig 4.4.2: Power Consumed using logic style 1

B. Logic Style 2

Full Adder Logic Style 2 is designed Using 2 XOR and 2*1 MUX. The circuit is as follows:

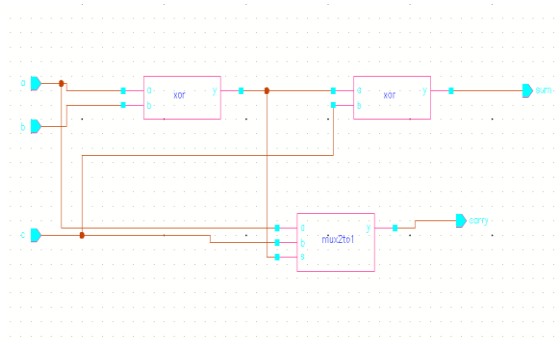

Fig 4.4.3: Full Adder using logic style 2

The power consumed is obtained as 2.409E-6 milliWatts.

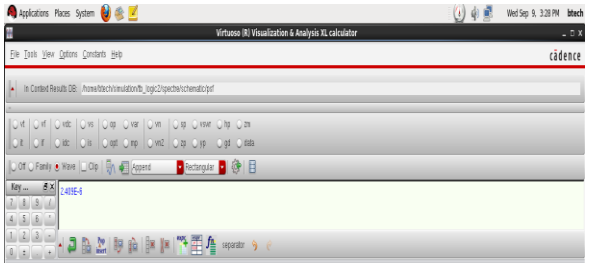

Fig 4.4.4: Power Consumed using logic style 2

C. Logic Style 3

Full Adder Logic Style 2 is designed Using 2 XOR ,3 AND, 1 OR gates. The circuit is as follows:

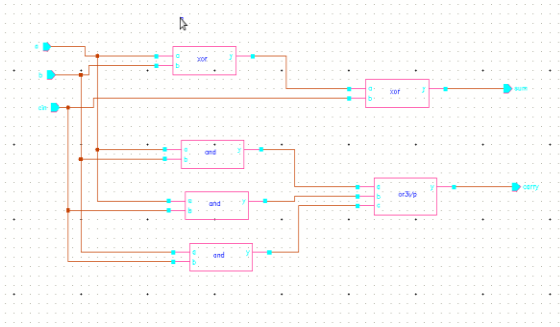

Fig 4.4.5: Full Adder using logic style 3

The power consumed is obtained as 2.092E-6 milliWatts.

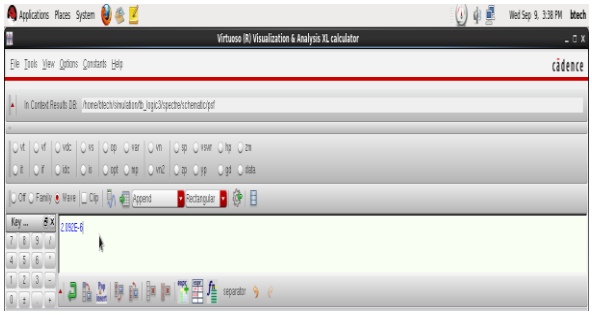

Fig 4.4.6: Power Consumed using logic style 3

V. COMPARISON OF POWER CONSUMPTION FOR 3 DIFFERENT STYLES

Comparator styles	Power consumption
Logic style 1	2.63E-6 milli watts
Logic style 2	2.409E-6 milli watts
Logic style 3	2.096E-6 milli watts

Table 5.1: power consumption of 3 comparators

VI. CONCLUSION

All the comparator circuits designed using different styles of full adder are perfectly operational. The comparator designed using logic style 3 of full adder consumes less power than the full adders which are designed using the logic style 1 and logic style 2.. Hence it can be concluded that the comparator designed using the 3rd logic style of full adder is the best circuit in terms of power consumption.

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