SIMULATION AND ADVANTAGES OF A DOUBLE TAIL COMPARATOR

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***Abstract*— Single tail comparators have higher input impedance. Due to the presence of high input resistance, the power consumed is low which results in less static power consumption. Moreover, it has no loss in voltage from VDD to ground which results in rail to rail output swing. But, it has only one path for the current to flow in the circuit and more number of transistors are present in the top half of the circuit which represents stacking and due to this high supply voltage is consumed for circuit operation. In order to overcome these limitations, Double tail comparator is considered.**

Index Terms*: *ADC, Cadence, Spice, 90nm

I. Introduction

Single tail comparator [1] provides a higher input impedance. It also has high input resistance, so the power consumed is low which results in less static power consumption. Moreover there is also no loss in voltage from VDD to ground which results in rail to rail output swing. The tail transistor increases the speed of the circuit when compared to the pre amplifier circuit as fast switching of PMOS and NMOS occurs. The single tail comparator is shown below [2]

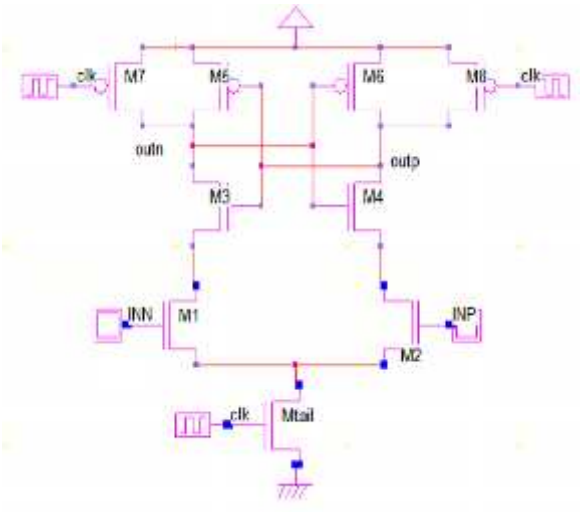

Fig 1 - Single tail comparator

But it has only one path for the current to flow in the circuit. As more number of transistors present in the top half of the circuit, it experiences stacking and due to this high supply voltage is consumed for circuit operation. To overcome these limitations, we go for the change in the circuit by adding another tail transistor making it a double tail comparator.

Thus, we design a double tail comparator using Cadence software tools.

II. Tool Description

Cadence tools with full custom VLSI design is to be implemented. MOS transistor level design entry using Schematic/Symbol/Simulation is the starting level. Transient analyses simulation is done by using SPICE model files. The following order is implemented:

Design entry – MOS transistor level design entry – Library – GPDK 90nm

A. Schematic Design

The transistor level schematic is designed by using CMOS logic. This consists of pull up network with PMOS transistors connected between VDD and GND. The schematic design is entered by using **Virtuoso(R) Schematic Editor- XL 6.1.6**

B. Symbol Creation

The symbol view of a circuit module is an icon that represents the collection. It is generated using **Virtuoso(R) Symbol Editor – XL 6.1.6**

C. Simulation using Test Bench

The simulation is designed by using schematic symbol with defined input voltage/current and sinusoidal/non sinusoidal sources based on type of output analyses. Test bench schematic entry is done using **Virtuoso(R) Schematic Editor- XL 6.1.6.** The simulation results can be analyzed using Transient and another responses based on selected design input. The design functionality is verified by sepetre SPICE simulation tool **Virtuosos(R) Analog Design Environment – XL- 6.1.6**

III. Double Tail comparator

A. Circuit design

The double tail comparator circuit diagram is shown below [3]

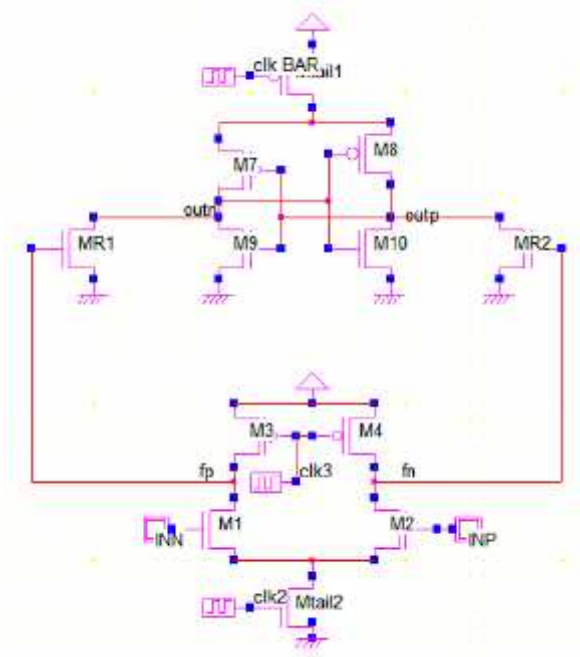

Fig 2 - Double tail comparator

The circuit designing is done using the cadence software. The circuit is built with five PMOS transistors and seven NMOS transistors including the tail transistors. Transistors are placed according to the circuit design changes and connections are made using the wires by giving respective inputs and outputs are given. The circuit consists of three inputs namely CLK,INN, INP and two output outp and outn where INN and INP are input at n and p nodes, and CLK is the input, outp and outn are outputs at n,p nodes.

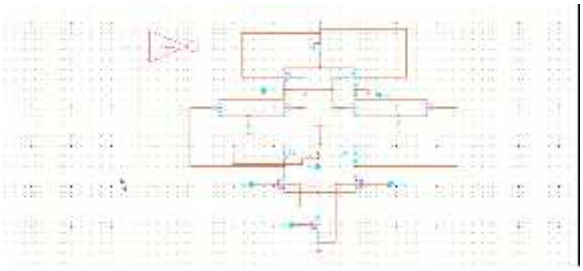

Fig 4 - Schematic of a double tail comparator

B. Symbol Creation

Symbol generation is done by converting the schematic using the design tools. This symbol is used in the test bench construction to simulate the required waveforms.

Fig 4 - Symbol of a single tail comparator

C. Test bench Design

The symbol is called for the test bench area and the required input and output pins are chosen. A 1v dc voltage is applied to the VDD and the other pin is grounded. Clock pulses are given as the inputs and the circuit is simulated for the output waveforms.

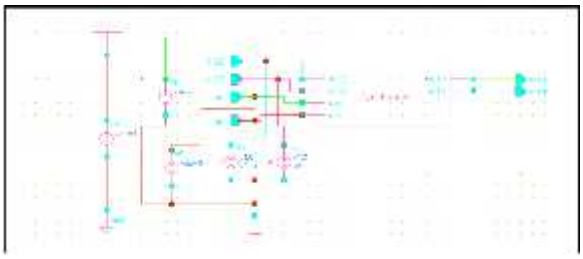

Fig 5 – Test Bench of a single tail comparator

D. Working

The operation of this comparator is explained briefly, when CLK = 0, the circuit is in reset phase. Here , the Mtail1 and Mtail2 are off , transistors M3 and M4 charge the fn and fp nodes to VDD, that causes the transistors MR1 and MR2 to discharge the output nodes to the ground. When CLK =VDD, the circuit is in Comparision phase. Mtail1 and Mtail2 gets on, M3 and M4 turn off. The voltages at nodes fn and fp start to drop with the rate defined by Mtail1 current/Cfn(p) and a ΔVfn(p) will build up. This intermediate stage formed by MR1 and MR2 passes ΔVfn(p) to the cross coupled inverters. It also provides a good shielding between input and output that results in reduction of kickback noise. Similar to the single tail comparator, the delay here consists of two parts which can be explained below such that the delay t0 represents the capacitive charging of the load capacitance at the latch stage, output nodes such as Outn and Outp until the first n-channel transistor (M9 or M10) gets on. Only after this the latch regeneration starts; thus t0 is obtained. After the latch that belongs to the first n-channel transistor turns on, the corresponding output will be discharged to the ground, which leads the front p-channel transistor (M8) to turn on, charging another output (Outp) to the VDD. The regeneration time (tlatch) is thus achieved.

E. Waveforms

The following waveforms are obtained after performing the simulation with various input values.

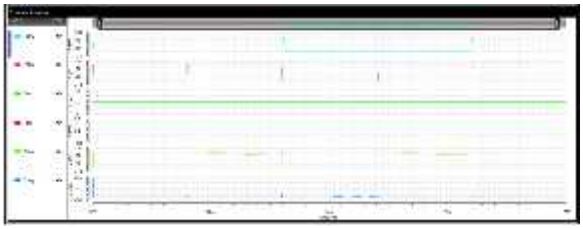

Fig 6.1 – INN>INP : Comparison phase outn<outp

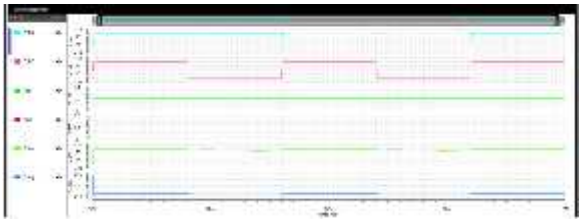

Fig 6.2 – INN=INP=1 : No Comparison

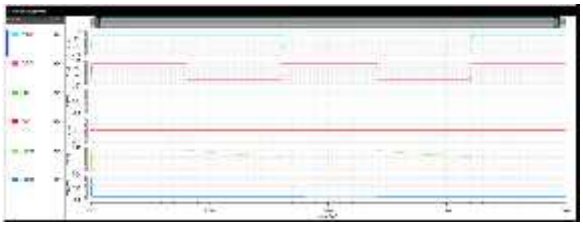

Fig 6.3 – INN=INP=0 : No Comparison

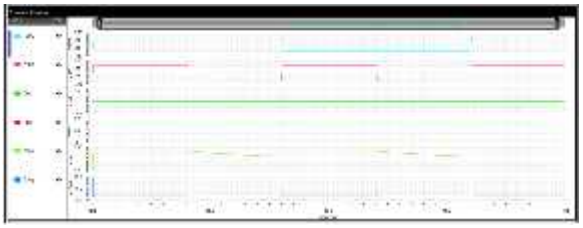

Fig 6.4 – INN<INP: Comparison phase outn>outp

IV Advantages

The topology designed has less stacking, so it can operate at lower voltages compared to the single tail transistor. The double tail enables both a large current and smaller current in the latching stage for fast operation and input stage for lower offset respectively.

V Limitations

The initial output voltage difference at the beginning of the regeneration is low. The effective transconductance of the latch is also less.

VI Conclusion

The proposed changes in the single tail comparator circuit is thus implemented on a 90nm technology using Cadence software tools. The stacking effect is thus reduced and more than one current path is introduced. The overall performance of the circuit is thus improved.

VII References

[1] Venkata Sai Rohit Bhagaatula ,Sri Harsha Gubbala, “Design of a Single tail Comparator on a 90nm technology,” IJERT Vol 4 Issue 10 Oct 2015.

[2] Rameshkumar.R, Bharathiraja.S. , “Dynamic Comparator in 180nm and 90nm using H-spice,” IJISER Vol 1 Issue 11 Dec 2014.

[3] VLSI design by V.S Bagad.