

Design of a Low-Voltage Low-Power Double-Tail Comparator

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Abstract- Comparator is one of the fundamental building blocks in most analog to digital converters. Many high speed analog to digital converters such as flash analog to digital converter require high speed and low power comparators. A new double tail comparator is designed, where the circuit of a conventional double tail comparator is modified for low power and fast operation even in small supply voltages. In this paper, a novel new double tail comparator which consumes very less power and can operate at high speeds when compared to the existing double tail comparators is proposed and simulated. Because of its high speed and low power consumption it can be used in high speed analog to digital converters, such as Flash ADCs requiring low power, high speed comparators.

Index Terms- Double-tail comparator, Clocked Regenerative Comparator, Positive feedback, Switching transistor.

I. INTRODUCTION

Dynamic latched comparators are very attractive for many applications such as high speed analog to digital converters (ADCs), memory sense amplifiers (SAs) and data receivers, due to fast speed, low power consumption, high input impedance and full swing output. They use positive feedback mechanism with one pair of back to back cross coupled inverters (latch) in order to convert a small input voltage difference to a full scale digital level in a short time [12]. A clocked comparator generally consists of two stages. In that first stage is to interface the input signals. The second (regenerative) stage consists of two cross coupled inverters, where each input is connected to the output of the other. In a CMOS based latch, the regenerative stage and its following stages consume low static power since the power ground path is switched off either by a NMOS or PMOS transistor.

High speed comparators in ultra-deep submicrometer (UDSM) CMOS technologies suffer from low supply voltages especially, when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes. The general trend in CMOS technology is to make the devices smaller and smaller to increase the density and speed of digital circuits. Reduced power supply voltage is normally not an advantage for analog design and a low supply voltage may require some special circuit techniques. The input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output-latch stage. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise [6]. The pre-amplifier based comparators suffer not only from large static power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain to source resistance due to the continuous technology scaling.

High speed comparators in ultra deep submicrometer CMOS technologies suffer from low supply voltages [2]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. Many techniques, such as supply boosting methods [3], [4] techniques employing bodydriven transistors [5], [6], current-mode design [7] and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Additional nMOS switches are used to overcome the static power consumption [1].

In this paper a new dynamic comparator is presented, which does not require boosted voltage or stacking of too many transistors. Merely by adding a few

minimum-size transistors to the conventional doubletail dynamic comparator, latch delay time is profoundly reduced. This modification also results in considerable power savings when compared to the conventional dynamic comparator and double tail comparator. The rest of this paper is organized as follows. Section II investigates the operation of the conventional clocked regenerative comparators and the pros and cons of structure is discussed.

II. RELATED WORKS

Conventional dynamic comparator: Conventional dynamic comparator is widely used in A/D converters. The comparator has high input impedance, rail-to rail output swing, and has no static power consumption. The schematic diagram of the conventional dynamic comparator is shown in fig 1. The operation of the conventional dynamic comparator is explained below During the reset phase when $CLK = 0$ and M_{tail} is off, the reset transistors M_7 and M_8 pull both the output nodes O_{utn} , O_{utp} to V_{DD} to define a start condition and to have a valid logical level during the reset.

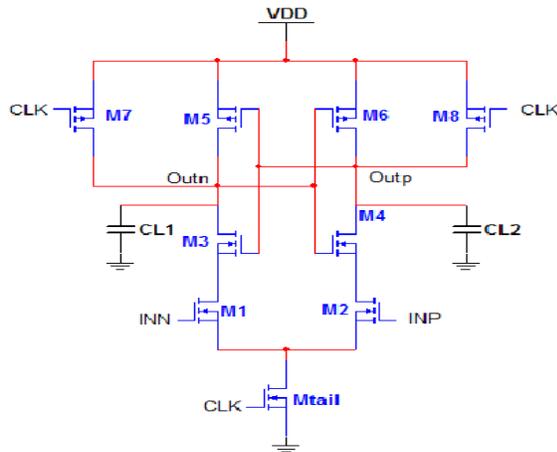


Fig. 1. Conventional dynamic comparator
In the comparison phase, when $CLK = V_{DD}$, transistors M_7 , M_8 are off and M_{tail} is on. Output nodes (O_{utp} , O_{utn}) which had been pre-charged to V_{DD} , start to discharge at different discharging rates depending on the corresponding input voltages (V_{INP} , V_{INN}). Assuming the case where $V_{INP} > V_{INN}$, the output node $Outp$ discharges faster than O_{utn} , hence with O_{utp} (discharged by transistor M_2 drain current), falling down to $V_{DD} - |V_{thp}|$ before O_{utn} (discharged by transistor M_1 drain current), the corresponding PMOS transistor (M_5) will turn on to

initiate the latch regeneration caused by back-to-back inverters (M_3 - M_5 and M_4 - M_6). Thus, the output node O_{utn} pulls to V_{DD} and O_{utp} discharges to ground. If the input voltage V_{INP} is less than V_{INN} , the circuit works vice versa.

This structure has the advantage of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. The disadvantage is the fact that due to several stacked transistors, a sufficiently high supply voltage is need for a proper delay time. Another drawback of this structure is that there is only one current path, via tail transistor M_{ta} , which defines the current for both the differential amplifier and the latch. While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better G_m / I ratio, a large tail current would be desirable to enable fast regeneration in the latch.

Conventional double tail comparator :The schematic of conventional double tail comparator is shown in the fig 2. This structure has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider M_{tail2} , for fast latching independent of the input common-mode voltage (V_{cm}), and a small current in the input stage (small M_{tail1}), for low offset.

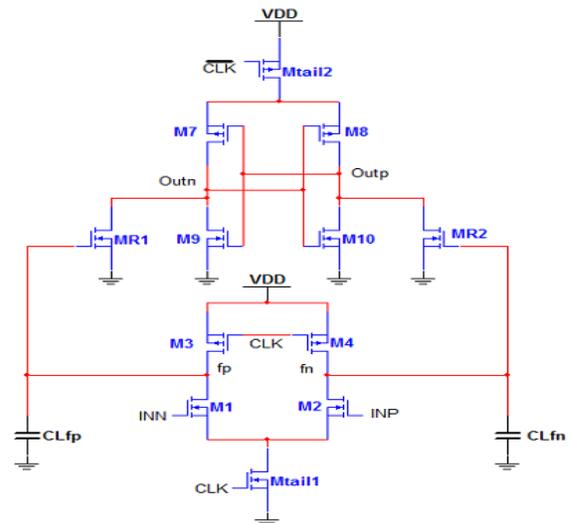


Fig. 2. Conventional double tail comparator
The operation of the conventional double tail comparator is as follows. During the reset phase ($CLK = 0$, M_{tail1} and M_{tail2} are off), transistors M_3 , M_4 pre-charge the nodes f_n and f_p to V_{DD} , which in turn

make MR1 and MR2 to discharge the output nodes Outn and Outp to the ground. During decision-making phase ($CLK = V_{DD}$, M_{tail1} and M_{tail2} turn on), the transistors M_3, M_4 turn off and the voltages at nodes f_n, f_p start to drop with the rate defined by $I \cdot M_{tail1} / C_{fn}(p)$ and an input-dependent differential voltage $\Delta V_{fn}(p)$ will also build up. The intermediate stage formed by the transistors M_{R1} and M_{R2} passes $\Delta V_{fn}(p)$ to the cross coupled inverters and provides a good shielding between to input and output to get a reduced value of kickback noise.

Modified double tail comparator: Fig.3 shows the schematic diagram of the modified double tail comparator. The modified double tail comparator is designed based on the double tail architecture.

The idea of this comparator is to increase $\Delta V_{fn}/f_p$ in order to increase the latch regeneration speed. For this purpose, M_{c1} and M_{c2} are the two control transistors that have been added to the first stage in parallel to M_3/M_4 transistors but in a crosscoupled manner [3]. The operation of the modified double tail comparator is as follows. During reset phase ($CLK = 0$, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pulls both f_n and f_p nodes to V_{DD} , hence transistor M_{c1} and M_{c2} are cut off. Intermediate stage transistors, M_{R1} and M_{R2} , reset both latch outputs to ground.

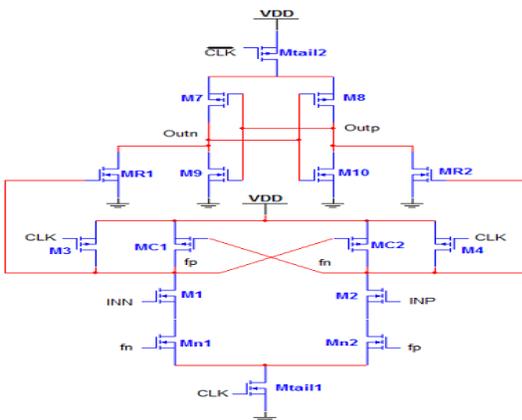


Fig. 3. Modified double tail comparator

During decision-making phase ($CLK = V_{DD}$, M_{tail1} , and M_{tail2} are on), transistors M_3 and M_4 turn off. Furthermore, at the beginning of this phase, the control transistors are still off (since f_n and f_p are about V_{DD}). Thus, f_n and f_p start to drop with different rates according to the input voltages. Suppose $V_{INP} > V_{INN}$, thus f_n drops faster than f_p , (since M_2 provides more current than M_1). As long as f_n continues

falling, the corresponding PMOS control transistor (M_{c1} in this case) starts to turn on, pulling f_p node back to the V_{DD} ; so another control transistor (M_{c2}) remains off, allowing f_n to be discharged completely. In other words, unlike conventional double-tail dynamic comparator, in which $\Delta V_{fn}/f_p$ is just a function of input transistor trans conductance and input voltage difference, in the existing double tail structure as soon as the comparator detects that for instance node f_n discharges faster, a PMOS transistor (M_{c1}) turns on, pulling the other node f_p back to the V_{DD} . Therefore by the time passing, the difference between f_n and f_p ($\Delta V_{fn}/f_p$) increases in an exponential manner, leading to the reduction of latch regeneration time.

III. PROPOSED SYSTEM STRUCTURE

Fig.4 shows the schematic diagram of the proposed double tail comparator. The proposed double tail comparator is designed based on the existing double tail architecture due to its better performance in the low voltage applications. The idea of this comparator is to reduce the total power consumption of the circuit. For this purpose, M_{n1} and M_{n2} are the two switching transistors that have been added to the second stage in series to M_1/M_2 transistors.

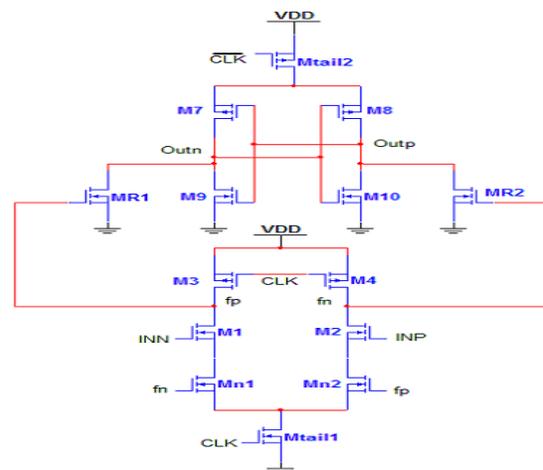


Fig. 4. Proposed double tail comparator

The operation of the proposed double tail comparator is as follows. During the reset phase ($CLK = 0$, M_{tail1} and M_{tail2} are off, avoiding static power), M_3 and M_4 pulls both f_n and f_p nodes to V_{DD} . Intermediate stage transistors, M_{R1} and M_{R2} , reset both latch outputs to ground. During decision-making phase when $CLK = V_{DD}$, M_{tail1} , and M_{tail2} are on and transistors M_3 and M_4 are turned off, since f_n and f_p are about V_{DD} .

Thus, the nodes f_n and f_p start to drop with different rates according to the input voltages.

Suppose if $V_{INP} > V_{INN}$, thus f_n drops faster than f_p , (since M_2 provides more current than M_1). As long as f_n continues falling, the corresponding PMOS transistor (M_3 in this case) starts to turn on, pulling f_p node back to the V_{DD} ; so another transistor (M_4) remains off, allowing f_n to be discharged completely. In other words, unlike the conventional double-tail dynamic comparator, in which $\Delta V_{fn/fp}$ is just a function of input transistor transconductance and input voltage difference, in the proposed double tail structure as soon as the comparator detects that for instance node f_n discharges faster, the PMOS transistor (M_3) turns on, pulling the other node f_p back to the V_{DD} . Therefore by the time passing, the difference between f_n and f_p ($\Delta V_{fn/fp}$) increases in an exponential manner, reducing the latch regeneration time.

Delay Analysis: The dynamic comparator enhances the speed of the double-tail comparator by affecting two important factors: first, it increases the initial output voltage difference (ΔV_0) at the beginning of the regeneration ($t = t_0$); and second, it enhances the effective transconductance of the latch.

1) Effect of Enhancing ΔV_0 : t_0 is a time after which latch regeneration starts. In other words, t_0 is considered to be the time it takes until the first nMOS transistor of the back to back inverters turns on, so that it will pull down one of the outputs and regeneration will commence. The latch output voltage difference at time t_0 , (ΔV_0) has a considerable impact on the latch regeneration time, such that bigger ΔV_0 results in less regeneration time.

2) Effect of Enhancing Latch Effective Transconductance: In conventional double-tail comparator, both f_n and f_p nodes will be finally discharged completely. The fact that one of the first stage output nodes (f_n/f_p) will charge up back to the V_{dd} at the beginning of the decision making phase, will turn on one of the intermediate stage transistors, thus the effective transconductance of the latch is increased. In other words, positive feedback is strengthened, which strengthen the whole latch regeneration. This speed improvement is even more obvious in lower supply voltages. This is due to the fact that for larger values of V_{th}/V_{dd} , the transconductance of the transistors decreases, thus the

existence of an inner positive feedback in the architecture of the first stage will lead to the improved performance of the comparator.

IV. SIMULATION RESULTS

To compare the performances of the proposed comparator with the previous works, each circuit was designed using $0.25\mu\text{m}$ CMOS technology, frequency at 41MHZ is simulated

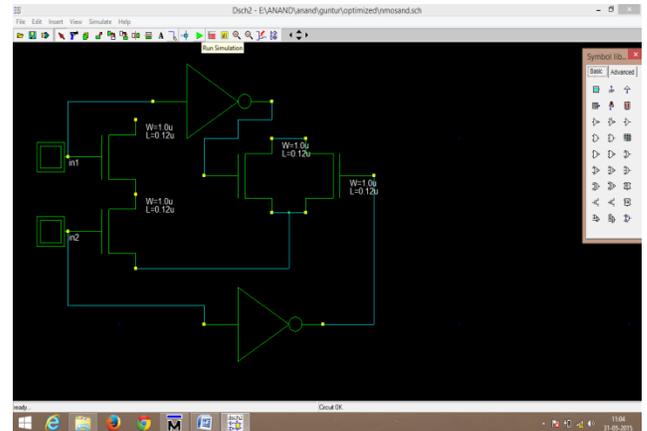


Fig.5 AND/NAND

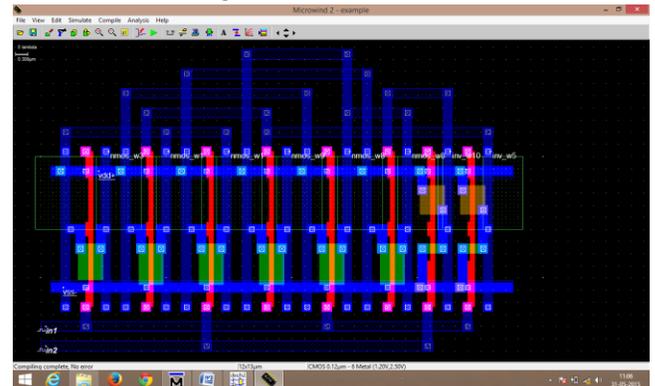


Fig.6 NAND layout

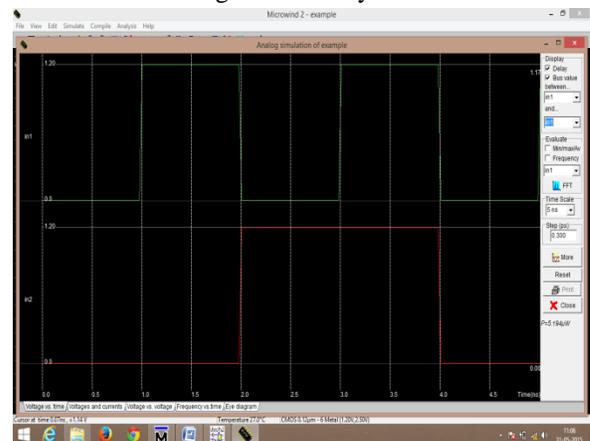


Fig.7 NAND power

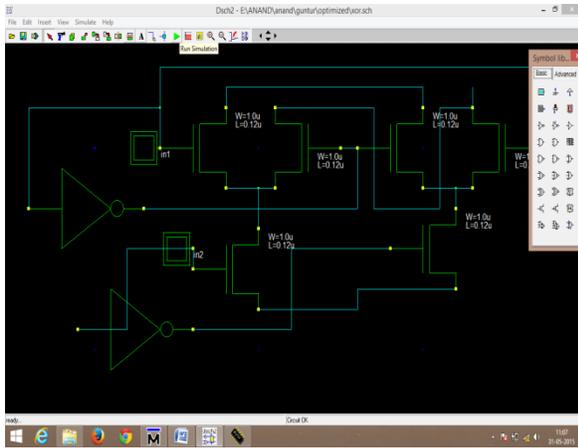


Fig.8 XOR schematic

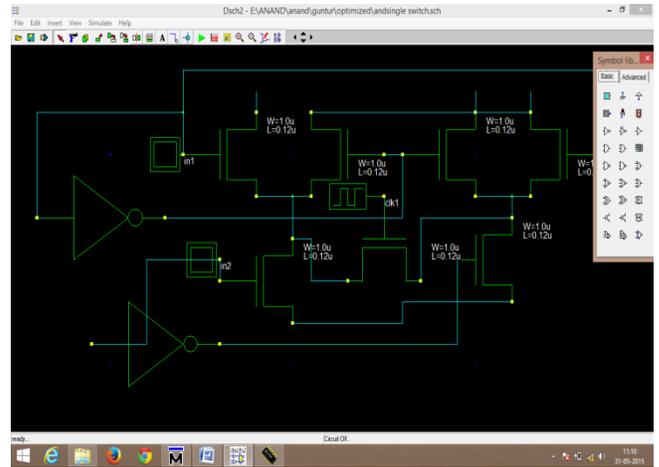


Fig.11 AND/NAND single switch

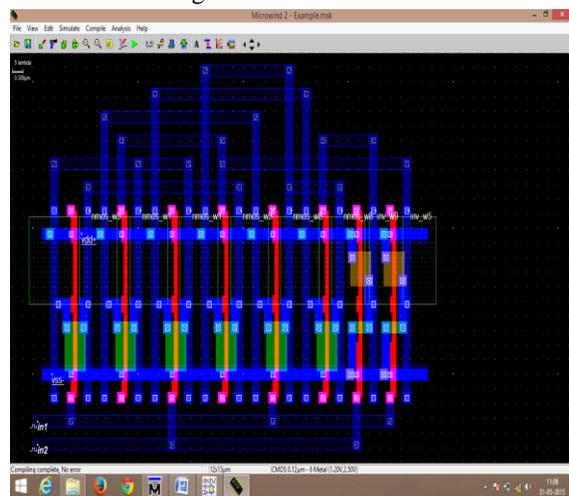


Fig.9 XOR layout

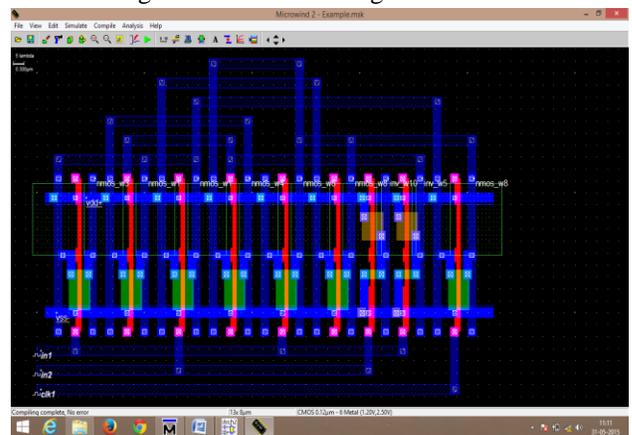


Fig.12 AND/NAND single layout



Fig.10 XOR power

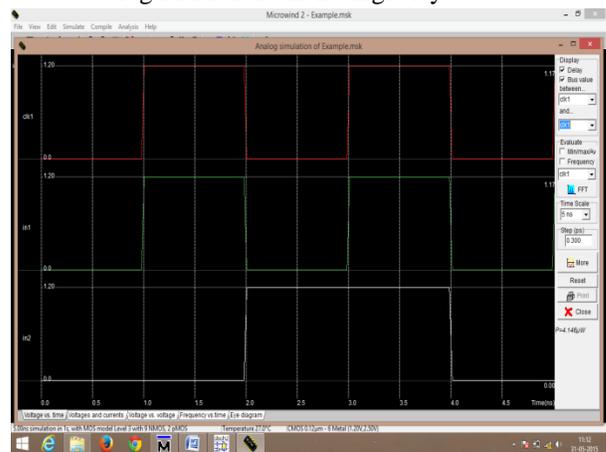


Fig.13 AND single power

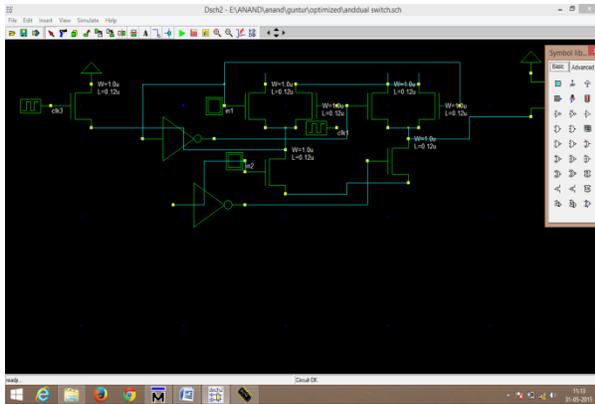


Fig.14 Dual switch

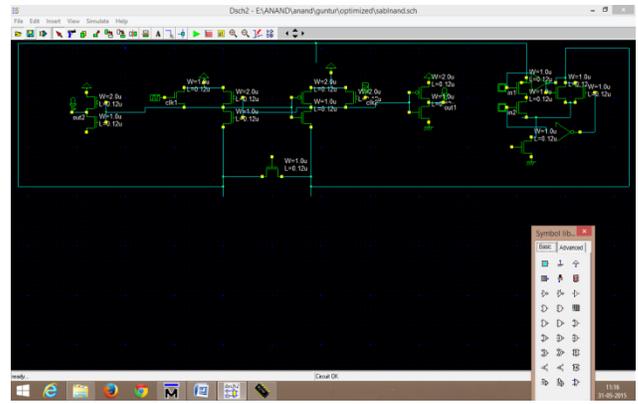


Fig.17 Sabl AND

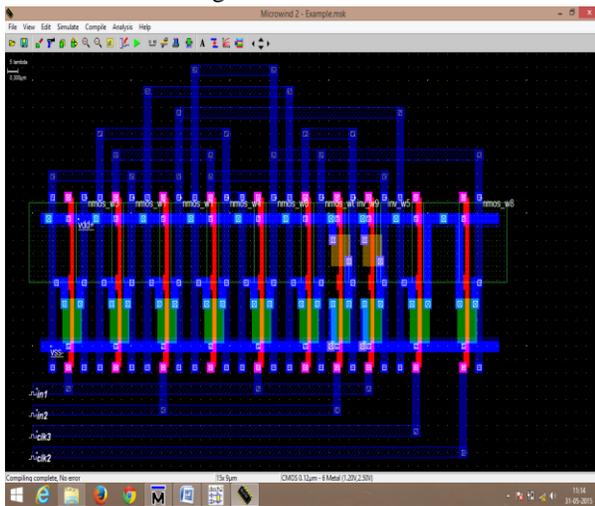


Fig.15 Dual layout

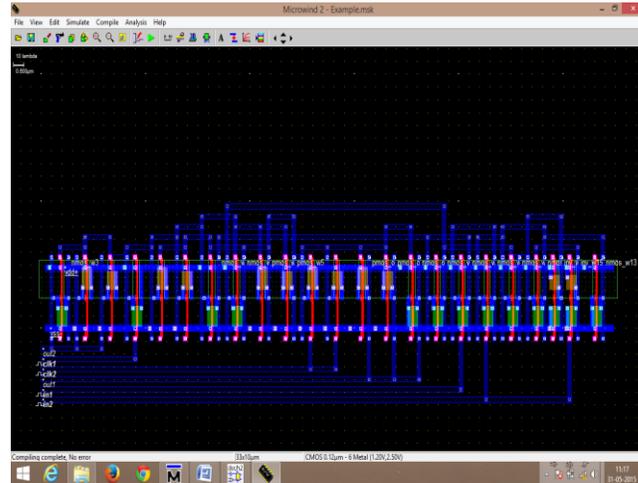


Fig.18 Sabl and layout



Fig.16 Dual power

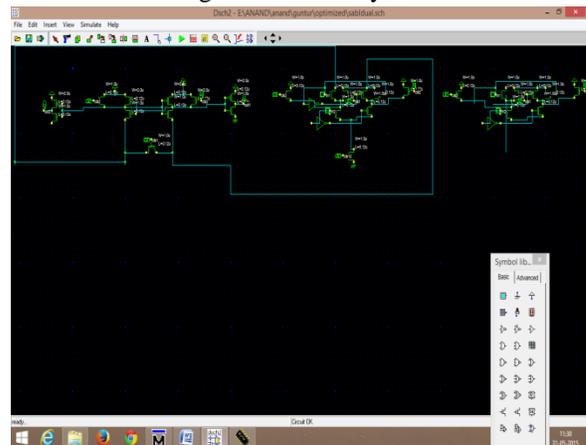


Fig.19 Sabl Dual schematic

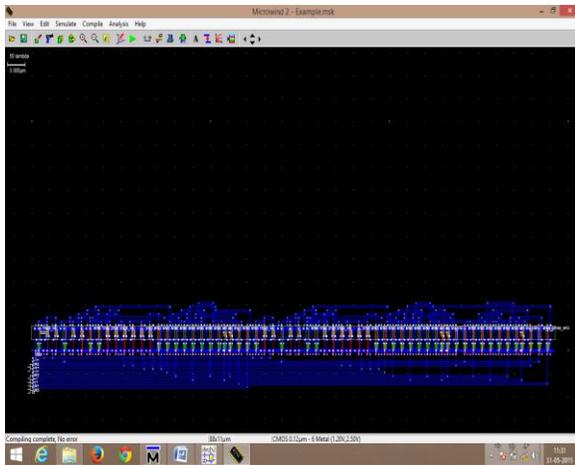


Fig.20 Sabl Dual layout

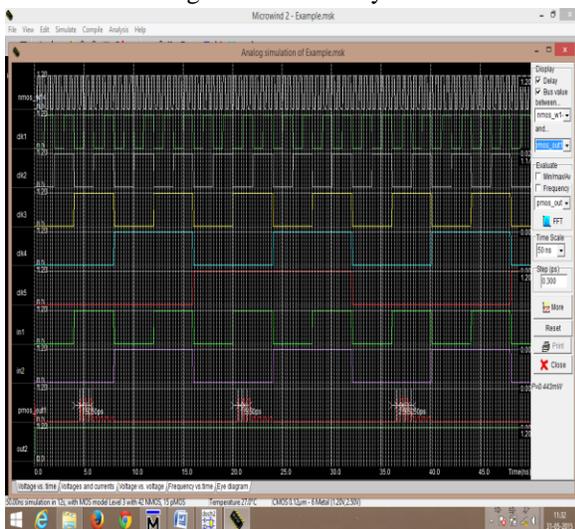


Fig.21 Sabl Dual power analysis

V. CONCLUSION

In this paper, presented a comprehensive delay analysis for clocked dynamic comparators. Two common structures of conventional dynamic comparator and conventional double-tail dynamic comparators were analyzed. Also, based on theoretical analyses, a new dynamic comparator with low-voltage low-power capability was proposed in order to improve the performance of the comparator.

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