Design and Implementation of VLSI DHT highly Modular and Parallel Architecture for Image Compression

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***Abstract*- Discrete Hartley transform is one of the most imperative algorithms of the signal processing and imageprocessing system. Now a day in each field obligatory an ever increasing demand for high speed processing and low areadesign. Many types of discrete Hartley transform algorithm are design in different adder but bit by bit is required highspeed adder.In addition, the hardwarecomplexity can be expressivelycondensed using sub expressionsharing technique of the proposed algorithm in highly parallelVLSI implementation. With efficient sharing of multipliershaving the same constant and using the advantages of theproposed algorithm, the numbers of multipliers and adders usedhas been significantly reduced and is kept at a minimumcompared with that of the existing algorithms. Efficientimplementation of multipliers with a constant is possible inVLSI. Digital image processing is the use of computer algorithmsto perform image processing on digital images.In this project, imagecompression has been taken as an application to prove thefunctionality of DHT algorithm in the field of digital signalprocessing.**

***Index Terms*- Discrete Hartley Transform (DHT),DHT domain processing, image compression, Xilinx Spartan family**

I. INTRODUCTION

Digital signal processing (DSP) includes processing of data invarious domains based on their applications.DSP has vastapplications in various fields such as space, medical,commercial, industrial and scientific. Each requiresprocessing of vast data for collecting useful information [1].Transform is a technique used in DSP for converting one formof data in another. A family of transform is available in DSPfor data processing .Fourier analysis one of the oldesttechnique used in this family. Fourier analysis is named afterJean baptiste joseph fourier (1768-1830) a Frenchmathematician and physicist. It was used for periodiccontinuous signals [2-3]. Fourier series is a technique whichdecomposes a signal in time domain into a no. of sine andcosine waves in frequency domain. But it was not applicablefor non-periodic signals Then came Fourier transform intoexistence which removes the drawback of fourier series andthus can be used for non-periodic continuous signals. Fouriertransform is a mathematical tool using integrals [3]. Butfourier transform is not suitable for non-stationary signals.Since both transforms are not applicable for discrete signals,so there is a need for new transform for discrete signals [4].

Discrete time fourier transform (DTFT) is used for signalsthat extend from positive to negative infinity but are notperiodic. DTFT is not used for periodic discrete signals sodiscrete fourier transform (DFT) can into existence. DFT is adiscrete numerical equivalent of FT using summation insteadof integrals.DFT is used for signals that repeat themselves inperiodic fashion extending from positive to negative infinity.FFT is a improvement of DFT in which computation has becomes faster.

Compression is useful as it helps in reduction ofthe transmission bandwidth required or the usage ofexpensive resources, such as memory (hard disks).The term data compression refers to the process ofreducing the required data to represent a quantity ofinformation. Because various amounts of data canbe used to represent the same amount ofinformation, representations that contain irrelevantor repeated information are said to containredundant data. Digital image compression is themost important part in applications like multimediawhich aims to minimize the number of bits in animage data for its efficient storage (less storagearea).Two-dimensional intensity arrays suffer fromthree principle data redundancies that can beidentified and exploited:

Spatial and temporal redundancy

Irrelevant information

Coding redundancy.

In this brief, a new VLSI DHT algorithm that iswell suited for a VLSI implementation on a highlyparallel and modular architecture is proposed. It canbe used for designing a completely novel VLSIarchitecture for DHT.

II. RELATED WORKS

H. M. De Oliveira et al. [1], discrete transforms which include theDiscrete Fourier Transform (DFT) or the Discrete HartleyTransform (DHT) supply a critical tool in SignalProcessing. The software of reworktechniques is based on the lifestyles of the so-called speedytransforms. In this paper, a few rapid algorithms are derivedwhich meet the lower bound at the multiplicative complexity of a DFT/DHT. The method is based totally on thefactorization of DHT matrices. New algorithms for shortblock lengths such as N = three, five, 6, 12 and 24 are offered.Inthis paper we have seen DHT algorithms for N= 12 which might beused 52adders and 4 multipliers.

Said Boussakta et al. [2], the discrete Hartley remodel(DHT) has proved to be a precious tool in virtual signal/image processing and communications and has additionally attractedresearch interests in lots of multidimensional packages.Although many speedy algorithms were developed for thecalculation of one- and -dimensional (1-D and a 2-D) DHT,

the improvement of multidimensional algorithms in three andextra dimensions remains unexplored and has no longer been givencomparable attention; hence, the multidimensional Hartleyremodel is generally calculated via the row-columnmethod. However, right multidimensional algorithms canbe greater efficiency than the row-column method and need to beevolved. Therefore, it's far the aim of this paper to introducethe idea and derivation of the three-dimensional (3-D)radix-2 algorithms for fast calculation of the 3-D discrete Hartley transform. The proposed set of rules is primarily based on theideas of the divide-and-overcome technique implemented directlyin 3-D. It has an easy butterfly structure and has been determinedto provide substantial savings in arithmetic operations in comparisonwith the row-column method based on comparable algorithms. Inthis paper we have seen DHT algorithm for N=8 which can beused 39 adders and 24 multipliers.

GautamAbhay Chand Shah et al. [3], the radix-4 decimation in-time fast Hartley remodel an set of rules for DHT turned intobrought by Bracewell. A set of rapid algorithms have been in additionevolved by Sorenson et al. In this paper, a quick radix-4 decimation-in-time set of rules that calls for less number ofmultiplications and additions is proposed. It utilizes fourdistinctive systems inside the sign flow diagram. It exhibits arecursive pattern and is modular. The operational counts forthe proposed set of rules are decided and confirmed viaenforcing the program in C. An analog structure toenforce the set of rules is proposed. The validity of the identicalis examined by way of simulating it with the help of the OrcadPSpice.Inthis paper we have seen DHT algorithm for N=4 that are used8 adder and zero multipliers.Doru Florin Chipper et al. [4], we gift a new greentechnique for the computation of the discrete Hartley reworkof type II and radix-2 length. This recursive method requires adecreased variety of mathematics operations in comparison withcurrent methods and may be without difficulty applied. A newtechnique for the direct computation of a period Ntype-II DHT from adjoining DHT-II sequences of periodN/2 is likewise supplied. In this paper, we've got visible DHTalgorithm for N=eight which might be used 28 adders and 10 multiplier.

M. N. Murty et al. [5], Discrete Hartley rework is ancritical device in virtual sign processing. This paper givesa singular recursive set of rules for attention of one-dimensionaldiscrete Hartley rework of even duration. The transform isconstructed by way of single folding of access data and the usage ofChebyshev Polynomial. The single folding set of rules offersdatathroughput times of that achieved via theconventional techniques. Compared to a few different algorithms,the proposed algorithm achieves savings at the range ofadditions and multiplications. The recursive algorithms aresuitable for VLSI implementation.In this paper, we havevisible DHT algorithm for N=4 which are used 7 adders and 6 multiplier.

Doru Florin Chipper et al. [6], A new very massive scaleintegration (VLSI) set of rules for a 2N-duration discrete Hartleytransform (DHT) that may be effectively applied on anoticeably modular and parallel VLSI structure having athe everyday shape is presented. The DHT set of rules may becorrectly cut

up into numerous parallel parts that can be performedconcurrently. Moreover, the proposed algorithm is well suitedfor the subexpression sharing technique that may be used tosignificantly reduce the hardware complexity of the enormouslyparallel VLSI implementation. Using the blessings of theproposed set of rules and the fact that we are able to successfully percentagethe multipliers with the equal constant, the number of themultipliers has been appreciably decreased such that therange of multipliers could be very small evaluating with that of theexisting algorithms. Moreover, the multipliers with a steadymay be efficiently applied in VLSI. In this paper we'vevisible DHT algorithm for N=8 which might be used 16 adders and a pair ofmultiplier.

III. SUGGESTEDSYSTEM

Table I lists the required number ofmultiplications and additions for the proposedalgorithm, the Sorensen one and Bi algorithm,where rotations are implemented with fourmultiplications and two additions (Radix-2[13]∗)and with three multiplications and three additions(Radix-2[13]∗∗).

Table I computational complexity

	Radix 2[13]		Radix 2[13]*		Radix 2[11]**		Proposed	
N	M	A	M	A	M	A	M	A
8	-	-	-	-	4	26	2	24
16	10	62	10	62	20	74	-	-
32	40	168	38	174	69	194	32	31
64	118	418	98	438	196	482	-	-
128	320	1008	258	1070	516	1154	-	-
256	806	2354	642	2518	1284	2690	-	-

The values of M in the proposed algorithm arecomputed considering both the multipliers with thesame constant and common subexpression sharing.The number of multipliers in Sorensen algorithm[11] is significantly greater than that in theproposed one. However, the split-radix algorithmhas an irregular structure and is difficult to beimplemented in hardware as opposed to thealgorithm been proposed that has a regular andmodular structure and can be very easilyimplemented in parallel for a DHT of length N = 32.By reducing the number of number of multipliersand adders as shown in Table I mean that the costas well as the hardware complexity will be reducedsignificantly.

The multiplier "MUL" blocks are used toimplement the shared multipliers with a constant.This block contains two multipliers with a constant.Each multiplier is shared by four input sequencesand are multiplied with the same constant. Theprocess is done in an interleaved manner usingmultiplexers and demultiplexers controlled by twoclocks. One of the advantages of this algorithm andarchitecture is the fact that the multiplications withthe same constant are shared in the MUL blocks.Thus, the number of multipliers is significantly lessthan that of the existing algorithms given in Table.Iwhich has become now only 32.

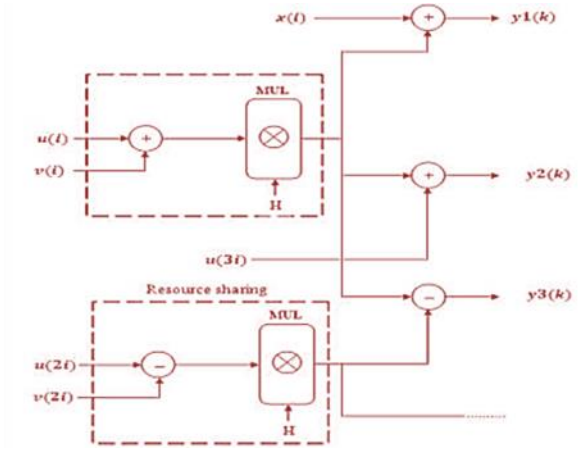

Fig. 1 VLSI architecture for DHT of length N = 32

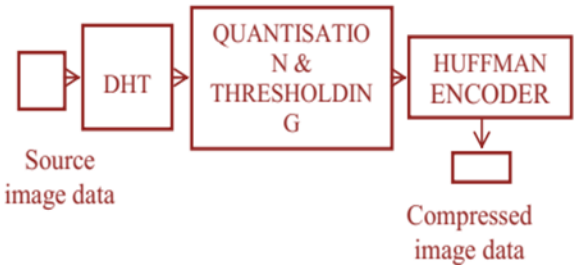

Fig. 2 Block diagram of the proposed system

Since the image data is easier to compress whenpixel values are converted into another domain,hence the need for transformation. The imagespixel values is operated by the transform andconverts them to a set of less correlated transformedcoefficients. Natural images (which are the mostcommon images to be compressed) usually have alot of spatial correlation between the pixelintensities in its neighbourhood.

The spatial andtemporal redundancy is reduced by using thetransform where it exploits the correlations justmentioned. This operation is generally reversibleand may or may not reduce the data content of theimages. Here discrete Hartley transform (DHT) hasbeen used for generating the coefficients.Quantization is the process of approximating acontinuous range of values (or a very large set ofpossible discrete values) by a relatively small("finite") set of discrete symbols or values. In otherwords it means limited number of output values aremapped by a broad range of input values. Theaccuracy of the transformed coefficients will bereduced in accordance with a pre-establishedfidelity criterion. The goal is to reduce theirrelevant amount of information present in theimage. The process is irreversible since theinformation is lost in this process. So this step mustbe avoided to keep the whole information intact inerror-free techniques.

Quantization matrix for DCT can be easilyobtained but the scanning order is special for DHTand hence is difficult for DHT. Since thequantization matrix is difficult to design, energyquantization method can be applied. In this method,the energy content of the transformed coefficientsof each matrix is obtained by using the followingformula. The normalized energy is given by:

$$E_n = \sum_{m=0}^{M} \sum_{n=0}^{N} x(m,n)^2$$

Where M and N are the widths of the sampleblock and x (m, n) is the transformed sample.Next a threshold value is selected andtransformed values will be neglected or kept intactaccording to this threshold value. Since thethreshold value is determined as a percentage of theenergy content of the matrix i.e. the intensity ofpixel values, hence the threshold value is not aglobal value and hence varies for each matrix. Thepercentage value is only pre-decided. Thetransformed co-efficient is truncated if thetransformed co-efficient is less than the thresholdvalue otherwise it is kept intact. By using themethod just stated, helps in sustaining the requiredinformation in different regions of the images andalso helps in treating the image in segments.An entropy encoding is a lossless datacompression scheme that is independent of thespecific characteristics of the medium. The mainobjective of entropy coding is to encode the main types ofentropy coding, a unique prefix code will begenerated and assigned to each unique symbol thatoccurs in the input.

Huffman coding is one of the most populartechniques for removing coding redundancy. Theterm refers to encoding a source symbol (such as acharacter in a file) with the use of a variable-lengthcode table. Based on the estimated probability ofoccurrence for each possible value of the sourcesymbol, the variable-length code table has beenderived in a particular way. A Huffman coder formsa data tree from the original data symbols and theirassociated probabilities and determines thecompressed symbols.

IV. CONCLUSION

In this momentary, a new highly parallel VLSIalgorithm for the computation of a length-N = 2nDHT having a modular and regular structure hasbeen offered. Furthermore, this algorithm can beimplemented on a highly parallel architecturehaving a modular and regular structure with a lowhardware complexity by extensively using asubexpression sharing technique and the sharing ofmultipliers having the same constant. So from theacquired results, it can be concluded that eventhough after optimizing the DHT, it can be used forapplications in signal processing domain.

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