

Design and Implementation of High Speed Digital Vedic Multiplier Using Cadence

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Abstract- In this design our objective is to emphasize the importance of Vedic Mathematics for digital applications. Ancient Vedic mathematics not only facilitate the complex mathematical Operations but also useful for logical applications. In the present work we are using the concept of Urdhva-tiryakbyham, i.e., vertical and crosswise Multiplication and its implementation for 16-bit multiplication. This technique optimizes the output in term of steps of calculation and therefore reduces the delay, area, power of a digital circuit. We develop this design with the help of front end language Verilog.

I. INTRODUCTION

Vedic Mathematics (VM) is Ancient Indian Mathematics which in Indian mythology is part of four books of wisdom known as Vedas. It is basically an element of Sthapatya-Veda (book on civil engineering and architecture), which is a supplement (upaveda) of Atharva Veda.

It acquires a description of the contemporary mathematics such as arithmetic, geometry, trigonometry, integral and differential calculus.

His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaj (1884-1960) compiled this form of mathematics together and illustrated various mathematical explanations and it's applications.

He constructed 16 sutras (formulae) and 16 Upasutras (sub formulae) after extensive research of Atharva Veda. Vedic mathematics is not only a mathematical wonder but also logical. Due these phenomenal characteristics, VM has already crossed the boundaries of India and has become a leading topic of research abroad. VM deals with several basic as well as complex mathematical operations, especially, methods of basic arithmetic are extremely simple and powerful. Arithmetic is the oldest and most elementary branch of Mathematics. The name

Arithmetic comes from the Greek word (arithmos). Arithmetic is used by almost everyone, for tasks ranging from simple day to day work like counting to advanced science and business calculations. As a result, the need for a faster and efficient Arithmetic Unit in computers has been a topic of interest over decades. The work presented in this thesis, makes use of Vedic Mathematics and goes step by step, by first designing a Vedic Multiplier, then a Multiply Accumulate Unit and then finally an Arithmetic module which uses this multiplier and MAC unit. The four basic operations in elementary arithmetic are addition, subtraction, multiplication and division. Multiplication basically is the mathematical operation of scaling one number by another. Talking about today's engineering world, multiplication based operations are some of the frequently used Functions, currently implemented in many Digital Signal Processing (DSP) applications such as Convolution, Fast Fourier Transform, filtering and in Arithmetic Logic Unit (ALU) of Microprocessors.

The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutra). These Sutra have been traditionally used for the multiplication of two numbers in the decimal number system. we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. .

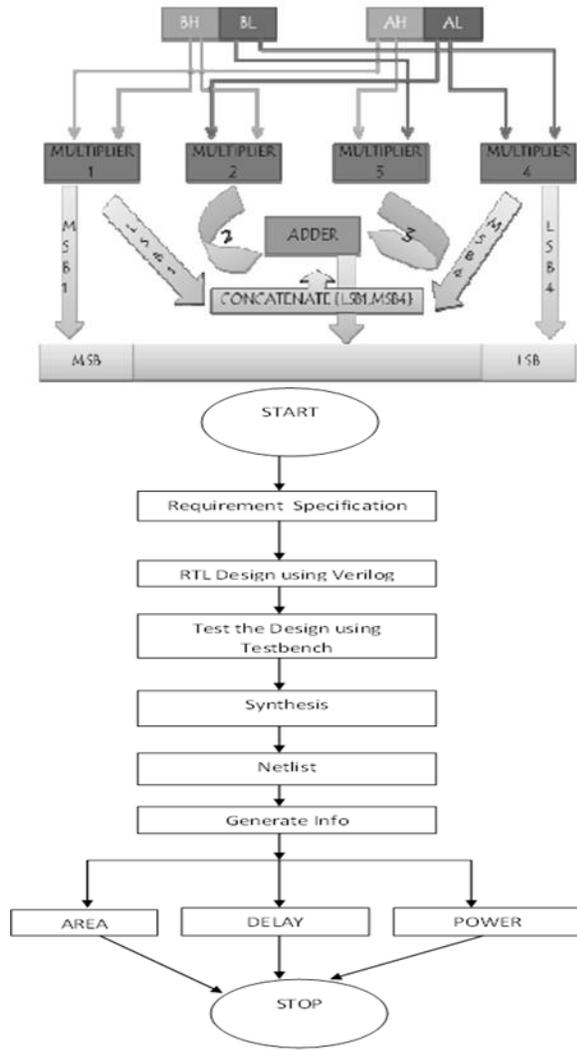
PROPOSED DESIGN ALGORITHM :

Designing a higher bit multiplier some modifications in the conventional Vedic Multiplication is enviable.

We have made a significant modification by dividing the bigger bits into smaller till one reaches a state of affairs of 2-bit multiplication which can be very easily solved by the conventional Vedic Multiplication and then applying the results back to the hierarchy of division into smaller bits.

In general, the proposed algorithm work as follows:

1. Let the multiplier be A and the multiplicand be B.
2. Now, divide the 2 into AH, AL and BH, BL respectively and keep doing this till the 2-bit multiplication state of affairs is not reached.
3. In the process we obtain 4 results, 2 from vertical and 2 from cross products.
4. The LSBs of the result from vertical product of LSBs are the actual LSBs of the product to be obtained. Similarly, the MSBs of the result from vertical product of MSBs are the actual MSBs of the product to be obtained.
5. The sum of the cross products resultant and the concatenated number obtained from the MSBs of LSB vertical products and the LSBs of MSB vertical products gives the rest of the final results' bits. The block diagram is as follows



Design Methodology



EXISTING 2 BIT MULTIPLIER—AREA

Report Area

Generated by: Encounter(R) RTL Compiler RC11.10 - v11.10-p005_1 (Nov 10 2011)
 Generated on: May 01 2017 05:27:39
 Module: mul_2bit
 Technology library: osu025_stdcells
 Operating conditions: typical (balanced_tree)
 Wireload mode: enclosed

Instance	Cells	Cell Area	Net Area	Total Area	Wireload	Wl. Flag
mul_2bit	14	1205.55	0.00	1205.55	-none-	{0}
mul_2bit/mul_4_18	14	1205.55	0.00	1205.55	-none-	{0}

Close Help

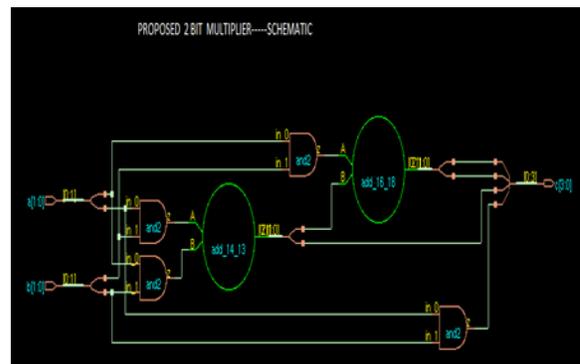
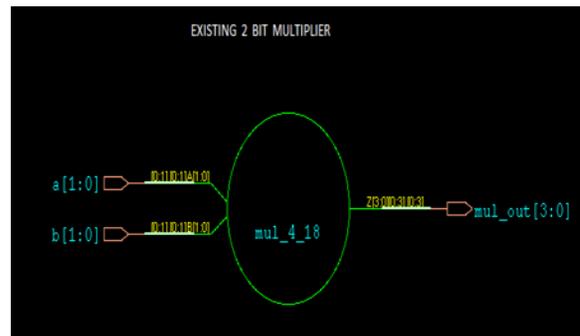
EXISTING 2 BIT MULTIPLIER—POWER

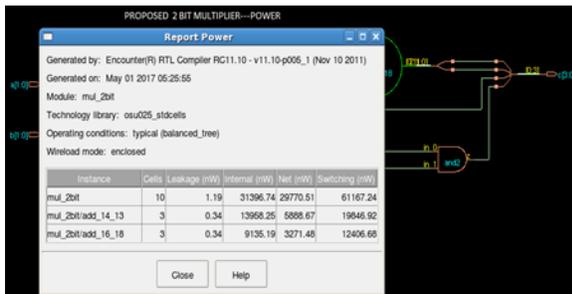
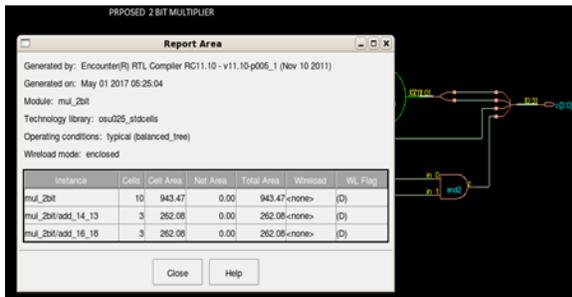
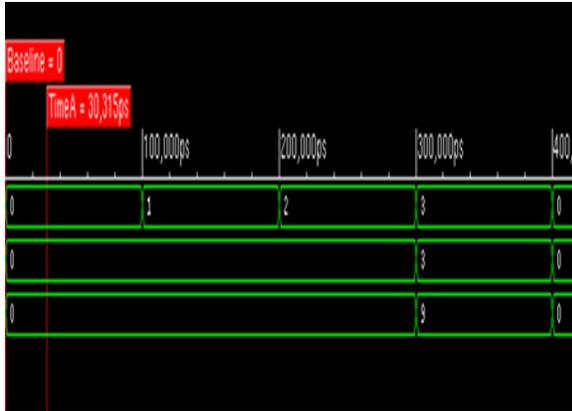
Report Power

Generated by: Encounter(R) RTL Compiler RC11.10 - v11.10-p005_1 (Nov 10 2011)
 Generated on: May 01 2017 05:29:44
 Module: mul_2bit
 Technology library: osu025_stdcells
 Operating conditions: typical (balanced_tree)
 Wireload mode: enclosed

Instance	Cells	Leakage (mW)	Internal (mW)	Net (mW)	Switching (mW)
mul_2bit	14	1.01	26484.61	38930.66	65415.28
mul_2bit/mul_4_18	14	1.01	26484.61	28461.91	54946.53

Close Help





CONCLUSION

The design of 16 bit Vedic multiplier, 16 bit multiplier built by 8 bit multiplier. Multiplier module has been realized using 2 bit multiplier. The computation delays for the proposed multiplier and traditional multiplier are compared which clearly shows improvement in performance. Cadence implementation proves the hardware realization of Vedic Mathematics Algorithms. Urdhva Tiryakbhayam Sutra is highly efficient algorithm for multiplication.

FUTURE WORK

Even though Urdhva Tiryakbhayam Sutra is fast and efficient but one fact is worth noticing, that is 2x2 multiplier being the basic building block of 4x4 multiplier and so on. This leads to generation of a large number of partial products and of course, large fan-out for input signals a and b. To tackle this

problem, a 4x4 multiplier can be formed using other fast multiplication algorithms possible, and keeping Urdhva Tiryakbhayam for higher order multiplier blocks. Also multiplication methods like Toom Cook algorithm can be studied for generation of fewer partial products.

In this work, some steps have been taken towards implementation of fast and efficient ALU or a Math Co processor, using Vedic Mathematics and maybe in near future, the idea of a very fast and efficient ALU using Vedic Mathematics algorithms is made real.

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