Simulation of PV based multi-level DC-DC converter with symmetrical duty cycle control DC motor applications

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***Abstract*- The recent growth of battery powered applications and low voltage storage elements are increasing the demand of efficient step-up dc–dc converters. Typical applications are embedded systems, renewable energy systems, fuel cells, mobility applications and uninterrupted power supply (UPS). These applications demand high step-up static gain, high efficiency and reduced weight, volume and cost. Some classical converters with magnetic coupling as fly-back or current-fed push-pull converter can easily achieve high step-up voltage gain. However, the power transformer volume is a problem for the development of a compact converter. The energy of the transformer leakage inductance can produce high voltage stress, increases the switching losses and the electromagnetic interference (EMI) problems, reducing the converter efficiency. Half-bridge three-level (TL) converter is a potential topology in high input voltage applications. It is essentially derived from the neutral point clamped (NPC) inverter, which can reduce the voltage stress of the power switches to only a half of the input voltage, when compared with traditional topologies. The common features of TPTL (three-phase three level) dc/dc are the employment of an NPC inverter configuration and a three-phase transformer; although the voltage stress on switches can be reduced, the numerous power switches result in the higher overall cost and increased control circuit complexity. To simplify the circuit configuration, a novel TPTL converter is proposed in this project, which keeps the advantages of the available TPTL converters including the lower voltage stress, efficient utilization for transformer, and reduced output filter requirement. The proposed concept is verified by using Matlab/Simulink software and the corresponding results are presented.**

Index Terms- Three phase three levels (TPTL), Three Phase, DC/DC Converter.

I. INTRODUCTION

The three-phase single-switch boost rectifier is an interesting option for this PFC stage, since it can comply with the aforementioned standard with simplicity, efficiency, reliability and low cost. However, in order to reduce the harmonic distortion in the three-phase boost rectifier, its output voltage has to be significantly increased with respect to the input voltage [1]. Therefore, this increment in the output voltage also increases the voltage stress across the devices in the DC/DC step-down second stage converter. At this power level (6 kW), the DC/DC second stage converter is usually implemented with a full-bridge topology. In this case, each switch in the full-bridge topology is subjected to the full bus voltage. In this voltage range, MOSFET devices with a high rdson may be used. This approach increases the conduction losses of the DC/DC converter. Another option at this power range is to use IGBT devices. However, in this case the switching frequency must be reduced and consequently the power density of the converter.

This paper presents a novel Zero Voltage Switching Three-Level DC/DC converter, whose main characteristics are to reduce the voltage stress across the main switches, provide ZVS operation for all switches, and simplify the control by using the well-known phase-shift control. This paper will first address the operation and analysis of the proposed converter. Half-bridge three-level (TL) converter is a potential topology in high input voltage applications [14]–[17]. It is essentially derived from the neutral point clamped (NPC) inverter [18], which can reduce the voltage stress of the power switches to only a half of the input voltage, when compared with traditional topologies. It can also achieve ZVS easily via using the leakage inductance of the transformer and the intrinsic capacitors of the switches without additional components. To incorporate the advantages of half-bridge TL converter and three-phase full-bridge converter, three-phase three-level (TPTL) PWM dc/dc converters were proposed in [19]–[21]. The proposed converters are composed of an NPC inverter connected to the primary side of a three-phase high-frequency transformer. The secondary side of the transformer feeds a three-phase rectifier, and the output stage of the converter is composed of the output filter and the load. The symmetrical duty cycle control was adopted in the converter proposed in [19], and the converter has the features including lower voltage stress on switches, soft-switching capabilities, and voltage source characteristic for output stage.

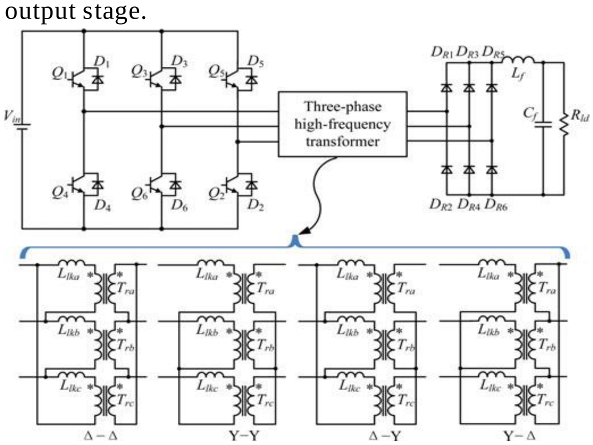


Fig.1.Circuit configuration of a three-phase full-bridge dc/dc converter.

A phase-shifted PWM control strategy was introduced into the converter proposed in [20] and [21]; as a result, the switches can achieve ZVS and Zero-current-switching without additional auxiliary components. The common features of TPTL dc/dc converters mentioned previously are the employment of an NPC inverter configuration and a three-phase transformer; although the voltage stress on switches can be reduced, the numerous power switches result in the higher overall cost and increased control circuit complexity. To simplify the circuit configuration, a novel TPTL converter is proposed in this paper, which keeps the advantages of the available TPTL converters including the lower voltage stress, efficient utilization for transformer, and reduced output filter requirement; meanwhile, the number of switches is reduced significantly, along with the gate drivers and PWM channels, resulting in a simpler architecture and lower cost. In this paper, the derivation of the proposed converter is illustrated; the operation principle and the theoretical analysis are presented. Toobtain behavioral and performance characteristics of the converter, the experimental verification from a prototype about 1 kW is carried out.

A Photovoltaic (PV) system directly converts solar energy into electrical energy. The basic device of a PV system is the PV cell. Cells may be grouped to form arrays. The voltage and current available at the terminals of a PV device may directly feed small loads such as lighting systems and DC motors or connect to a grid by using proper energy conversion devices.

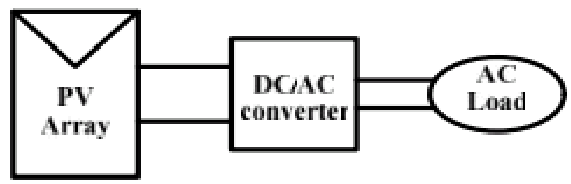


Fig.2. Block diagram representation of Photovoltaic system

This photovoltaic system consists of three main parts which are PV module, balance of system and load. The major balance of system components in this systems are charger, battery and inverter. The Block diagram of the PV system is shown in Fig.2. A. Photovoltaic cell A photovoltaic cell is basically a semiconductor diode whose p–n junction is exposed to light. Photovoltaic cells are made of several types of semiconductors using different manufacturing processes. The incidence of light on the cell generates charge carriers that originate an electric current if the cell is short circuited1

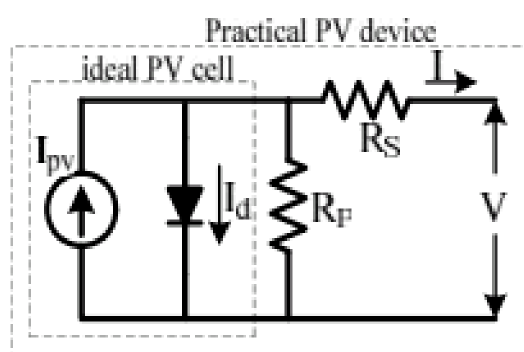


Fig.3. Practical PV device

The equivalent circuit of PV cell is shown in the fig.3. In the above figure the PV cell is represented by a current source in parallel with diode. Rs and Rp represent series and parallel resistance respectively. The output current and voltage form PV cell are represented by I and V.

II. DERIVATION OF THE PROPOSED TPTL CONVERTER

Fig. 2 shows the circuit configuration of half-bridge TL converter and conventional full-bridge converter, respectively. For simplicity, only the primary stages are presented. As well known, the two converters can both adopt phase-shifted control, and the switches are classified into the leading switches and the lagging switches. The waveforms of *vAB* and the primary current in two converters are basically the same; therefore, in this sense, the half-bridge TL converter is essentially equivalent to the full-bridge converter. Fig. 3 shows the topology of three-phase full-bridge converter and the corresponding control strategy, in which a three-phase transformer with Δ-Y connection is employed for the smaller

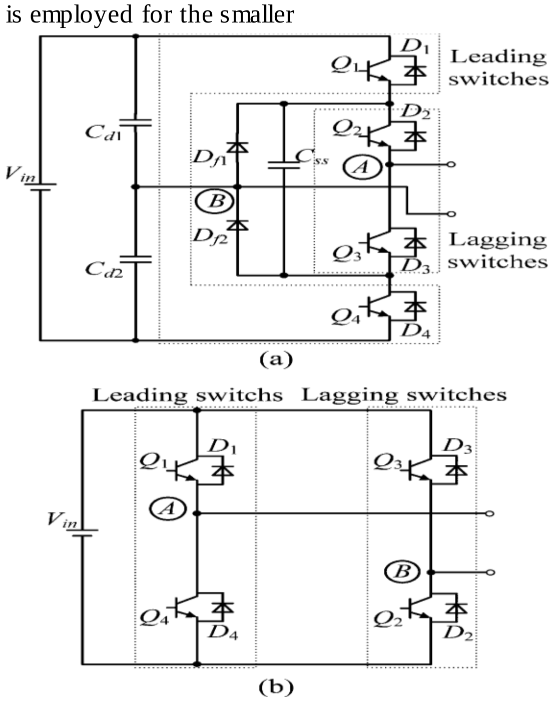


Fig. 4. Comparison of the primary configuration between half-bridge T-converter and full-bridge converter.

(a) Half-bridge TL converter. (b) Full-bridge converter.

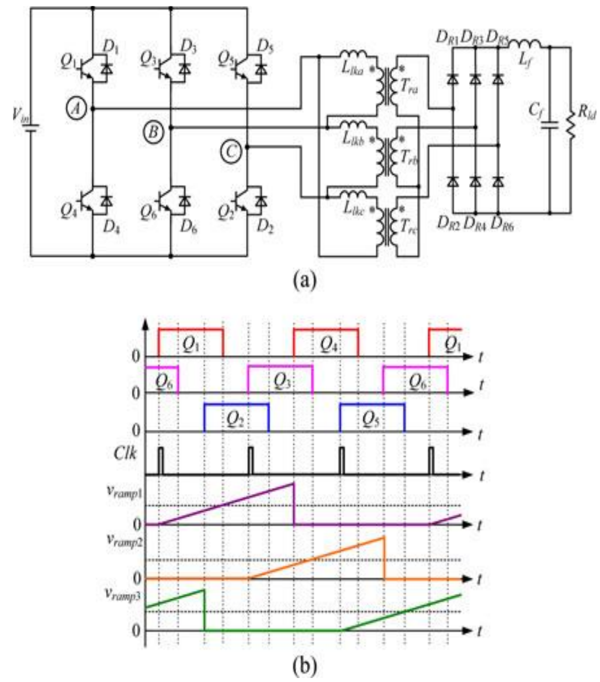


Fig. 6.Topology and control strategy of three-phase full-bridge converter. (a) Main circuit. (b) Control strategy.

turns ratios and transformer VA rating [22]. *Q*1,*Q*3 , and *Q*5 are switched ON in turn according to the rising edge of the clock signals with interval of one-third switching period; the duty cycles of *Q*1,*Q*3 , and *Q*5 are modulated by the comparison between three same carrier signals and the error signal. The gate signals of *Q*4,*Q*6 , and *Q*2 are interleaved with *Q*1,*Q*3 , and *Q*5 by a half switching period, respectively. For the duty cycles

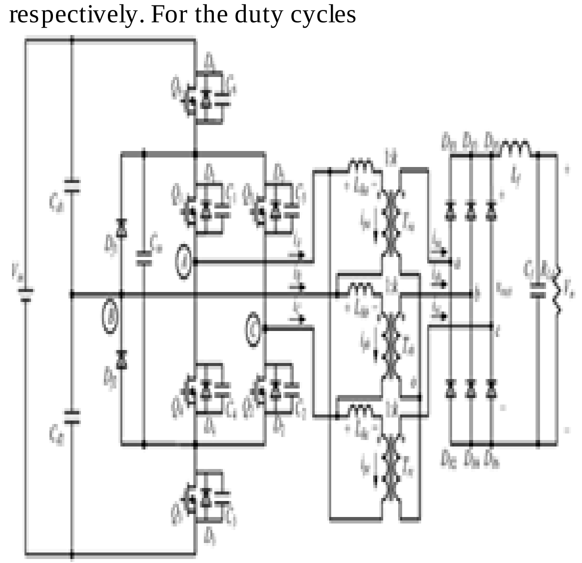


Fig. 7 Proposed TPTL dc/dc converter.

of all the switches are equal, the control strategy in Fig. 3(b) is named as symmetrical duty cycle control. As shown, the three-phase full-bridge converter can be viewed as a combination of two full-bridge sections sharing a common bridge leg. In the full-bridge section composed of Q1,Q3,Q4 , and Q6,Q6 is turned ON leading to Q1 , and Q3 is turned ON leading to Q4 , as depicted in Fig. 3(b). According to the correspondence between two converters shown in Fig. 2, the full-bridge section composed of Q1,Q3,Q4 , and Q6 can be replaced by a half bridge TL section directly, and the transformer and secondary stages remain unchanged. Therefore, a novel TPTL converter can be derived, as shown in Fig. 4. The proposed converter shares the same control strategy shown in Fig. 3(b). As shown in Fig. 4, Cd1 and Cd2 are large enough and they share evenly the input voltage, i.e., VCd1 = VCd2 = Vin /2. Llka, Llkb , and Llkc are the equivalent primary leakage inductances of each phase. Df 1 and Df 2 are freewheeling diodes. Css is the flying capacitor, which is in favor of decoupling the switching transition of Q1,Q3,Q4 , and Q6 .DR1−DR6 are rectifier diodes. The output filter is composed of Lf and Cf , and RLd is the load.

III. OPERATION PRINCIPLE

This section will analyze the operation principles of the proposed converter. The following assumptions are made for the simplicity before the analysis: 1) all power devices and diodes are ideal; 2) all capacitors and inductances are ideal; 3) the output filter inductance is large enough to be treated as a constant current source during a switching period, and its value equals output current Io ; and 4) Llka, Llkb , and Llkc are identical, and Llka = Llkb = Llkc = Llk . Fig. 5 shows the key waveforms of the proposed converter; as seen, the converter adopts symmetrical duty cycle control, and each switch has a maximum conduction period of 120◦. Evidently, if the duty cycle is less than 0.167, only one switch will turn ON at any moment, and the output voltage will be zero; furthermore, if the duty cycle is beyond 0.33, the output voltage will be uncontrolled, so the required range for the duty cycle of any switch is from 0.167 to 0.33.

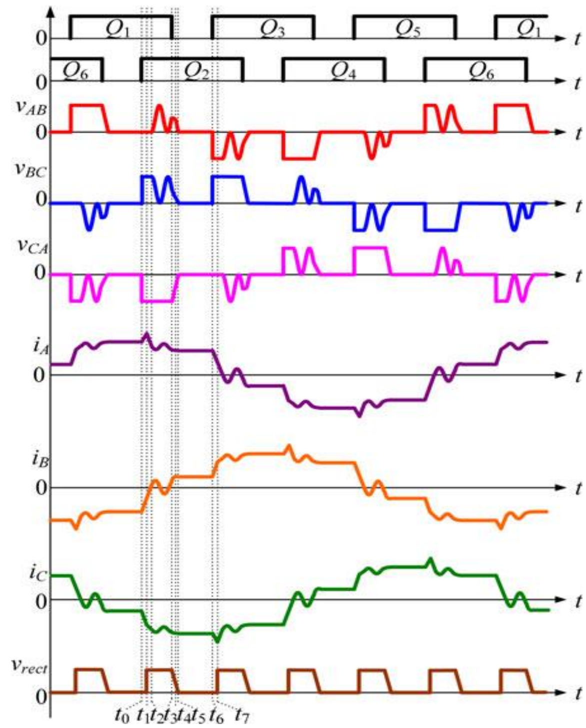
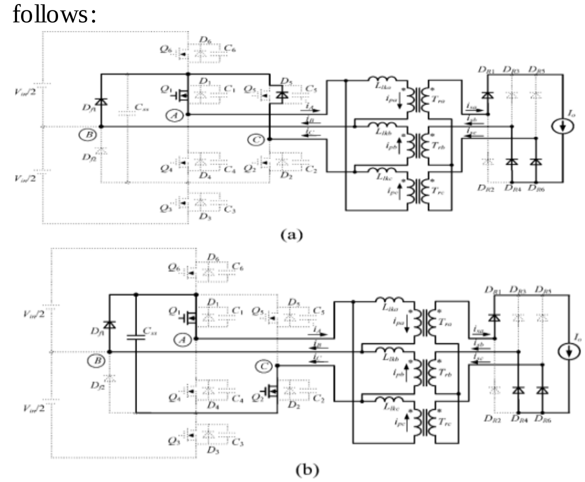


Fig. 8. Key waveforms of the proposed TPTL converter.

There are disparities between several operation principles due to different steady-state operation points and devices parameters of the converter. In this paper, only one specific example will be described due to publication space limitations. Fig. 6 shows eight operation stages of the converter under rated conditions. The other operation stages during the rest of a switching period are not depicted but they are symmetrically equivalent, expect for the fact that they are phase-shifted. The basic equations of the voltages and currents of the transformer are listed as follows:



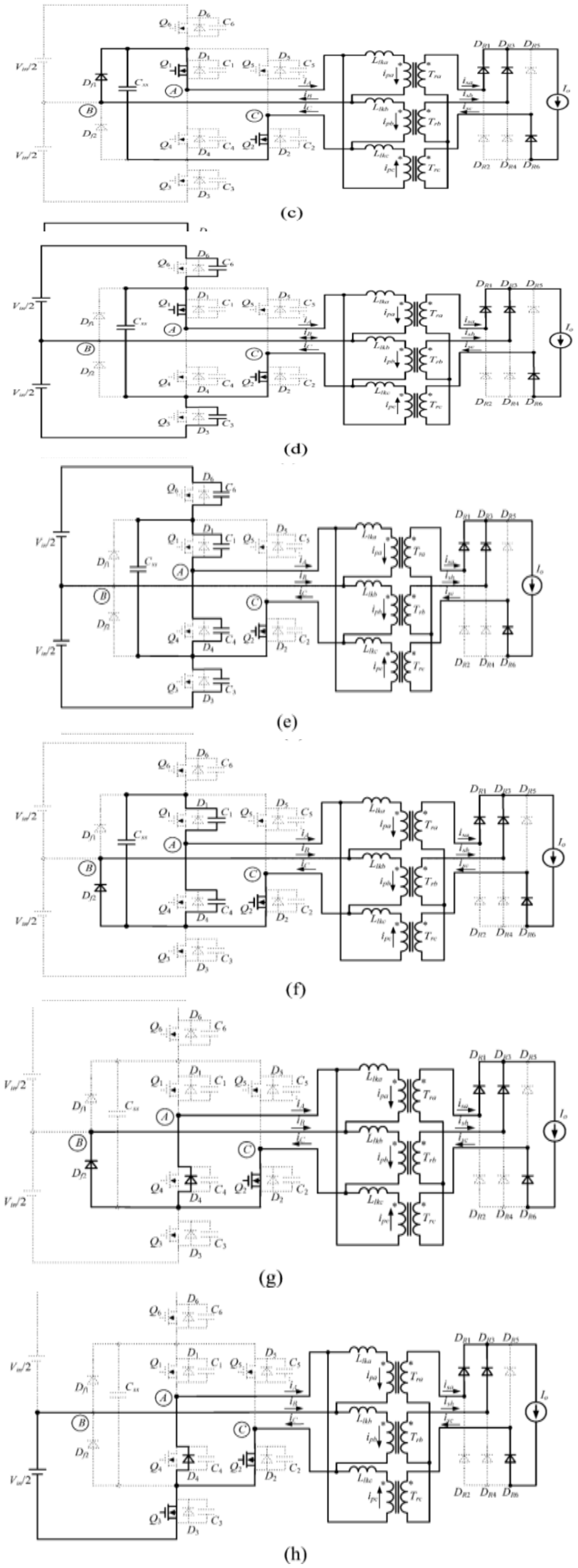


Fig. 9. Equivalent circuits under different operation stages. (a) prior to $t0$. (b) [$t0$, $t1$]. (c) [$t1$, $t2$]. (d) [$t2$, $t3$]. (e) [$t3$, $t4$]. (f) [$t4$, $t5$]. (g) [$t5$, $t6$]. (h) [$t6$, $t7$].

$$v_{AB} + v_{BC} + v_{CA} = 0 \qquad (1)$$

$$i_{sa} + i_{sb} + i_{sc} = 0 \qquad (2)$$

$$\frac{di_{pa}}{dt} = k\frac{di_{sa}}{dt} = \frac{v_{Llka}}{L_{lk}} \qquad (3)$$

$$\frac{di_{pb}}{dt} = k\frac{di_{sb}}{dt} = \frac{v_{Llkb}}{L_{lk}} \qquad (4)$$

$$\frac{di_{pc}}{dt} = k\frac{di_{sc}}{dt} = \frac{v_{Llkc}}{L_{lk}} \qquad (5)$$

where k represents the secondary-to-primary turns ratios of the transformer. The voltage of leakage inductance of the transformer can be derived from (2)–(5) and is given in the following equation:

$$v_{Llka} + v_{Llkb} + v_{Llkc} = 0. \qquad (6)$$

1) Stage 1 [prior to t0] [see Fig. 6(a)]: Prior to t0,Q1,Df 1 , and D5 are conducting in the primary side; the voltages of the transformer windings are zero, so the rectified voltage vrect is zero too.

2) Stage 2 [t0, t1] [see Fig. 6(b)]: At t0,Q2 is turned ON with hard-switching condition and the current transfers from D5 to Q2 . vBC rises to Vin /2 while vCA decays to −*V*in /2. In the primary section of the converter, the sum of *vLlka* and *vpa* is zero, and the sum of *vLlkc* and *vpc* is −*V*in /2. Meanwhile, in the secondary section of the converter, *vsb* is equal to *vsc* , and *v*rect is the difference between *vsa* and *vsc* . The secondary current of *Tra*, *isa*, is equal to *Io* , so the primary current of *Tra*, *ipa* , is constant as *kIo* ; then, *vLlka* is equal to zero. From (1), (2), (6), and the conditions mentioned above, the three-phase line currents *iA*, *iB* , and *iC* can be obtained.

$$i_A(t) = i_A(t_0) + \frac{V_{\text{in}}}{2L_{lk}}(t - t_0) \qquad (7)$$

$$i_B(t) = i_B(t_0) + \frac{V_{\text{in}}}{2L_{lk}}(t - t_0) \qquad (8)$$

$$i_C(t) = i_C(t_0) - \frac{V_{\text{in}}}{L_{lk}}(t - t_0). \qquad (9)$$

From (7)–(9), iC decays while iA and iB rise linearly. The primary current of transformer-B, ipb , increases with iB ; when ipb rises to zero, DR4 turns OFF and DR3 turns ON naturally, in which a commutation process in the secondary stage is completed. 3) Stage 3 [t1, t2] [see Fig. 6(c)]: During this stage, Q1,Q2,Df 1,DR1,DR3 , and DR6 are conducting. Similarly, from (1), (2), (6), and other constraints between voltages

IV. SIMULATION RESULTS

Here the simulation is carried out by different cases are shown in below by using Matlab/simulink software.

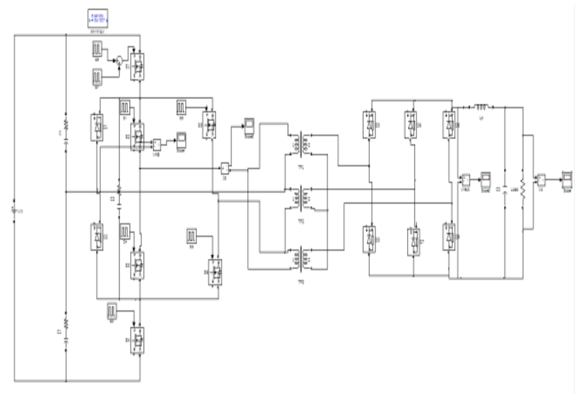


Fig.10. matlab/simulink model of proposed concept

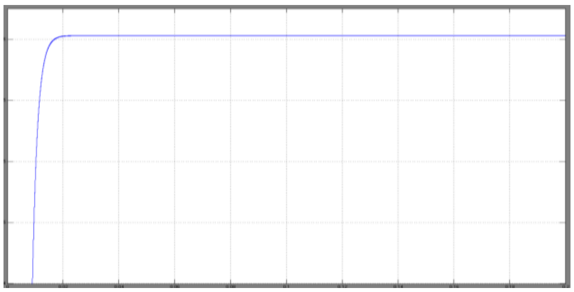


Fig.11. simulation waveform of speed

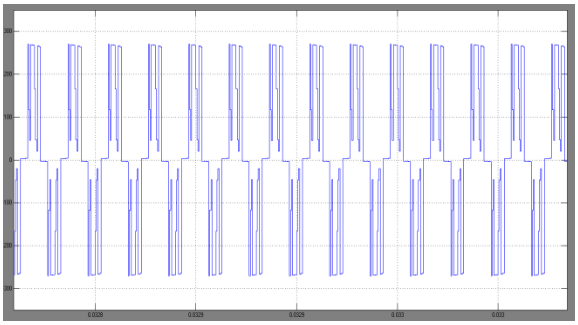


Fig.12. waveforms at full load and nominal voltage

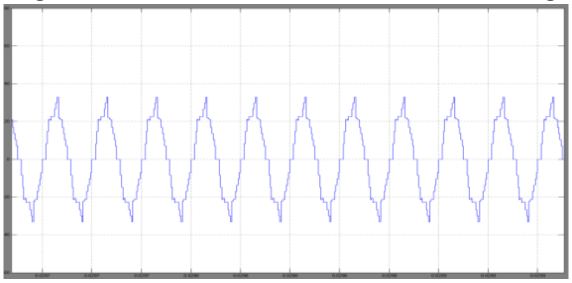


Fig.13. waveforms at full load and cureent

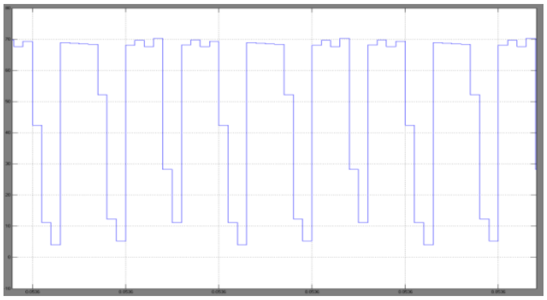


Fig.14. waveforms at full load and switching voltage

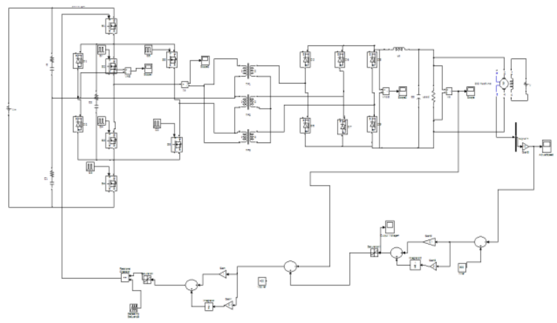


Fig. 15 matlab/ simulink model of dc motor drive

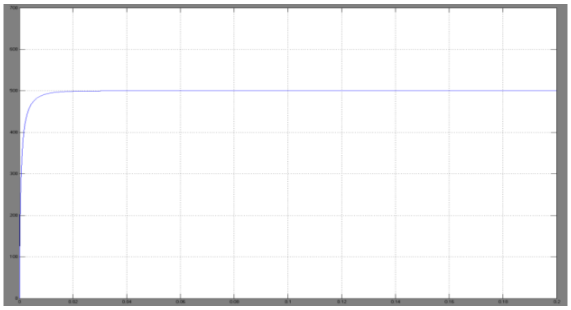


Fig.16. waveform of motor speed

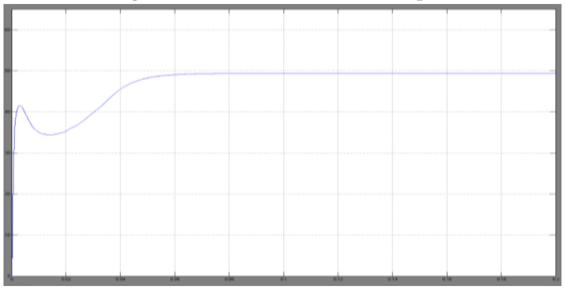


Fig.17 waveforms at full load and nominal voltage

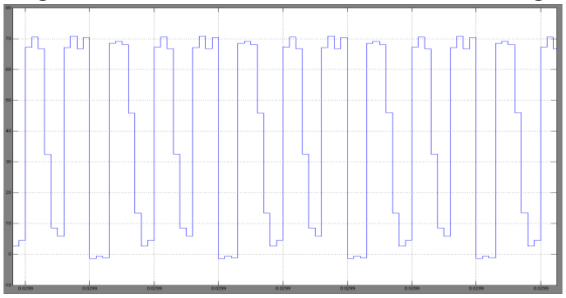


Fig.18. waveforms at full load and nominal voltage

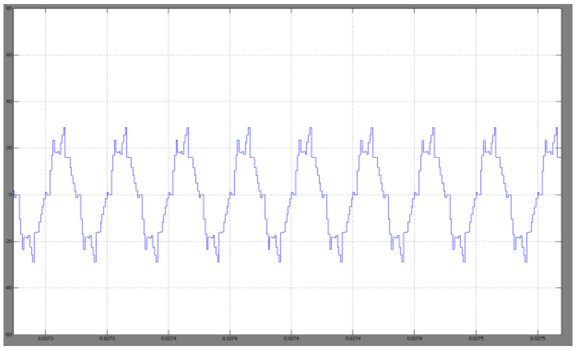


Fig.19. waveforms at full load and current

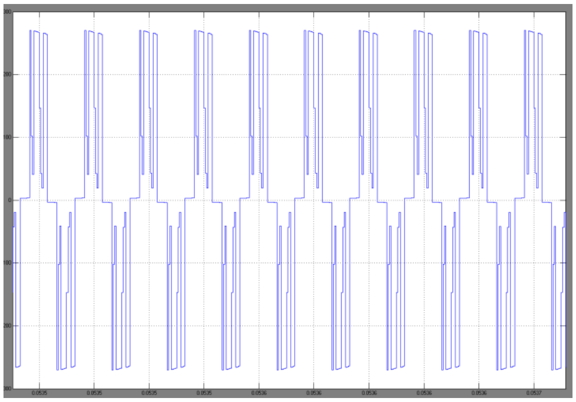


Fig.20. waveforms at full load and switching voltage

V.CONCLUSION

A novel ZVS Three-Level DC/DC converter was introduced in this paper. The operation stages and characteristics of the proposed converter were presented. It was shown that this converter reduces the voltage stresses across the main switches to half of the input voltage. Therefore, devices with lower voltage rating, which present better characteristics, can be used. Besides, the addition of a flying capacitor in the primary side allows ZVS operation for all switches with phase-shift control. These characteristics make the proposed converter an interesting option for high voltage, high-power applications that require high efficiency. The proposed converter has a voltage-fed characteristic at the input side, which will lead to a high input current ripple. The theoretical analysis has been validated by the experimental results obtained from a prototype of 1 kW and operating at 50 kHz. For the higher switching loss will degrade the performance of the proposed converter, it is necessary to investigate the improved control schemes in the next step to realize the soft-switching for switches.

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