Cadence Design of Transient Fault Tolerant Latches in 45nm Technology

Mallikarjunarao Jangam, B.Ramarao
Assistant., professor VLSI System Research Group, Department of Electronics and Communication Engineering, Amrita Sai Institute of Science &Technology, Paritala, AP,India.

***Abstract*- As the technology is going on increasing rapidly the electronic component units are also increasing. chip density is rapidly growing so there is a need for the low power memory devices to transfer information from one place to another without any loss so there is a need for building low power block of the memory device. so with the help of this block we can build efficient low power memory devices. A Transient Fault Tolerant latch is presented that is insensitive to transient faults affecting its internal and output nodes by design, independent of the size of its transistors. The above Latch is implemented with 90nm and 45nm CMOS Technology and a comparative statement to be made for speed and power consumption. A novel 8-T Transient Fault Tolerant latch is proposed and the same is implemented with a standard 45 nm CMOS technology using Cadence tool. The proposed latch is going to be designed by changing the (W/L) ratios of the transistors to achieve low power. Our approach is to change the technology for obtaining better performance and low power compared to the previous approach. Our proposed latches are particularly suitable to be adopted on critical paths.**

***Index Terms*- Transient faults, soft errors, static latch, robust design.**

I. INTRODUCTION

The operation of low frequency circuits in the sub-threshold region stands out as the optimal method of power reduction. Supply voltage scaling reduces both active energy dissipation and leakage power. When applied aggressively, voltage scaling leads to sub-threshold (sub- VT) operation. In this regime, severely degraded on/off current ratios and increased sensitivity to process variations are the main challenges for sub- circuit design in 90nm and 45nm technologies and below.

Sub-threshold circuit operation is driven by currents much weaker than standard strong-inversion circuits, and so is characterized by longer propagation delays and limited to lower frequencies. Due to the exponential dependency on the value of VTH, sub-threshold circuits are very sensitive to process variations and temperature fluctuation. These, and other factors, have to be taken into consideration when designing circuits for sub-threshold operation.

The continuous advances of microelectronic technology are leading to an aggressive reduction of device dimensions down to the nanometer region. Because of the consequent reduction of circuit node capacitances together with the simultaneous decrease of power supply voltages, the amount of charge stored on a circuit node is becoming increasingly smaller, making circuits more susceptible to Spurious voltage glitches caused by cosmic ray neutron or alpha particle hits. Such spurious voltage glitches are generally referred to as transient faults (TFs). If in the past TFs had been a concern only for space applications, they are recognized as a problem even at the sea level. In particular for terrestrial applications, high energy neutrons are the dominating source of TFs, and the susceptibility of modern ICs to TFs is expected to increase with the scaling of technology node. When a TF affects a memory cell or a storage element (latch or flip-flop), it can cause a flip of the stored bit, thus giving rise to a soft error (SE), also referred to as single-event upset (SEU). Soft errors have traditionally been recognized as a problem for high-density memories, because of their small cell size. Error-correcting codes (ECCs), in particular single error-correcting/double error-detecting codes, have been successfully employed to guarantee a satisfactory level of memory reliability. Recently because of the increasing probability of

having multiple bit upsets, memory designers are facing new and challenging problems.

An SE may also be generated because of a TF affecting combinational logic, when the generated spurious voltage glitch propagates till the input of a sampling element. In this regard, however, it has been proven that SEUs storage elements (latches and flip-flops) within sequential logic are by far the largest contributor to soft error rate (SER) in logic. For this reason, extensive research efforts have been recently devoted to devising novel hardening schemes/approaches for latches and flips-flops. Some approaches rely on the modification of the latch structure in order to make it robust independently of the hitting particle energy. This is the case of the scheme proposed in, referred to as the DICE cell, and the latch in. These latches make use of two independent feedback loops controlling the output. This way, a TF affecting one of the loops cannot alter the output logic value.

The latches and present this characteristic. As for the latches in their robustness relies on the deactivation of the feedback loop (during the latching phase), thus avoiding the generation of soft errors due to TFs affecting their nodes. The latch in instead, reuses the scan portion of a scan FF to duplicate the latch, thus producing two independent values that are feeding an output stage first Exploited in for robust latches, then denoted as C-element. For all these latches, TFs affecting any of their internal or output nodes cannot produce an output SE. Other approaches aim at improving the latches' robustness against TFs by increasing node capacitances.

This approach is adopted by the latches. In particular, the robustness of derives from the idea of either splitting the internal nodes and adopting proper feedback structures, or using a Schmitt trigger-like scheme. Instead, solutions in improve the latch robustness by inserting either explicit capacitances, or transistors acting as filters for voltage glitches. All latches in include nodes that, if affected by TFs, may produce an output SE. In this paper, first a new robust latch able to tolerate TFs independently of the hitting particle energy is presented. It is based on the latch structure introduced in, and will be hereinafter referred to as High-Performance Robust (HiPeR) latch. Then, a modified version of such a HiPeR latch is also proposed that is suitable to be used together with clock gating (CG). TFs affecting some internal nodes of the HiPeR latch may leave its output in high impedance state.

If this event happens when clock gating is activated to reduce power consumption, the high-impedance node may be improperly charged/discharged to an incorrect logic value due to leakage current, and an SE may originate. This is not expected to be a problem if clock gating is not adopted. In fact, also in the perspective of increasing leakage currents with technology scaling, since the latch operation frequency will also increase, the output of the latch will remain in a high-impedance state for a time interval that will be too short to allow leakage currents to charge/discharge the output node. To cope with the problem possibly arising in case of clock gating, the HiPeR latch is proposed. Differently from HiPeR, HiPeR is such that its output cannot remain in a high-impedance state when a TF affects any of its internal nodes, thus being suitable to be used together with clock gating.

The proposed latches are compared to each other, as well as to the standard latch, and to the most recently presented robust latches we are aware of. The solution in has not been considered for comparison purposes, since it is oriented to scan FFs. It will be shown that the HiPeR and HiPeR latches feature considerably better characteristics in terms of performance than all other considered robust latches, but for the latch in, which presents a comparable input output delay. In addition, our proposed latches provide higher or comparable robustness to TFs compared to the considered alternative robust solutions, except for the latch in, which features the higher robustness.

This latter, however, is the one with the highest cost in terms of area and power among all compared latches. More in detail, our latches feature higher area than the latches presenting lower robustness while, as for power, the latch in is the less consuming robust solution, but it is considerably slower and less robust than our proposed latches. Finally, compared to the latch in, the proposed solutions present comparable area, power, and robustness, but are considerably faster. Therefore, thanks to the good trade-offs in terms of performance, robustness, and cost, our proposed latches are particularly suitable to be adopted on critical paths. The HiPeR latch structure and behavior are described. Some results of the electrical-level simulations performed to verify the

HiPeR latch behavior are reported. The effects of leakage currents on the HiPeR latch, when clock gating is applied, are analyzed. The HiPeR latch is introduced. Some results of the electrical-level simulations performed to verify the HiPeR latch behavior are reported. The proposed latches are compared to each other, and to alternative solutions (including the standard latch), considering cost and TF robustness as metrics for comparison.

There are three main sources of power dissipation in the latch:

- Internal power dissipation of the latch, including the power dissipated for switching the output loads
- Local clock power dissipation, presents the portion of power dissipated in local clock buffer driving the clock input of the latch
- Local data power dissipation, presents the portion of power dissipated in the logic stage driving the data input of the latch

II.PROPOSED SCHEMATIC

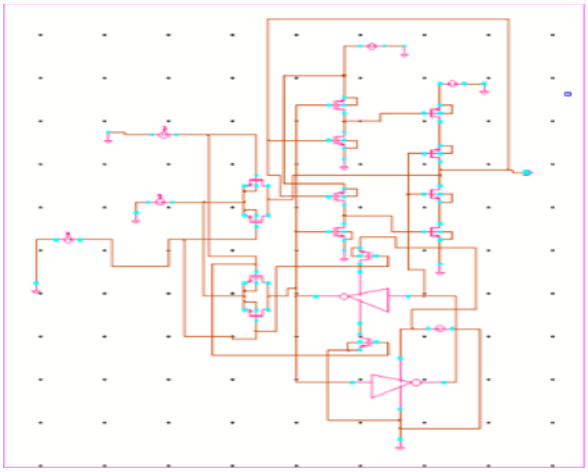

Fig.1 HiPeR Latch design in cadence

The proposed HiPeR latch relies on two basic principles:

1) Triplication of the latch internal node driving a special output stage (first exploited in for robust latches, then denoted as C-element in allowing the output to change its logic value accordingly to the value of the majority of the internal nodes and 2) design of two proper independent feedback loops that are activated during the latching phase (here assumed to occur when CK = 1). The idea in 1) above allows tolerating TFs affecting internal nodes, while the design principle in 2) allows tolerating also TFs affecting the output node. As for TFs affecting the input node.

The HiPeR latch provides high robustness, similarly to the previous solutions in. The electrical scheme of the proposed HiPeR latch is shown in Fig. 1. Transistors MN3 and MP4 (driven by the output Q) should be dominant over transistors MP3 and MN4 (driven by the internal node INT2), respectively. The behavior of the latch will now be described in detail. When CK = 0, the latch is transparent, and the logic value d at the input node D propagates to the output Q and to the internal node INT2 through transfer gates TG1 and TG2, respectively. Then, the complemented logic value d0 propagates to the internal nodes driving the output C-element, that is INT3 (through inverter I2), INT1a (through the series MP3-MN3), and INT1b (through the series MP4-MN4). Thus, the C-element confirms the logic value d at the output node Q. It is worth noticing that, when CK = 0, MP7 and MN7 are OFF to avoid possible contention on node INT2. Furthermore, TFs affecting the latch during the clock low phase are not of concern, since the output of the latch is not valid during such a clock phase. Instead, when CK = 1, the transfer gates TG1 and TG2 are OFF and the input node D is disconnected from the output node Q. The value previously charged on node Q is maintained by the C-element, which is driven by two independent feedback loops (Fig. 1): 1) the feedback loop denoted by FL1, including the output node Q and the internal nodes INT1a and INT1b and 2) the feedback loop denoted by FL2, composed by the back-to-back inverters I1 and I2 and including internal nodes INT2 and INT3. This way, if a TF affects a latch internal node, it may change the state of only one of the two feedback loops, so that the logic value at the output Q is preserved. Furthermore, thanks to the previously mentioned dominance of transistors MN3 and MP4 (driven by the output Q) over transistors MP3 and MN4 (driven by internal node INT2), TFs affecting nodes INT2 or INT3 cannot change the logic values of nodes INT1a and INT1b, so that they cannot alter the output value Q. Let us now describe in detail the behavior of the latch in case of TFs affecting its internal and output nodes when CK = 1 (latching phase). In case of TFs affecting the internal node INT1a, the following two conditions can be distinguished: 1) Q = 1, thus INT1a = INT3 =0 (the series MP5-MP6 is on) and 2) Q = 0, thus INT1a

=INT3 = 1 (the series MP5-MP6 is OFF). In case 1), the TF makes INT1a flip to 1, thus temporarily turning OFF MP5, and leaving the output Q in a high-impedance state.

However, the correct logic value of the output is not altered, and the conductive transistor MN3 restores the correct value 0 on INT1a, thus making MP5 turn on again. In case 2), the TF makes INT1a flip to 0, thus temporarily turning on MP5. However, since INT3 = 1, MP6 is kept OFF and the logic value of Q is not altered. Similarly, in case of TFs affecting INT1b, the following two conditions might be in order: 1) Q =1, thus INT1b = INT3 =0 (the series MN5-MN6 is OFF); 2) Q = 0, thus INT1b = INT3 = 1 (the series MN5-MN6 is on). In case 1), the TF makes INT1b flip to 1, thus temporarily turning MN6 on. However, since INT3 =0 (it is not altered by the TF) MN5 remains OFF, and the logic value of Q is not altered. In case 2), the TF makes INT1b flip to 0, thus temporarily turning OFF MN6 and leaving the output Q in a high impedance state, thus not altering its correct logic value. As for TFs affecting INT2 and INT3, they may produce incorrect logic values on both nodes INT2 and INT3, since the positive feedback loop constituted by inverters I1 and I2 could confirm the wrong voltage value till the following CK cycle. The incorrect logic value on INT2 may turn on transistors MP3 or MN4, thus generating a contention between transistor MP3 and MN3 (that are driving node INT1a), or between transistors MP4 and MN4 (that are driving node INT1b). Despite the possible contention, INT1a and INT1b do not change their logic value, since MN3 and MP4 (driven by the output node Q) are dominant over MP3 and MN4. However, the electrical conflict gives rise to an increase in static power consumption till the following clock cycle. Moreover, both the series MP5-MP6 and MN5-MN6 are turned OFF, thus leaving node Q in a high-impedance state, so that the correct output value is maintained and the latch keeps on working correctly. As for TFs affecting the output node Q when CK = 1, similarly to the case of the previous solutions in, they generate only a voltage glitch, whose width and amplitude depend directly on the amount of charge injected by the hitting particle, and inversely on the strength of the transistor driving the node (that is, the series MP5-MP6 or MN5-MN6) and on the fan-out load. Afterward, since the series of transistors driving the output node keeps on conducting also after the TF exhaustion, the correct output value is restored. Finally, let us consider the case of a TF affecting node INT2 or INT3 when the clock is gated. If a following TF affects node Q, an incorrect logic value may be feed backed, thus giving rise to an SE.

III.EFFECTS OF LEAKAGE OF CURRENTS ON HIPER LATCH

In this section, we analyze the effects that leakage currents can produce on the HiPeR latch, when clock gating is employed to reduce power consumption. As described in Section 2, TFs affecting nodes INT2 or INT3 when CK =1 may produce incorrect logic values on both nodes INT2 and INT3. These incorrect logic values are Fig. 2. Simulation results obtained for nominal values of electrical parameters and TFs affecting the internal feedback nodes (a) INT1a and (b) INT1b. Simulation results obtained for nominal values of electrical parameters and TFs affecting the internal feedback nodes (a) INT2 and (b) INT3. Simulation results obtained for nominal values of electrical parameters and TFs affecting the output node Q. maintained till the next clock phase making the latch transparent (CK =0). As a consequence, a contention between transistors MP3 and MN3 (driving node INT1a), or between transistors MP4 and MN4 (driving node INT1b) is generated. This contention does not change the logic values on INT1a and INT1b, thanks to the dominance of transistors MN3 and MP4 over transistors MP3 and MN4, respectively. However, it gives rise to static power consumption. Moreover, the flip of INT2 and INT3 moves one of the internal nodes INT1a (if Q = 0), or INT1b (if Q = 1) to a high-impedance state. In addition, the output C-element is turned OFF, thus making the output node Q to be also in a high-impedance state till the next clock low phase, thus retaining its correct logic value. As introduced earlier, even in the perspective of significantly increased leakage currents with scaled technologies, since the latch operation frequency will also increase with scaling, the output Q and nodes INT1a or INT1b will remain in a high-impedance state for a time interval lower or equal to half clock cycle, which will not be long enough to allow also high leakage currents to change the logic value of these nodes. Instead, if clock gating is implemented to reduce

power consumption, the clock may be fixed to a constant value for long time intervals, which can be much longer than a single clock period. In this case, if a TF affects either INT2 or INT3, nodes Q and INT1a, or INT1b may remain in a high impedance state for a time interval long enough to be possibly charged/discharged to incorrect logic values by leakage currents.

In order to analyze in detail the effects of TFs affecting INT2 or INT3 when clock gating is activated, electrical-level simulations have been performed, considering the same technology, power supply, and implementation of the HiPeR latch reported in the previous section.

TF occurring at time t1 and affecting node INT2 when it presents a low logic value while reports the case of a TF affecting INT2 when it is at a high logic value. Similarly, the cases of TFs affecting node INT3 when it presents a low and a high logic value are shown in respectively. It can be observed that, in all cases, after the particle hit, nodes INT2 and INT3 flip to an incorrect logic value, thus turning off the output C-element and leaving the output Q in a high-impedance state. Particularly, after the particle hit (at time t1), the voltage on the output node Q starts slowly swinging to an incorrect logic value due to leakage currents. After a time interval $\Delta t = t2 - t1$ ranging from 31 ns to 149 ns, the output node Q moves to an incorrect logic value. More in detail, it can be observed how leakage currents flowing through the series MP5-MP6 and MN5-MN6 start to slightly charge the node Q after t1 we can observe how such leakage currents start to slightly discharge the node Q after. Simulation results for the HiPeR latch when the clock is kept constant to a high logic value and (a) a TF affects INT2 at t1, when it presents a low logic value; (b) a TF affects INT2 at t1, when it presents a high logic value; (c) a TF affects INT3 at t1, when it presents a low logic value; and (d) a TF affects INT3 at t1, when it presents a high logic value. t1. This process continues during the time interval $\Delta t = t2 - t1$ As described before, during Δt an incorrect logic value of INT2 (i.e., provoked by a TF affecting INT2 or INT3) may turn on transistors MP3 or MN4 (Fig. 1), thus generating a contention between transistors MP3 and MN3 (which drive node INT1a), or between transistors MP4 and MN4 (which drive node INT1b). The logic value on nodes INT1a and INT1b is not changed by this contention, because MN3 and MP4 are designed to be dominant over MP3 and MN4. However, the continuous increase (decrease) of the voltage on node Q due to leakage makes transistor MP4 (if Q = 0) or MN3 (if Q = 1) become less conductive, thus less dominant over transistor MN4 or MP3, respectively. At time t2, transistors MP4 or MN3 are eventually no longer dominant over MN4 or MP3, and nodes INT1a and INT1b flip to an incorrect logic value, thus making the latch provide a wrong output.

IV.PROPOSED LATCH DESIGN

Latches, flip-flops, RAMs, and other sub-circuits with memory impose specific timing requirements such as setup and hold times on data, and minimum pulse widths on clock inputs.

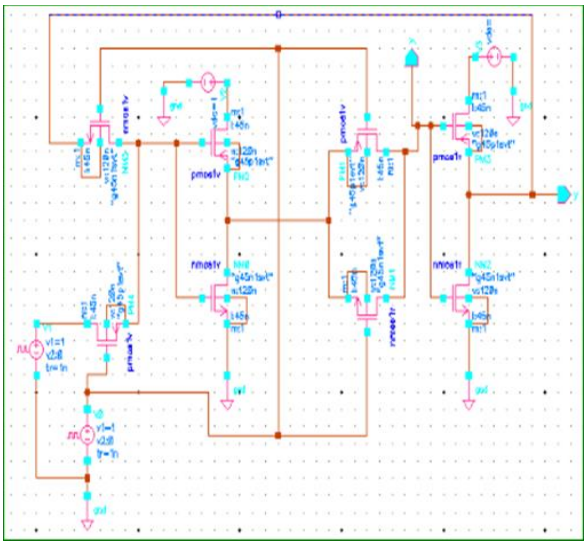

Fig 2 proposed 8-Trasistor Latch

V. SIMULATION RESULTS

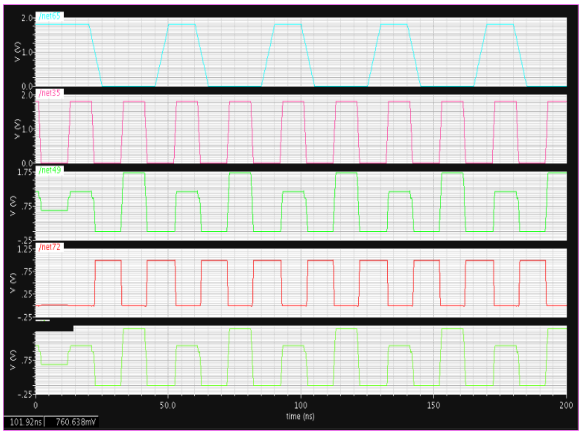

Fig 3

Simulation results obtained for nominal values of electrical parameters and TFs affecting the internal feedback nodes.

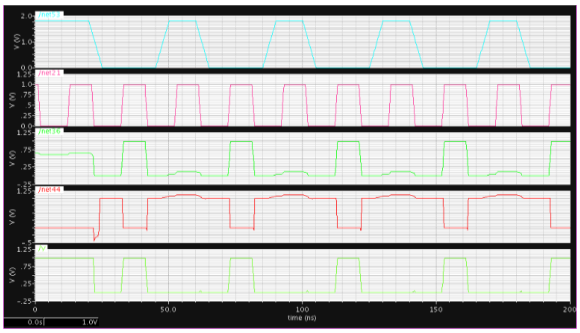

Fig 4

Simulation results obtained for nominal values of electrical parameters and TFs affecting the internal feedback nodes

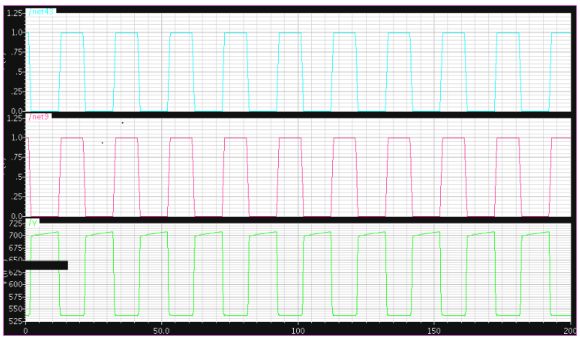

Fig 5

Output waveform of the proposed 8T latch comparison

TABLE 1

Comparison of the Hiper-Latch in different technologies

Technology	Power	Delay
90nm	24.088uw	34.48E-9
45nm	32.611uw	20.48E-9

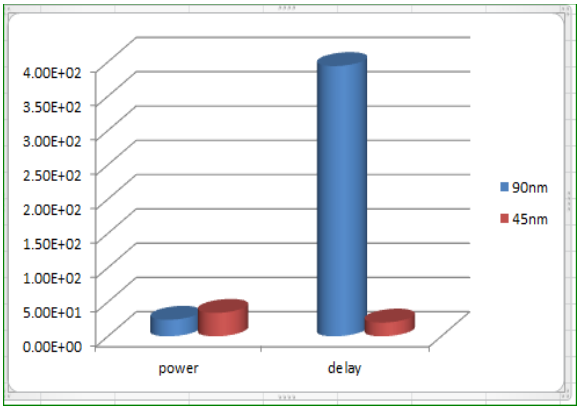

Fig: 6

Comparison of power and Delay of Hiper Latch

TABLE 2

Comparison of the 8-Transostor latch and Hiper-latch in 45nm technology

	Power	Delay
Hiper Latch	32.611uw	20.48E-9
8-Transistor	2.93uw	7.84E-9

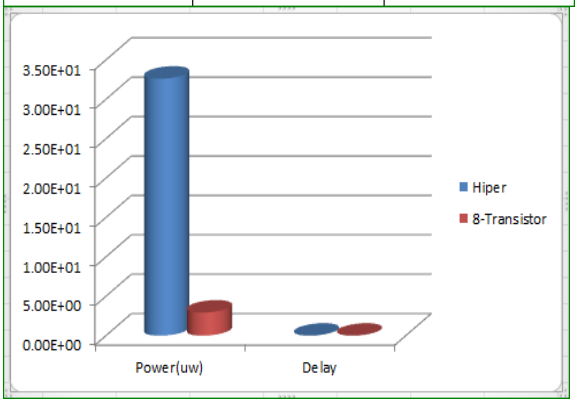

Fig: 7

Comparison of Hiper Latch and 8-Transistor latch

VII.CONCLUSION

The proposed design of 8-transistor latch is compared and found better than the Hiper Latch in terms of power consumption and delay at the variation of the parameters, i.e.(W/L) ratios of transistors. The proposed design is also technology independent as it operates better in technologies, i.e., 45nm. The tremendous decrease in delay reported in the proposed level triggered design during the simulation makes it better than the Hiper Latch design. The proposed design uses only 8 transistors compared to the 16 in and hence our design is area efficient one. This design will certainly improve the performance of the low power devices. This can be further integrated in the memory devices for better efficiency.

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