

# Optimized Error Detection for Residue Adder Using Signed Digit Arithmetic

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**Abstract-** In this paper, a new residue checker using optimal signed-digit (SD) adder tree structure is presented for the error detection of multiply-accumulate arithmetic circuit. The modulus of the residue checker is set to  $m = 2p + u$ , where  $u \in \{-1, 1\}$  and  $p$  is the wordlength of the residue checker. By switching  $u = 1$  to/from  $u = -1$ , more 2-bit errors can be detected using the same checking circuit. The fast modulo  $m$  SD adder with an end-around carry is introduced, so that the modulo  $m$  addition time is independent of the wordlength of operands of the residue checker, and the delay time of the proposed residue checker is dependent of the stages of the binary tree structure of the modulo- $m$  SD adders.

## I. INTRODUCTION

In real-time applications such as high speed digital signal processing and digital control systems, high speed VLSI circuits are the general requirements. Increased chip density and logical complexity of recent VLSI circuits with longer word length make circuit reliability critical. Hence effective detection of computation faults in real time is an important issue and various techniques have been developed for this purpose. By adding redundant moduli to a residue number system(RNS), the error detection and error correction can be done while performing arithmetic operations. Moreover, a checker with residue arithmetic can be also applied to detect the calculation error of an ordinary binary arithmetic circuit. A modulo  $2p \pm 1$  addition can be implemented by a  $p$ -bit binary adder and some modulo  $2p \pm 1$  multipliers have been proposed. Thus, modulo  $2p \pm 1$  arithmetic circuits are considered to be applied to an RNS or a residue checker for high speed computations.

## II. ERROR DETECTION BASED ON RESIDUE ARITHMETIC

Consider that a product-sum circuit, which can be used in a multiply-accumulate (MAC) unit of a digital signal processor, performs the following arithmetic function,

$$Z = A \times B + C \quad \dots\dots\dots (1)$$

In the above equation,  $A$  and  $B$  are in the  $n$ -bit,  $C$  and  $Z$  are in the  $2n$ -bit binary number representations, respectively. By converting the operands into residue numbers, that is,  $a = |A|_m$ ,  $b = |B|_m$  and  $c = |C|_m$ , we have the following residue product-sum equation,

$$z = |A|_m \times |B|_m + |C|_m \dots\dots\dots (2)$$

where

$$|X|_m = X \text{ mod } m \quad \dots\dots\dots (3)$$

and  $m = 2p + u$  and  $u \in \{-1, 1\}$ . Since  $|X|_m$  usually has a value in the following number set  $Im0$ :

$$Im0 = \{0, 1, \dots, (m - 1)\} \dots\dots\dots (4)$$

$|Z|_m$ ,  $|A|_m$ ,  $|B|_m$  and  $|C|_m$  are in the  $p$ -bit binary number representation, respectively. We convert the result of the product sum calculation of Eq.(1) into a residue number,

$$z' = |Z|_m = |A \times B + C|_m \dots\dots\dots (5)$$

An error of the product-sum calculation occurs and results in  $Z' = Z = A \times B + C$ . If  $z' = |Z'|_m \neq z = |A|_m \times |B|_m + |C|_m$ , then the error can be detected. Therefore, let the error signal be  $E$ ,

$$\text{then } E = z - z' \dots\dots\dots (6)$$

A product-sum circuit with an error checker is usually constructed as shown in Fig.1. From Eqs.(2), (5) and (6), the residue checker consists of a residue product-sum circuit, four binary-to-residue converters and a subtraction circuit.

The binary-to-residue converters perform the operations converting  $A$ ,  $B$ ,  $C$  and  $Z$  from  $n$ -bit or  $2n$ -bit binary numbers into  $|A|_m$ ,  $|B|_m$ ,  $|C|_m$  and  $|Z|_m$  in the  $p$ -bit binary number representation, where  $n \gg p$ . When  $E \neq 0$ , the calculation error, which may occur in the product-sum circuit or in the error checker, is detected.

In conventional methods, the residue checker is implemented based on the ordinary binary number arithmetic, then the carry propagation and the complicated residue operation limit the operation speed of the residue checker. The critical delay time in the arithmetic circuit is dominated by the residue arithmetic circuits for the error detection.

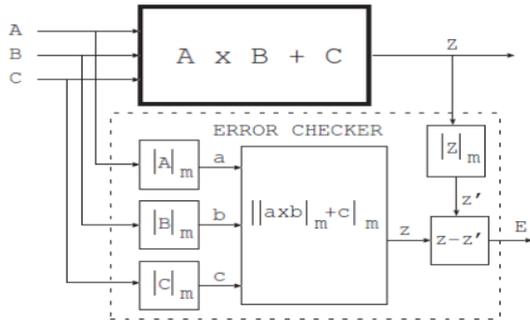


Fig1. Block Diagram of Product-Sum Circuit

III. RESIDUE ADDITION WITH

SD-NUMBER SYSTEM

Residue additions for the moduli in the form of  $2^{p \pm 1}$  and  $2^p$  are widely used, because they offer the ability to generate remainders without any memory. However, when a binary number system is used to perform the residue addition, the carry propagation will arise inside the residue digit and the speed of arithmetic operation will be limited. A common addition  $Z = X + Y$  in SD number system, X and Y are p-digit SD numbers, can be performed in parallel as follows: Let  $c_i$  and  $s_i$  be the carry and the intermediate sum of  $i^{th}$  digit position, respectively. Their values are determined by a particular rule with respect to the values of,  $y_i, x_i, x_{i-1}, y_{i-1}$ , as shown in Table I, then compute the final sum by  $z_i = s_i + c_{i-1}$ , where  $i = 0, 1, \dots, p-1, x_{-1} = 0, y_{-1} = 0$  and  $c_{-1} = 0$ . Residue generation for such popular moduli can be done easily by the additional end-around-carry operation for modulo  $2^p + u$ , as follows.

Step1: Use Table I to determine  $c_i$  and  $s_i$  where  $x_{-1} = u \times x_{p-1}, y_{-1} = u \times y_{p-1}$

$a_i$	$a_i(1)$	$a_i(0)$
-1	1	1
0	0	0
1	0	1

Binary Representation For Sd Addition

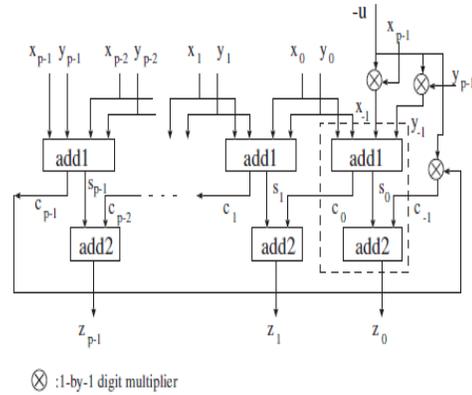


Fig2: Block Diagram Of Sd-Adder

Step2: Compute the final sum by  $z_i = s_i + c_{i-1}$ , where  $c_{-1} = u \times c_{p-1}$ .

Figure.2 illustrates the circuit diagram and symbol of a modulo m SD number adder consisting of p add 1's and p add 2's, where  $m = 2^p + u$  and  $u \in \{-1, 1\}$ . The add1 generates the  $c_i$  and the  $s_i$ , and the add2 sums the  $c_{i-1}$  and  $s_i$ . The residue addition can be performed in parallel without the carry propagation.

Word Length	AREA ( $\mu m^2$ )		DELA Y(ns)	
	Binary	SD	Binary	SD
4	44629	45788	12.68	8.42
8	66133	47429	13.04	7.85

PERFORMANCE OF RESIDUE CHECKER WITH n=32

IV. CONCLUSION

This paper has presented a high-speed residue SD number adders between binary and residue numbers for moduli  $2^n, 2^{n-1}, 2^{n+1}$ . In the proposed method, only some fast SD additions are used for the arithmetic operations and the conversions.

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