Assessment of Power Optimization Using VLSI Techniques

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***Abstract*- With the advancement in compact, portable and high-density micro-electronic devices and systems, the power dissipated in very large scale integrated (VLSI) design circuits has become a critical concern. Accuracy and efficiency in power estimation involved in the design phase is important in order to meet power specifications without high cost redesign process. This paper, presents a review of the power optimization theory approach and the estimation techniques of recent proposition. VLSI design has fascinating application area for all combination circuit optimization. In virtual context all classical combination optimization issues, occur in natural way as subtasks. The rapid technological advancement and major theoretical concept advances the mathematics of VLSI design, which has changed significantly over the last two decades. This survey paper also gives a recent account on the key factors in optimization design. And presents a survey of layout techniques in order to design low power digital CMOS circuits. It describes the problems faced by the designers at the physical design abstraction and reviews some of the techniques which are proposed to overcome these difficulties.**

***Index Terms*-Optimization, VLSI, physical design, layout, placement, routing, MED, BDD, CMOS.**

I. INTRODUCTION

In the past decades, the main concerns of VLSI designers were area, performance, cost involved and reliability; power consumption was mostly of only secondary importance to other things. However, this has begun to change and, with major priority, power consumption is given comparable importance to area and speed. Numerous factors have contributed to this. Portable computing and communication devices demand high-resolution of fast computation and complex functional style with reduced power consumption. Heat generation in high-end computer products limits the feasible packing and performance of VLSI circuits and increases the packaging and cooling costs. Circuit and device reliability deteriorate with increased heat dissipation, and thus the die temperature. Heat pumped into the rooms, the electricity consumed and the office noise diminishes with low power LSI chipset. Our goal in writing this paper is to provide background and outlook for people interested in using or developing low power design methodologies and techniques.

Even though we tried to be complete, some significant research work might have been unintentionally left out. The paper is organized as follows. First, we describe sources of power dissipation in CMOS circuits and degrees of freedom in the low power design space. We then present an in-depth survey (and in many cases analysis) of power minimization techniques and describe some of the frontiers of the research currently being pursued. We conclude by summarizing the major low power design challenges that lie ahead of us. Managing the power of an IC design adds to a growing list of problems that IC designers and design managers have to contend with. Computer Aided Design (CAD) tools are needed to help with the power management tasks.

In CMOS and Bi-CMOS technologies, the chip components (gates, cells) extract power supply current only if a logical transition takes place(ignoringsmall leakage current). While considered an attractive low-power feature technology, it also makes the power-dissipation greatly dependent on the switching activities inside these circuits. Simply put, a more active circuit will consume more power. This complicates the power estimation problem because the power becomes a moving target-it is input pattern dependent. Thus the simple and straight-forward solution of estimating power by using a simulator is severely complicated by this pattern-dependence problem. Input signals are generally unknown during the design phase because

they depend on the system (or chip) in which the chip (or functional block) will eventually be used. Furthermore, it is practically impossible to estimate the power by simulating the circuit for all possible inputs.

Recently, several techniques have been proposed to overcome this problem by using probabilities to describe the set of all possible logic signals, and then studying the power resulting from the collective influence of all these signals. This formulation achieves a certain degree of pattern-independence that allows one to efficiently estimate and manipulate the power dissipation.

Sources of Power Dissipation

Power dissipation in digital CMOS circuits is caused by four sources as follows.

• The leakage current, which is primarily determined by the fabrication technology, consists of two components:

1) Reverse bias current in the parasitic diodes formed between source and drain diffusions and the bulk region in a MOS transistor, and
2) The sub-threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage,

- The standby current which is the DC current drawn continuously from Vdd to ground,
- The short-circuit (rush-through) current which is due to the DC path between the supply rails during output transitions,
- The capacitance current which flows to charge and discharge capacitive loads during logic changes.

The term static power dissipation refers to the sum of leakage and standby dissipations. Leakage currents in CMOS circuits can be made small with proper choice of device technology. Standby currents are important only in CMOS design styles like pseudo-nMOS and nMOS pass transistor logic. In this article, we assume that the standby dissipation is insignificant, thus limiting ourselves to CMOS technologies, logic styles and circuit structures [1] in which this condition holds.

The dominant source of power dissipation CMOS circuits is the charging and discharging of the node capacitances (also referred to as the capacitive power dissipation) and is given by:

$$P = 0.5CLVdd2\ E(sw)fclk \quad (1)$$

Where CL is the physical capacitance at the output of the node, Vdd is the supply voltage, E(sw) (referred to as the switching activity) is the average number of out-put transitions per 1/fclk time, and fclk is the clock frequency.

The term dynamic power dissipation refers to the sum of short circuit and capacitive dissipations. Using the concept of equivalent short-circuit capacitance described above, the dynamic power dissipation can be calculated using equation (1) if we add CSC to CL. Short-circuit currents in CMOS circuits can be made small with appropriate circuit design techniques [2]. In most of this article, we will thus focus on capacitive power dissipation.

II.POWER MINIMIZATION TECHNIQUES

The challenge to reduce power, the semiconductor industry adopted a multi-faceted approach, attacking the problem from many fronts:

1. Reduction in chip and packaging capacitance: Achieved through process development, SOI with
2. partially or fully depleted wells, CMOS scaling to submicron device design size, and advanced interconnected substrates such as Multi-Chip Modules (MCM).
3. Scaled supply voltage: Very effective in reducing the power dissipation, but requires new IC fabrication process system. Supply voltage scaling also requires support circuitry for low-voltage operation.
4. Improving design techniques: Can be very successful as the cost to reduce power by design is relatively small in comparison to the other approaches and considered high in potential.
5. Power management strategies: various static and dynamic power managing techniques are application dependent, but, also prove to be significant.

III.PHYSICAL DESIGN AUTOMATION

It provides the automatic layout of circuits minimizing some objective function subject to given constraints. Depending on the target design style, the

packaging technology (pcb, multi-chip modules, wafer-scaled integration) and the objective function (area, delay, power, reliability), various optimization techniques are used to partition, place, resize and route gates. Layout problems become more complicated under a real-delay model, which accounts for glitches in the circuit, because layout optimization operations influence the glitch activity in ways that cannot be accurately and reliably predicted.

In the recent past, post-layout optimization techniques (such as buffer and wire sizing, local restructuring and re-mapping) for power reduction (or area and delay recover given a fixed power budget) have become commonplace. The advantage of these techniques is that re-synthesis tools allow more global changes to the circuit structure compared to layout tools. At the same time, the re-synthesis tools have access to detailed post-layout information that allows accurate estimation of circuit area, delay and power dissipation.

Circuit Partitioning

Netlist partitioning is key in breaking a complex and large design into smaller pieces which are subsequently optimized and implemented as separate blocks. This is often needed to satisfy I/O pin constraints on the blocks, reduce the complexity of subsequent optimization steps, or improve performance. Traditionally, the objective functions for partitioning have been the cut-size and/or the circuit delay while the constraints have been I/O pin count per block and block size. Partitioning for low power has recently become an important problem.

Node Clustering

As a result of logic extraction, it is possible to increase the circuit depth to such an extent that the circuit delay becomes unacceptably large. This problem is often mitigated by a reduce depth operation that implements a depth optimal node clustering algorithm based on [3].

This algorithm however makes no attempt to explore alternative clustering solutions that result in the same logic depth, but have lower power dissipation. This is achieved by enumerating, in post order, all candidate clusters of up to a maximum cluster size and selecting the power-optimal cluster solution for each delay value at every gate in the circuit. The algorithm produces optimum delay solutions for general directed acyclic graphs, but the results are not power-optimum because of the possible logic duplication at the multiple fan-out nodes in the circuit. Thus, it is often necessary to perform a delay constrained power-recovery step as a post-process.

Floor planning

Floor planning is assigning shapes, pin positions and locations to a set of macro-cellular or modules for minimizing area of the floor plan. A successful floor planning approach is based on computing the shape functions (height versus width trade-off curves) during a post order traversal of a cluster tree that captures the connectivity among modules. The optimal floor plan topology, block shapes and room assignments, and pin positions (or block orientations) are determined during a pre order traversal of this tree [4, 5]. The two dimensional shape function curves can be indexed by the power cost, that is, for each distinct power dissipation value, one shape function is built. These indexed shape functions can then be used during the pre order traversal to compute the optimal power solution which also leads to minimum chip area as in [6].

Global Routing

Global routing produces routing trees for all nets in the circuit so as to minimize the interconnect length and/or chip area. The routing trees for multi-terminal nets are often constructed as Rectilinear Spanning or Steiner trees. In routing a single net to achieve lower power dissipation, the goal is to minimize the physical capacitance which coincides with the minimum length objective used in conventional routing. Therefore, there is no new routing problem here. The main tasks of a global router for Standard Cell layouts are to generate the routing topology for each net and to determine the number of feed through cells required on each cell row. They assign a feed through penalty to each cell row which characterizes the additional cost (in terms of layout area) that a routing tree edge accrues if it crosses that row. Parallel routing algorithms alleviate the net ordering problem by constructing routing trees for all nets concurrently. One can modify the feed through insertion and net segment assignment steps in these routers to generate tree connections with smaller

lengths for nets that are driven by gates with higher switching rates [7].

Detailed Routing

Detailed routing produces the wiring geometries and layer assignments within a routing channel, switchbox or general area. Again, we will only consider channel routing techniques commonly used in Standard Cell layouts. Given the channel length, top and bottom terminal lists, left and right connection lists, and the number of routing layers, the channel routing problem is to find interconnections of all the nets in the channel including the connection sets so that the channel achieves minimum height. The objective function for low power routing becomes the switched capacitance within the channel, that is, high activity nets should assume their shortest possible route at the expense of low activity nets. One must however achieve this with no or little increase in channel height, since otherwise, the increase in wire lengths due to larger layout area will more than compensate the reduction of switched capacitances within the routing channels.

Super Buffer Design

Super buffer design is a chain of inverters designed to derive a large capacitive load with minimal signal propagation time. A power-optimal buffer sizing technique applicable to the design of super buffers at high speed is presented in [8]. This work is based on an analytic relationship among signal delay, power dissipation, driver size and interconnect load which is in turn derived from the I-V characteristics of CMOS transistors. This work shows that optimal-power sizing requires a variable tapering (scaling) factor for the inverter chain.

Power Distribution

When supply voltage is reduced, the noise margins are effectively removed, and thus, small voltage drops in the power distribution system may have a relatively big influence on the systemcircuit speed. Careful power distribution is thus becoming more important at lower supply voltages. In [9], a technique for concurrent topology design and wire sizing in power distribution networks is presented. The objective is to minimize the layout area while limiting the average current density to avoid electro-migration-induced reliability problems and large resistive voltage drops. This technique is based on the observation that when two sinks do not draw currents at the same time, narrow wires can be used for power distribution to those sinks, thus reducing the layout area.

Probabilistic Simulation (CREST)

This approach [10, 11] requires the user to specify typical signal behaviour at the circuit inputs using probability waveforms. A probability waveform is a sequence of values indicating the probability that the signal is high for certain time intervals, and the probability that it makes low-to-high transitions at specific time points. The transition times,they are not random. This allows the computation of the average, as well as the variance, of the current waveforms drawn by the individual gates in the design in one simulation run. The average current waveforms can then be used to compute the average power dissipated in each gate and the total average power of the circuit.

Transition density (DENSIM)

The averaged amount of transitions per-second at single node in the circuit has been called the transition density in [12], where an efficient algorithm is presented to propagate the density values from the inputs throughout the circuit. This was implemented in the program DENSIM for which the required input specification is a pair of numbers for every input node, namely the equilibrium probability and transition density. In this case, both signal values and signal transition times are random.

Using a BDD

The technique proposed in [13] attempts to handle both spatial and temporal correlations by using a BDD to represent the successive Boolean functions at every node in terms of the primary inputs, as follows. The circuit topology defines a Boolean function corresponding to every node that gives the steady state value of that node in terms of the primary inputs. The intermediate values that the node takes before reaching steady state are not represented by this function. Nevertheless, one can construct Boolean functions for them by making use of the circuit delay information, assuming the delay of every gate is a specified fixed constant. Using a BDD to perform these tasks implicitly means that the BDD

variables are assumed independent. The reason is that temporal and spatial independence are effectively assumed at the primary inputs. One disadvantage of this technique is that it is computationally expensive. Since the BDD is built for the whole circuit, there will be cases where the technique breaks down because the required BDD may be too big. As a result, this approach is limited to moderate sized circuits.

Power of individual gates (MED)

This recent technique [13] is a modification of the McPower approach that provides both the total and individual-gate power estimates, with user-specified accuracy and confidence. One reason why one may want to estimate the power consumed by individual gates is to be able to diagnose a high power problem, and find out which part of the circuit consumes the most power.

Other reasons have to do with the fact that estimating gate power is essentially equivalent to estimating the transition density at every node. Indeed, the implementation of this technique in the program MED provides the transition density at every gate output node, in addition to the total power.

IV. CONCLUSION

Power estimation tools are required to manage the power consumption of modern VLSI designs during the design phase, so as to avoid a costly redesign process. Since average power dissipation is directly related to the average switching activity inside a circuit, it would not make sense to expect to estimate power without some information about the circuit input patterns. This information is usually much more readily available to designers than specific input patterns are. All these techniques use simplified delay models, so that they do not provide the same accuracy as, say, circuit simulation. But they are fast, which is very important because VLSI designers are interested in the power dissipation of large designs. In general, it is not clear that any one approach is best in all cases, but we feel that the second statistical approach (MED) offers a good mix of accuracy, speed, and ease of implementation. It may be that a combination of the different techniques can be used for different circuit blocks. The requirement for lower power systems is adapted by many market segments. There are several approaches to reducing power, and the highest economical is through designing for low power. The problem is further complicated by the need to optimize the design for power at all design phases. In summary, low power design requires a rethinking of the conventional design process, where power concerns are often overridden by performance and area considerations. This presented paper showed coverage of low power design methodologies and techniques for estimating the optimization in power of device circuits and systems.

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