Low Power Area Efficient Full Adder Cell New Approach Using GDI Technique

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Abstract- **An addition is a fundamental arithmetic operation which is used extensively in many very large-scale integration (VLSI) systems such as application-specific digital signal processing (DSP) and microprocessors. An adder determines the overall performance of the circuits in most of those systems. In this paper proposed a low power 1-bit full adder cell with less number of transistors. The power dissipation and area using the new design are analyzed and compared with those of other designs using tanner tool. The results show that the proposed adder has both lower power consumption and less area.**

Index Terms- **Complementary Metal Oxide Semiconductor (CMOS), Digital Signal Processing (DSP), Gate Diffusion Input (GDI), Very Large Scale Integration (VLSI), Exclusive OR gate (XOR).**

I. INTRODUCTION

Advances in CMOS technology have led to a renewed interest in the design of basic functional units for digital systems. The use of integrated circuits in high-performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. This trend is expected to continue, with very important implications for power-efficient VLSI and systems designs.

Digital integrated circuits commonly use CMOS circuits as building blocks. The continuing decrease in feature size of CMOS circuits and corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design. Excessive power dissipation in integrated circuits not only discourages their use in portable environment but also causes overheating which reduces chip life and degrades performance.

Computations in these devices need to be performed using low-power, area efficient circuits operating at greater speed. The design of high-speed and low-power VLSI architectures needs efficient arithmetic processing units, which are optimized for the performance parameters, namely, speed and power consumption.

Addition is one of the widely used fundamental arithmetic operations. In addition to its main task, which is adding two binary numbers, it is the nucleus of many other useful operations such as subtraction, multiplication, and division. Full adder is an essential component for designing all types of processors, namely, digital signal processors (DSP), microprocessors, and so forth. In most of the digital systems adder lies in the critical path that affects the overall speed of the system.

It is very important to choose the adder topology that would yield the desired performance. So enhancing the performance of the 1-bit full adder cell is the main design aspect. One way to achieve digital circuit with low power consumption and less area is GDI technique. Since there is many advancement in VLSI technology and there are many efficient styles of designing VLSI circuits. Some of the styles are CMOS, GDI (Gate Diffusion Input) techniques. GDI technique helps in designing low-power digital combinatorial circuit by which we can eradicate demerits of CMOS technique. This technique allows reducing power consumption and area of digital circuits while maintaining low complexity of logic design. The different methods are compared with respect to the transistor count, and power dissipation are discussed here in this paper showing advantages and drawbacks of GDI compared to CMOS style.

II. DESIGN OF FULL ADDER CELL IN CMOS AND GDI TECHNOLOGY

The full adder operation can be stated as follows. Given the three 1-bit inputs A, B, and Cin, it is

Full Adder Truth Table				
A	B	C_{in}	C_{out}	F
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

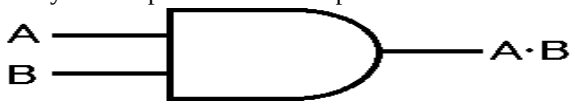
desired to calculate the two 1-bit outputs Sum and Cout, where

Sum = A ⊕ B ⊕ C_{in},

Cout = (A⊕ B)C_{in}+(AB)

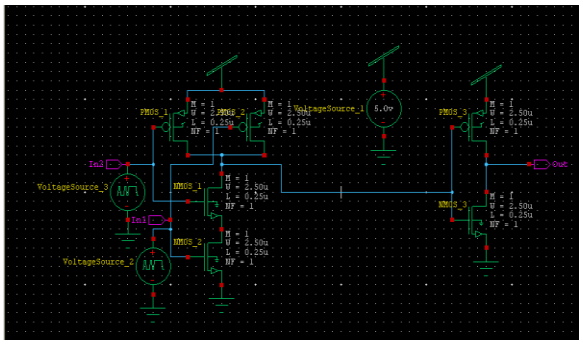
AND GATE:

The AND gate is a basic digital logic gate that implements logical conjunction - it behaves according to the truth table to the right. A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results. In another sense, the function of AND effectively finds the minimum between two binary digits, just as the OR function finds the maximum. Therefore, the output is always 0 except when all the inputs are 1's.

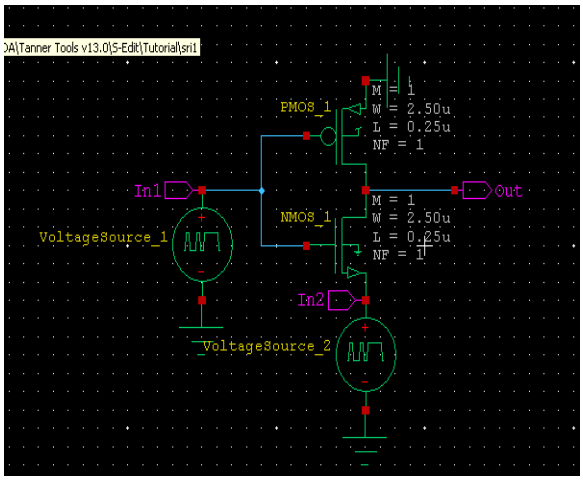


2 INPUT AND GATE		
A	B	F=AB
0	0	0
0	1	0
1	0	0
1	1	1

TRANSISTOR LEVEL CIRCUIT FOR AND GATE INCMOSTECHNOLOGY:

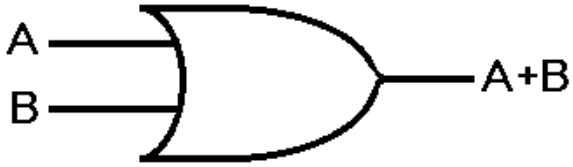


TRANSISTOR LEVEL CIRCUIT FOR AND GATE INGDI:



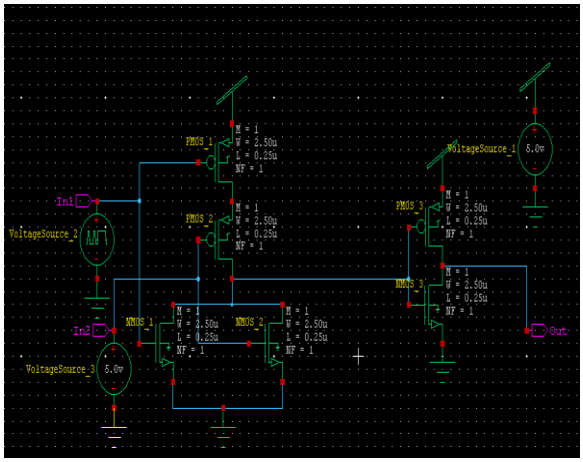
OR GATE:

The OR gate is a digital logic gate that implements logical disjunction - it behaves according to the truth table. A HIGH output (1) results if one or both the inputs to the gate are HIGH (1). If neither input is HIGH, a LOW output (0) results.

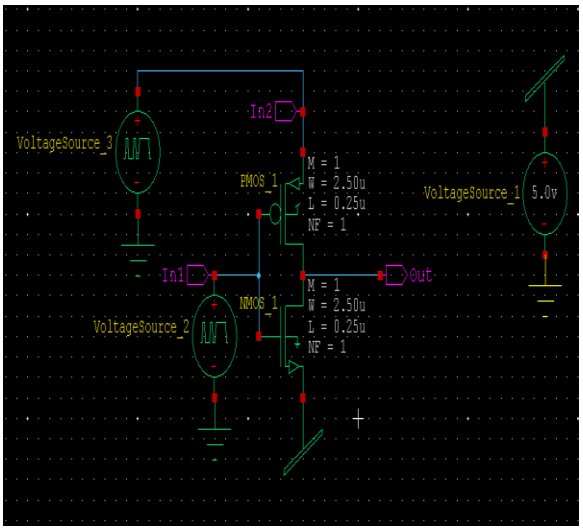


2 INPUT OR GATE		
A	B	F=A+B
0	0	0
0	1	1
1	0	1
1	1	1

TRANSISTOR LEVEL CIRCUIT FOR OR GATE IN CMOSTECHNOLOGY

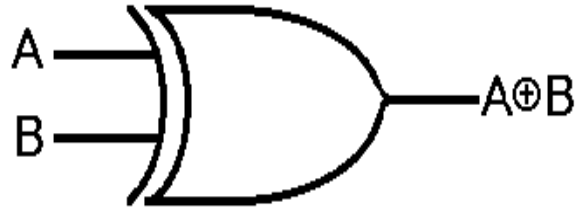


TRANSISTOR LEVEL CIRCUIT FOR OR GATE IN GDITECHNIQUE



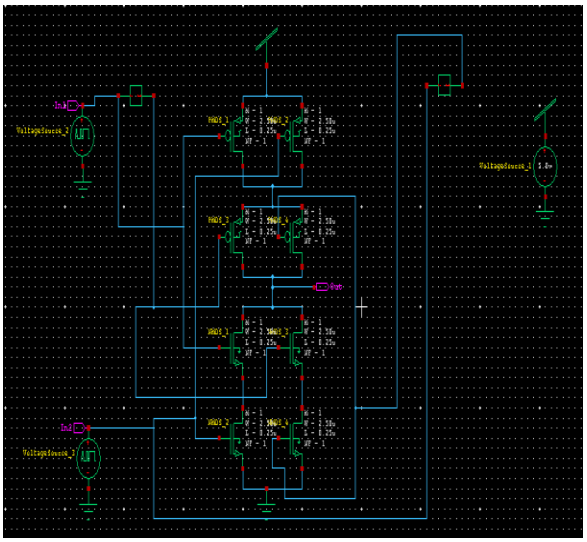
XOR GATE:

The XOR gate (sometimes EOR gate, or EXOR gate) is a digital logic gate that implements an exclusive or; that is, a true output (1/HIGH) results if one, and only one, of the inputs to the gate is true. If both inputs are false (0/LOW) or both are true, a false output results. XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false. A way to remember XOR is "one or the other but not both". XOR can also be viewed as addition modulo 2. As a result, XOR gates are used to implement binary addition in computers. A half adder consists of an XOR gate and an AND gate. The algebraic expressions AB'+A'B and (A+B)*(AB)' both represent the XOR gate with inputs A and B. The behaviour of XOR is summarized in the truth table shown below.

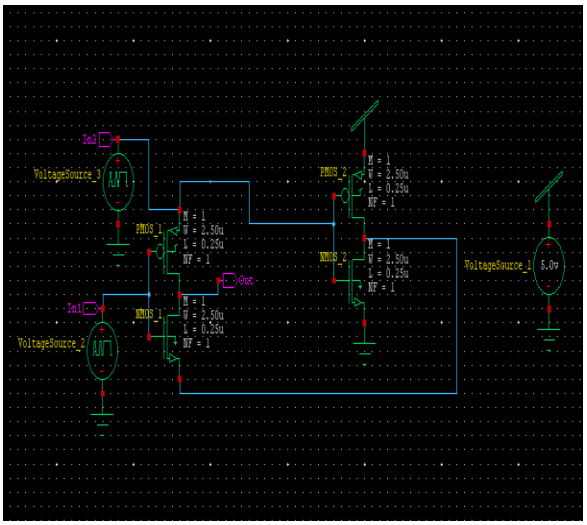


2 INPUT EX-OR GATE		
A	B	F=A^B
0	0	0
0	1	1
1	0	1
1	1	0

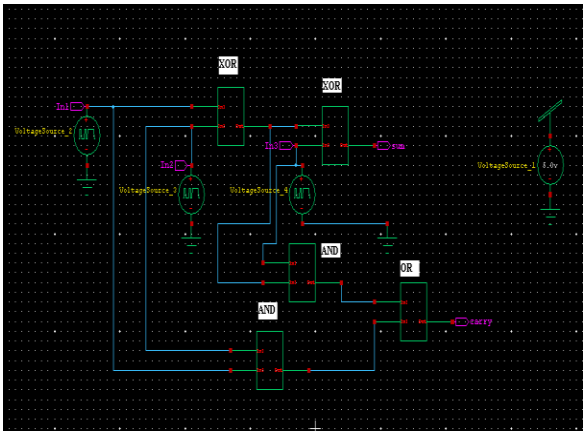
TRANSISTOR LEVEL CIRCUIT FOR XOR GATE IN CMOSTECHNOLOGY



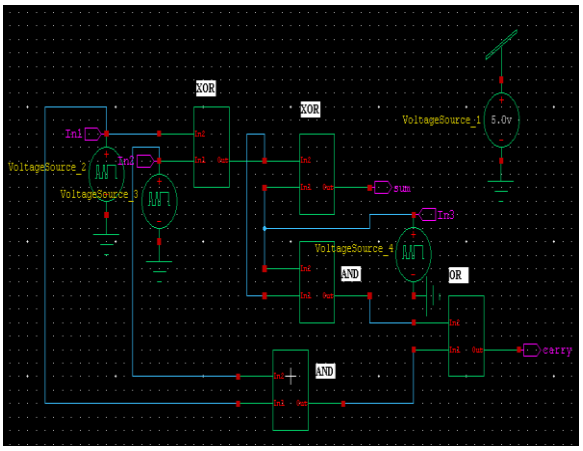
TRANSISTOR LEVEL CIRCUIT FOR XOR GATE IN GDI TECHNOLOGY



TRANSISTOR LEVEL CIRCUIT FOR FULL ADDER IN CMOS TECHNIQUE

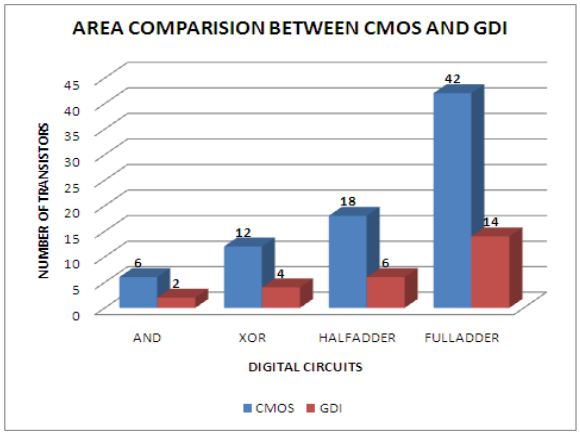


TRANSISTOR LEVEL CIRCUIT FOR FULL ADDER IN GDI TECHNIQUE

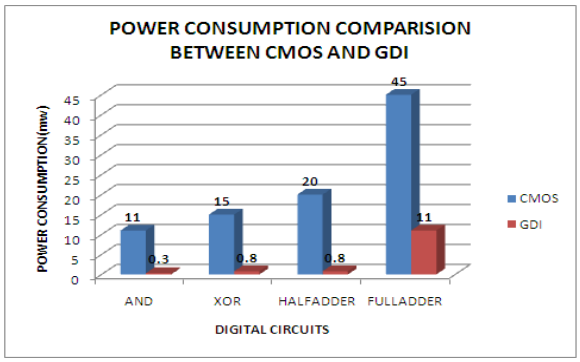


III. COMPARISION BETWEEN CMOS AND GDI TECHNOLOY

AREA COMPARISION BETWEEN CMOS AND GDI TECHNOLOY



POWER COMPARISION BETWEEN CMOS AND GDI TECHNOLOGY:



IV.CONCLUSION

A novel GDI technique for low-power design was presented. Comparisons with existing cmos technique were carried out, showing reduction of power in the test chip in GDI over CMOS and significant improvements in performance. GDI will allow high density of Fabrication as now a day's chip area is very important parameter. The GDI technique allows use of a simple and efficient design algorithm.

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