Efficient Pipelined CORDIC Architecture for Generation of Sine and Cosine Function

Ravi Mogili[1], Raju Katru[2], Kandukuri Shobha[3]
[1,2,3] *Assistant professor, Dept. of ECE, Ashoka Institute of Engineering and Technology, Hyderabad, Telanagana, India*

***Abstract*- In processing the real world data Digital signal processing algorithms provides unbeatable efficiency. One of the DSP algorithms is Coordinate Rotation Digital computer (CORDIC). The beauty of CORDIC lies in the fact that by simple shift-add operations and the CORDIC has gained momentum for decades because of its less hardware complexity. CORDIC algorithm is very simple and iterative process for performing various mathematical computations. Most of the literature lacks in calculation of resources utilized by a particular CORDIC architecture. In this paper, serial, parallel and pipelined CORDIC architecture has been implemented for computing both sine & cosine functions. This paper makes an attempt to survey different forms of CORDIC algorithms and its architectures and applications explore implementation exact to FPGAs and the way the structure has been coded in VERILOG, synthesis evaluation are carried out making use of Xilinx ISim software and targeted on Xilinx FPGA synthesis device.**

***Index Terms*- FPGA, CORDIC Algorithm, Folded & Unfolded Architecture, serial and parallel pipelined CORDIC, sine and cosine functions.**

I. INTRODUCTION

The solutions for the making plans of high-speed VLSIarchitectures for term digital signal processor (DSP) algorithms are mapped from a method intohardware low-cost architectures. With the appearance oflow-cost, low power FPGA's; style of sucharchitectures which would possibly satisfy the overall performancewishes for the signal system programs like 3dimensional (3D) images, video/image/ signalprocess systems have grown to be easy. Many of the DSPalgorithms use the calculation of standard featureslike trigonometric, inverse trigonometric, logarithm,exponential, multiplication, and division features thatneed high process power. The typically used packagesolutions for the digital implementation of thesefunctions are table search technique and polynomialexpansions, requiring an expansion of multiplication andadditions/subtractions. In 1959, Volder [6] hasprojected a unique purpose virtual computing unitreferred to as COordinate Rotation data processor(CORDIC). This formula turned into at first evolved for naturalarithmetic features, exploitation givens rotationredecorate technique. The CORDIC system computessecond rotation exploitation unvaried equations usingshift and add operations which have smooth design andconsume less power. Walther has projected a unifiedthe components to reckon rotation in round, linear, andhyperbolic coordinate systems. The CORDIC componentsperforms severa fundamental functions doable inrotation and vectoring mode of circular, linear, andhyperbolic coordinate structures [3][4]. CORDICthe technique has been utilized in several applications, likesignal system alterations, virtual filters andmatrix based totally computations. Radical lowenergy systems may be with performance evolved viaCORDIC [5] [6].

Large number of iterations is themain drawback which affects the system speed adversely.Many algorithms such as angle recoding (AR) [7], EEAS [8],modified vector rotation (MVR) [9], mixed scaling rotation(MSR) [10], scaling free CORDIC algorithms [11], [12] etc. havebeen proposed to overcome this drawback and to improve thespeed performance of the system. To speed up the system,parallel and pipelined CORDIC are used.In this paper, the concept of rotation and pseudo-rotation [13]has been discussed with the derivation of basic CORDICequations. Normally CORDIC is used in circular rotationmode due to simplicity. The mode of CORDIC, eithervectoring mode or rotational mode, is selected according tothe requirement. Till

now, some CORDIC based digital circuitsas well as processors have been designed. CORDIC basedcomplex multiplier has been discussed in [14] and suchmultiplier can be used in designing of digital filters withreduced power consumption.

II. LITERATURE SURVEY

Sine and Cosine waves have been used in countless applications; in recent research on Software Defined Radio (SDR), digital modalities of sine and cosine waves have received special attention. SDR involves highly reconfigurable resources and uses digital generated waves for modulation and demodulation of signals. Coordinate Rotation Digital Computer (CORDIC) is a well known algorithm used to approximate iteratively some transcendental functions. Arias et.al [15] presented a pipelined CORDIC architecture which is used for designing a flexible and scalable digital sine and cosine waves generator.

A scale factor compensation inherent to the CORDIC algorithm becomes an important drawback when trying to improve its benefits, although some authors have come up with a new scaling-free version, which has been successfully implemented within wireless applications. However, this new CORDIC can still be significantly improved by modifying some of its parts, therefore, Zapata et.al [16] showed an enhanced version of the scaling-free CORDIC. These new enhancements have been obtained some new architecture which are able to reach a 35% lower latency and a 36% reduction in area and power consumption compared to the original scaling-free architecture.

In conventional CORDIC algorithm, multiplier and a lookup table are needed to achieve calculation of multiple transcendental functions, which will lead to hardware circuit complexity and lower operation speed. Aim at overcoming the shortcomings of traditional CORDIC algorithm, a modified CORDIC algorithm was proposed by Xin et.al [17]. The method does not need the module of correction factor and the lookup table, and just needs a simple shift and add-subtract to achieve the calculation of multiple transcendental function. So it can reduce hardware costs and improve operational performance.

Many hardware efficient algorithms exists for hardware signal processing architecture. Among these algorithm is a set of shift-add algorithms collectively known as CORDIC (COrdinate Rotation for Digital Computers) for computing a wide range of functions including certain trigonometric, hyperbolic, linear and logarithmic functions. Sinith et.al [18] compared the different CORDIC architectures with respect to their area, speed, and data throughput performance especially in three different major styles iterative, parallel and pipelined structures.

Khare et.al [19] presented an area-time efficient CORDIC algorithm that completely eliminates the scale-factor. By suitable selection of the order of approximation of Taylor series the proposed CORDIC circuit meets the accuracy requirement, and attains the desired range of convergence. Besides they have proposed an algorithm to redefine the elementary angles for reducing the number of CORDIC iterations. The proposed CORDIC processor provides the flexibility to manipulate the number of iterations depending on the accuracy, area and latency requirements. A scale factor compensation inherent to the CORDIC algorithm becomes an important drawback when trying to improve its benefits, although some authors have come up with a new scaling-free version, which has been successfully implemented within wireless applications.

III. PROPOSED FRAMEWORK

CORDIC can be used to compute Sin of any angle θ with little variation. The angle is given as input. A vector length 1.647 (CORDIC gain) along the x-axis is taken. The vector is then rotated in steps so as to reach the desired input angle θ . The x and y values are accumulated. After fixed number of iterations the final co- ordinates of the vector i.e. the x and y values give value of cosine and sine respectively of the given angle θ . When the Sine or Cosine functional configuration is selected, the unit vector is rotated, using the CORDIC algorithm, by input angle θ This generates the output vector of $(\cos(\theta), \sin(\theta))$ .The compensation scaling module is disabled for the Sinθ and Cosθ functional configuration as it is internally pre-scaled to compensate for the CORDIC scale factor.

CORDIC architectures are commonly categorized into sequential (folded) and combinational (unfolded) depend on hardware realization of iterative equations.

The folded architecture is obtained by the direct duplication . In time domain the sequential architecture has to be multiplexed so that all iterations are approved in a particular functional unit. The signal processing architectures delivers a means for operating area for speed. Using a word sequential design the folded architecture is implemented the unabridged CORDIC core.

A. Folded Word Sequential Design

Folded word sequential design [1] is duplicated by using three difference equations in each. This is also called as iterative bit-parallel design, the hardware as shown in Fig.1. Each block contains a shift unit, subtraction-adder unit block, and one register used for output buffering. Initial values are given to register by the multiplexer for first level calculation.

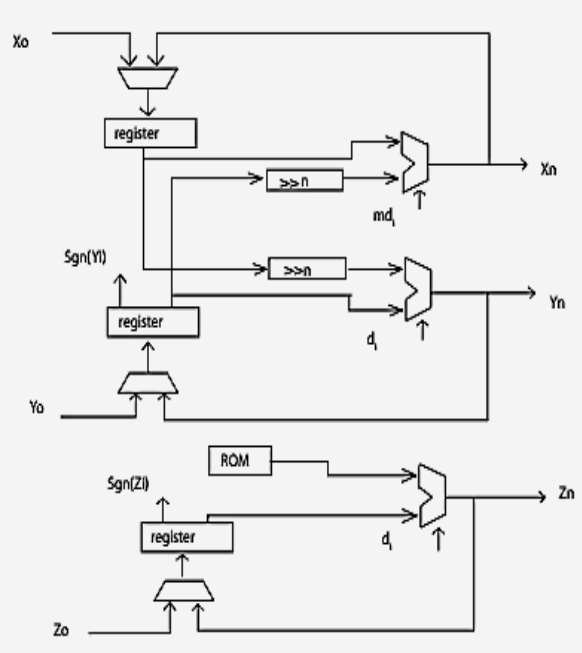

Fig.1 Folded word sequential design.

Here z-branch of MSB stored value determines the operation mode for the adder-subtraction unit x and y outlet Signals passes to block of shift unit and finally subtracted or added to un-shifted signal value in reverse path. The z branch mathematically mixing the registers values, lookup table passes these values, then each number of operations the address value is changed. After n operations output is passes again to register block before primary values are fed in again and these final value can be access as output. Normal FSM needs to control the addressing of the constant values and multiplexers. All the initial values are given hardwired in a word wide manner when it is implemented in FPGA. Both subtracted and adder component are passed out separately. Angle accumulator controls the multiplexer. Routing signals are required to find distinguish between subtraction and addition. For varying the shift distance value, shift operations are used. Shifters are not suitable for FPGA architectures because it desires several layers of logic. Due to numerous layers of logic cells, the resultant design structure will become slow.

Unfolded Parallel Architecture

The CORDIC processor discussed above is iterative algorithm, it means processor needs to perform n iterations at the given data rate. This is an unfolded operation [2], it means always performs the same iteration at n times processing elements. It shows in Fig.2 will result the value in two simplifcations. First one is fixed shifts at shifters; by using wiring we can implement it.

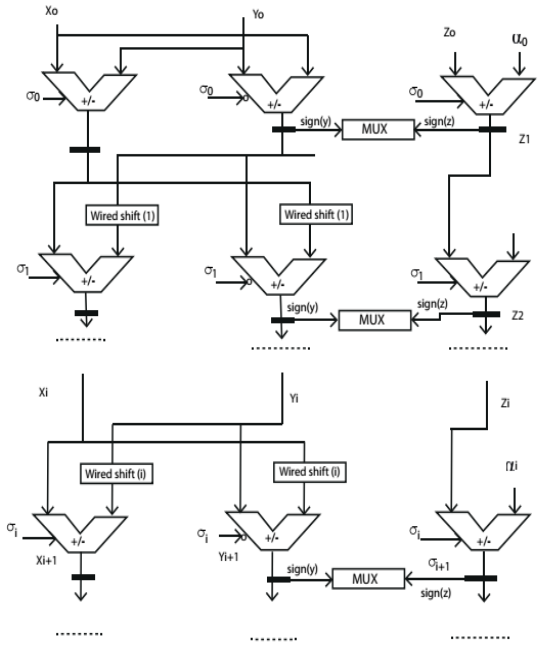

Fig.2. Unfolded parallel architecture.

Another one based on lookup table. Here angle accumulator distributed the LUT values, as constants to each adder; this is chain process in accumulator angle. Instead of using storage space we are moving to constants, which are hardwired. The whole CORDIC processor can be modified into grouping of subtraction-adder unit in interconnected manner. Now we do not require registers, building of this unrolled processor stringently combinatorial. Finally resulting circuit delay should be substantial; now

processing time is decreased compare to iterative circuit. Mostly and particularly in FPGA, they do not make any sense of using combinatorial large circuit what we required. The design of unrolled processor can be easily pipelined by inserting registers in-between the subtraction- adder unit block. Moreover FPGAs already contain registers in each logic cell, so this pipelined registers do not increase the hardware cost.

IV. RESULTS AND DISCUSSION

The implementation in this work is targeted FPGAfamilies viz. Spartan-6 .The implementation is carriedout for associate input quantity length varying from 16bits. The style synthesis, mapping, translation andsimulation are applied in Xilinx ISE 14.5. Thetrigonometric function uses simple pipelinedarchitecture using CORDIC processor. The CORDIC isoperated in rotating mode, hence only angle is given asinput and x, y values are given in the program .As thisarchitecture inputs can be given at every clock pulseand the value for inputs will output after eight clockcycle as it.

As it is discovered, that CORDIC processors are going toamplify their existence within the future excessive overall performance.This results in decrease scalability. Since the algorithmincludes handiest upload and shift operations, it has superbhardware performance and a very minimum manageoverhead. The realization of this paper will resolve mostof the difficulties discussed above and in the hassledefinition segment. This paper can have followingconsequences

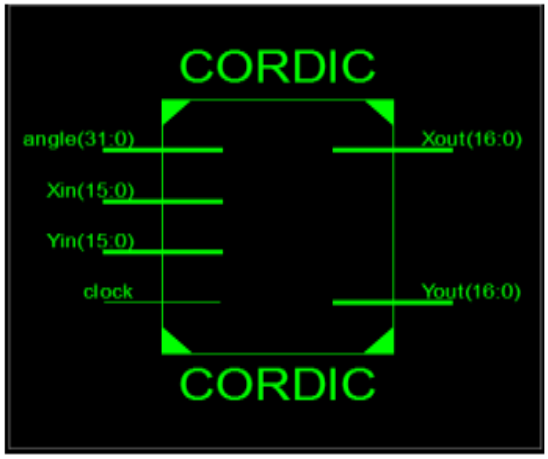

Fig.3 RTL Schematic of CORDIC Processor

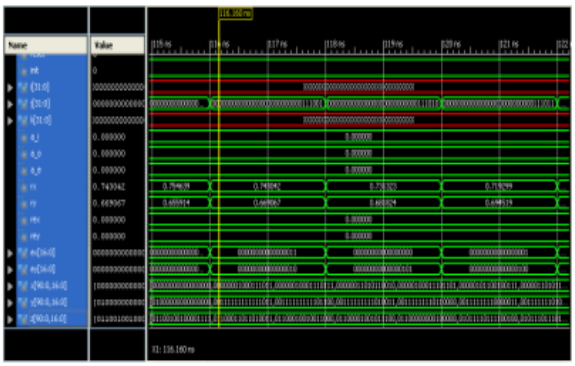

Fig.4 Simulation of sine – cosinewaveform CORDIC Processor

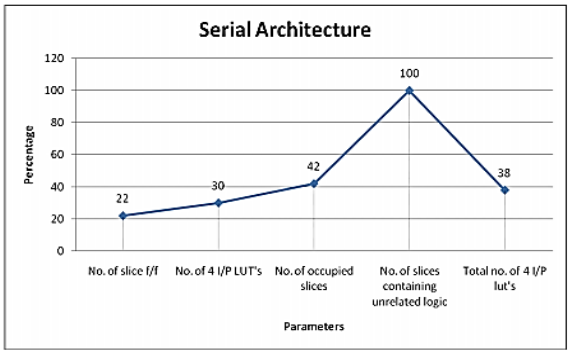

Fig.5 Resource Utilization of Sin and Cos functional Configuration in serial architecture

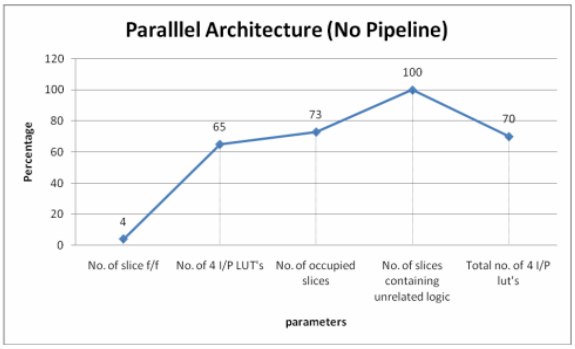

Fig.6 Resource Utilization of Sin and Cos functional Configuration in parallel architecture

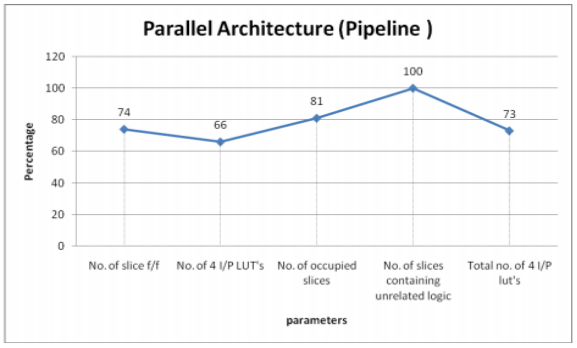

Fig.7 Resource Utilization of Sin and Cos functional Configuration in parallel architecture

From Figures 5-7, it has been concluded parallel architecture uses 74% no. of slices ascompare to 4% no. of slices used by parallel architecture without pipelining mode and 22% no. of slices used byserial architecture. 66% no. of 4 input LUTs used by parallel architecture with pipeline mode but 65% no. of 4input LUTs are used by parallel architecture without pipelining and 30% no. of 4 input LUTs are used by serialarchitecture. 81% and 73% occupied slices are used by parallel architecture with or without pipeliningcontinuously and 42% occupied slices are used by serial architecture.

V. CONCLUSION

This paper presents a comprehensive survey on different architectures for CORDIC, mainly in substantial operand of DSP and high speed applications, the above architectures can be used. From the directly above conversation, although parallel architecture with pipeline give the impression to be costlier as compareto parallel without pipelining and serial architecture, yet parallel architecture has high throughput (i.e. speed) ascompare to serial architecture.

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