Optimization of Full adder cells Using HDL

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***Abstract*- Power consumption has emerged as a primary design constraint for integrated circuits (ICs). In the Nanometer technology regime, leakage power has become a major component of total power [1]. Full adder is the basic functional unit of an ALU. The power consumption of a processor is lowered by lowering the power consumption of an ALU, and the power consumption of an ALU can be lowered by lowering the power consumption of Full adder. So the full adder designs with low power characteristics are becoming more popular these days. In this paper we are going to design four different types of Full adder these are applied to 32-bit RCA .The four designs will be developed using Verilog HDL.**

***Index Terms*- Adder, Low power, Multiplexer, RCA adder**

I. INTRODUCTION

The core of every micro-processor, electronic indication processer (DSP), and information systems application like specific incorporated routine (ASIC) is its information direction. At the heart of data-path and dealing with models in turn are mathematics models, such as comparators, adders, and multipliers. Finally, the primary function found in most mathematics elements is the binary inclusion. A calculations needs to be performed using low-energy, area-efficient circuits operating at greater speed. Addition is the most primary mathematics function complete adder routine is efficient foundation and most critical component of complicated mathematics circuits like micro-processors, electronic indication processer chips or any ALUs. Almost every complicated computational routine requires full adder circuits. The entire computational prevent energy intake can Be reduced by applying low energy techniques on full adder circuits. Several full adder circuits have been suggested focusing on design accessories such as energy, delay and place. Among those styles with less transistor count using pass transistor reasoning have been widely used to reduce energy intake. Regardless of the routine convenience, these styles suffer from severe outcome indication deterioration and cannot maintain low volts functions. In this document we existing an exploratory research of Swell Carry Adder components applied in the 180-nm procedure and examined for efficiency, energy, mobile place, and structure place and delay modifications. The adders chosen for this research involved in Regular adder, XNOR and MUX adder, NAND adder, and MUX adder. Each of the adders was categorized according to the reasoning operate noticed. Using this strategy we have provided a research of the possible effect of reasoning operate option and not just routine option on the efficiency of the ultimate adder. These different adder features were also noticed using the lately suggested Swell Carry Adder (RCA). Swell Carry Adder is designed by flowing complete adder prevents in sequence, The carryout one level is fed straight to the carry-in of the next level, For a N-bit RCA needs N-Full adders. The research provided here is designed to emphasize the effects of using a particular complete adder reasoning operate, routine topology, and interfacing design before selecting one for mathematics program implementation.

II. PROPOSED SCHEMATIC

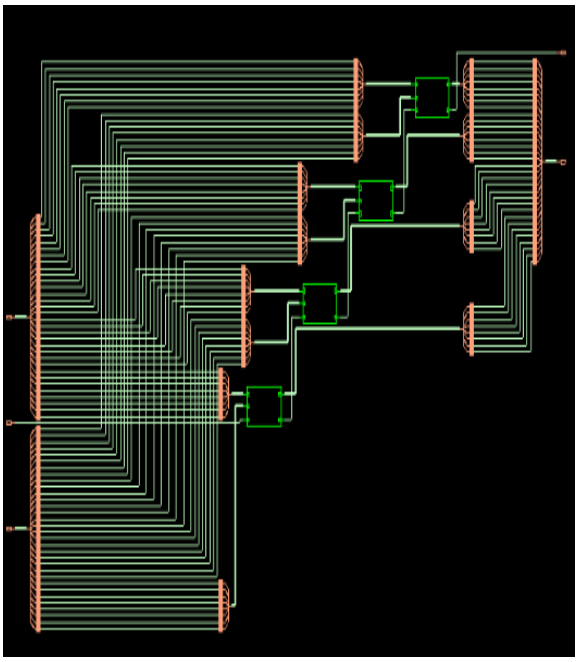

Fig.1 32-Bit Ripple carry adder.
Leakage Power: 8.24 NW
Dynamic Power: 281163.013 NW
Total Power: 281171.259 NW

Inclusion is a essential operate for any electronic program, electronic indication handling or management program. A quick and precise operate of a electronic program is significantly affected by the efficiency of the citizen adders because of their comprehensive use in other primary electronic functions such as subtraction, multiplication and department. The traditional reasoning formula for Sum and Carry: Sum = C ex-or (A ex-or B) Carry = (A and B) or C(A ex-or B) In RCA, the CARRY bit ripples all the way from first level to nth level. The delay in a RCA relies on the variety of levels cascaded and also the feedback bits' styles. In the feedback styles, a CARRY is neither produced nor spread. However, certain feedback styles produce carry bit in the first level itself, which have to swell through all the levels. This might improves the delay in the routine. The reproduction delay of such a situation, also known as crucial direction, is known as worst-case delay over all possible feedback styles. In a swell carry adder, the worst-case delay happens when a carry bit develops all the way from least essential bit (LSB) place to most essential bit place (MSB). The complete delay of the adder will be an addition of delay of a SUM bit and delay of a CARRY bit increased by variety of pieces less one in the feedback term. R adder = (N-1) R carry + R sum Where N is variety of pieces in feedback term, R carry and R sum are reproduction setbacks from one level to another. For an effective swell carry adder, it is essential decrease R carry than R amounts as the former impacts the complete adder delay more. In this style, it is must to be applied that the complete adder's style is done using MIFG CMOS gadgets Usually the SUM bit of a complete adder includes developing of XOR gateways to recognize its operate and in the same way CARRY bit needs AND gateways to recognize its Boolean appearance.

III. PROPOSED RIPPLE CARRY ADDER

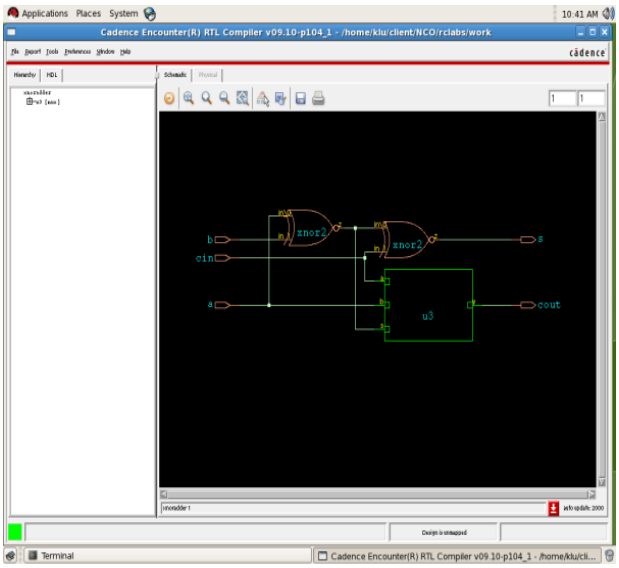

Fig.2 Logic diagram of Full Adder Using XNOR and MUX
Leakage Power: 5.416 NW
Dynamic Power: 74612.477 NW
Total Power: 74617 .894 NW

His execution of XOR and XNOR of A and B is done using successfully pass transistor reasoning and an inverter is to supplement the feedback indication A. This execution results in quicker XOR and XNOR results and also guarantees that there is a balance of setbacks at the outcome of these gateways. This results in less unwarranted SUM and Carry alerts (Fig 2). The energy recuperating reasoning reuses cost and therefore takes in less energy than non-energy recuperating reasoning. In non-energy restoration style the cost used to the fill capacitance during the reasoning stage high is cleared to floor during reasoning stage low. It should be mentioned

that the new XNOR and MUX adder has no immediate direction to the floor. The removal of a direction to floor decreases energy intake, eliminating the short routine from the energy formula. The cost saved at the fill capacitance is reapplied to the management gateways, the mixture of not having a immediate direction to floor and re-application of the fill cost to the management checkpoint makes the energy – recuperating full adder an energy effective style but it has the limit loss problem. In this style needs less check point depend and less variety of transistors, so the style needs less storage.

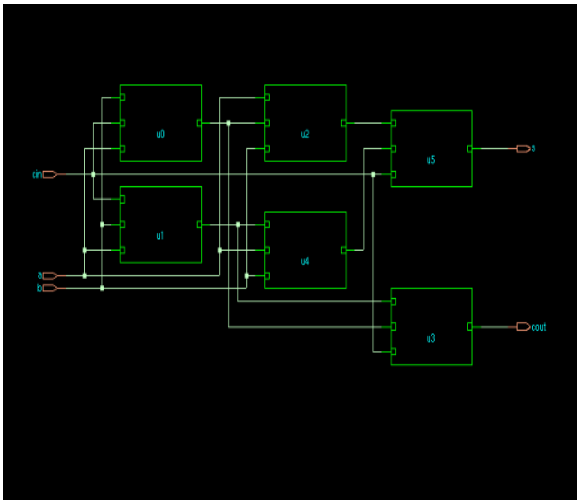

Fig.3 Logic diagram of Full Adder Using MUX
Leakage Power: 44.742 NW
Dynamic Power: 306159.401 NW
Total Power: 306204.143 NW

A 1-bit complete adder designed up on SIX similar multiplexers gateways is proven in fig.3.substituing each of the multiplexer gateways with a 2-transistor routine. There are three significant resources of energy dissipation in CMOS circuits: reasoning conversion, short-circuit present and leak present. The short-circuit present is the dc moving through the provide and the floor, when both the NMOS and the PMOS transistors are simultaneously effective. As the style MUX-12T adder does not have immediate relationships to VDD or VSS slot the prospect of a immediate direction development from beneficial volts provide to the floor during changing can be considerably reduced; that is, the energy intake due to brief routine present is regarded negligibly little. Furthermore, in the new MUX-12T adder, all of its inner checkpoint nodes are straight thrilled by the clean feedback alerts (A, B, and Cin), resulting in a much quicker conversion (low go up and down times) in its outcome alerts. Consequently, the energyintake of the following shield level can advantage from faster/cleaner Sum and Count results. In this style need more variety of transistors so the style enquire storage is more , The efficiency of the complete adder is need more time.

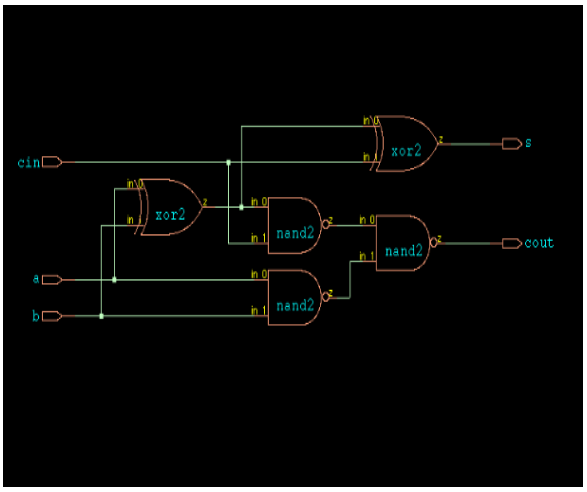

Fig.4 Logic diagram of Full Adder Using NAND.
Leakage Power: 15.968 NW
Dynamic Power: 189580.838 NW
Total Power: 189596.806 NW

One disadvantage of Regular adder style is that it uses three different kinds of gateways, demanding three different IC offers, even though there are only five gateways. You can upgrade the routine to substitute all the AND and OR gateways by NAND gateways. Then we will need only two IC offers to apply the routine.

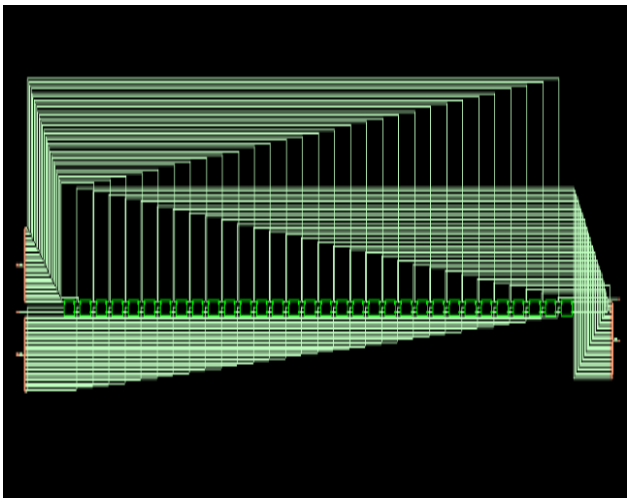

Fig.5 Proposed 32-Bit Ripple carry adder.

TABLE 1
Comparison of the RCA Power Variations in 180nm Technology

RCA Adder	Leakage Power (nw)	Dynamic Power (nw)	Total Power (nw)
Normal Adder	16.56	251601.0	251618.494
XNOR & MUX Adder	5.416	74612.477	74617.894
NAND Adder	15.968	189580.838	189596.806
MUX Adder	44.742	30615.401	306204.143

IV. WAVEFORMS AND RESULTS

Fig.6 Waveforms of RCA

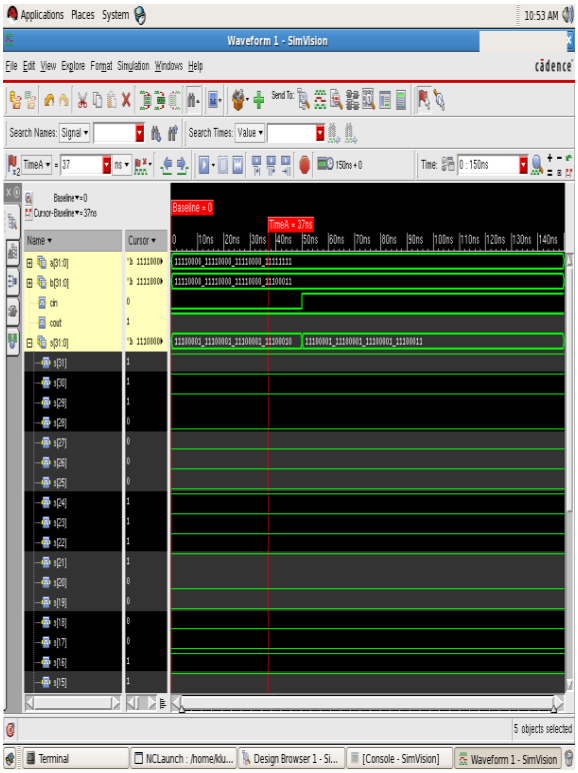

Fig.7 Waveforms of RCA

TABLE 2

Comparison of the RCA Variations in 180nm

Adder Type	Power(NW)	Delay(Ps)	P.D.P(10^{-12}W-S)
Basic ADDER	251618.494	6454	1.62
XNOR&MUX ADDER	142779.190	6826	0.94
NAND ADDER	189596.806	4707	0.89
MUX ADDER	306204.143	14463	4.42

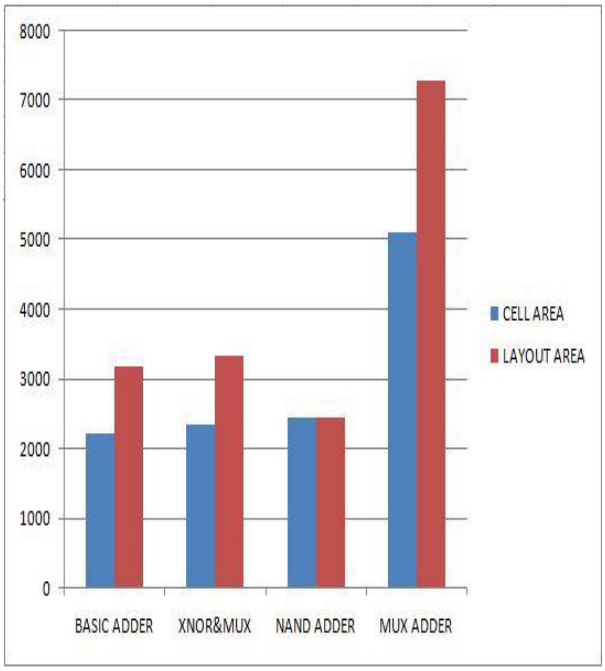

Fig.8 Comparison of power and Delay of RCA

V. CONCLUSION

The paper can be very useful for variousdigital circuitry and it reduces the design time of the digital circuits this can be used in various security machines this can be integrated immediately to any device that needs the clock signal of the particular frequency by using cadence 180nm technology the layout has been generated and which is the best and the optimized one obtained from the optimized net-list this can be used in applications such as ALU.

Four new Ripple Carry Adder designs have been proposed and simulation results have been compared with the previous results.

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