Parallel CMOS Implementation of NOR Logic in both Pull-Up and Pull-Down Networks

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***Abstract*- Aware to that the implementation of CMOS logic based on NAND and NOR logic principles of pull-up and pull-down combination of transistors, this work shows how by using both the combinations of pull-up and pull-down transistors in parallel too we can realize a NOR logic. This is illustrated with the help of using DSCH software.**

***Index Terms*-** CMOS, **NOR, Pull-up, Pull-down, Parallel and DSCH software.**

I. INTRODUCTION

The CMOS designing/ design constitute a pull-up and a pull-down network with:

1. Pull-up network having only PMOS transistors
2. Pull-down network having only NMOS transistors.

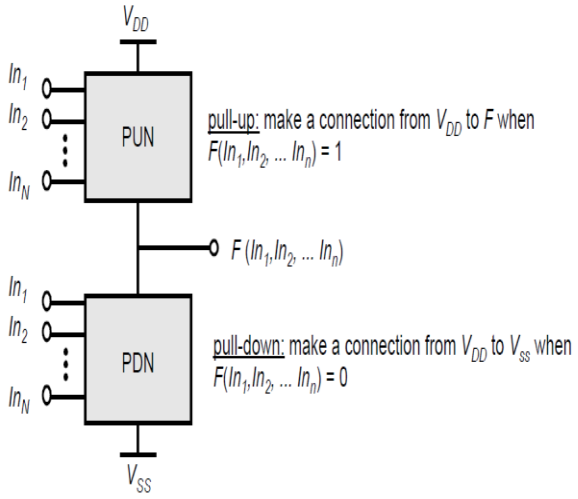

Fig. 1.0 - Pull-up and Pull-down network

These fundamental approach works basically on two logics i.e. NAND and NOR logic,

For NAND Logic	For NOR Logic
PUN-PMOS transistors - Parallel Connection	PUN-PMOS transistors - Series Connection
PDN-NMOS transistors - Series Connection	PDN-NMOS transistors - Parallel Connection

Table. 1.0 – NAND and NOR Combination Logic

Here a two input NOR logic is been implemented and analyzed as with respect to parallel combination of the transistors in both pull-up and pull-down networks using DSCH software.

II. BASIC NOR LOGIC PULL-UP AND PULL-DOWN NETWORKS

A. A basic NOR logic as per the CMOS design topology follows:

- PUN- PMOS transistors- series Connection
- PDN- NMOS transistors-Parallel Connection

$NOR\ FUNCTION\ (F = \overline{A+B})$

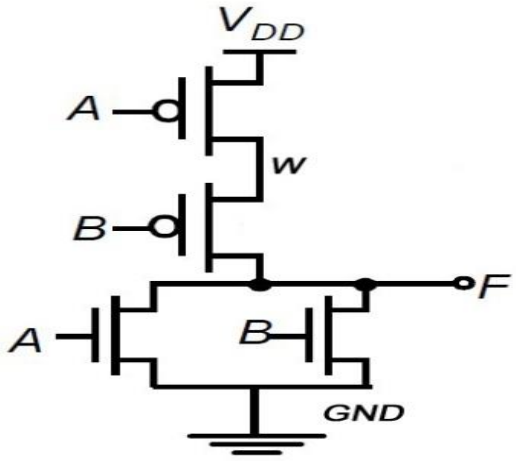

Fig. 2.0 – Two input CMOS based NOR Gate

Input A	Input B	Output F
0	0	1
0	1	0
1	0	0
1	1	0

Table. 2.0 – Truth Table of Two input CMOS based NOR Gate

The basic NOR logic verifies the NOR truth table. Implementing the basic NOR logic using DSCH software, it is observed to the conclusive verification of the NOR logic.

- Pull-up and pull-down arrangement.

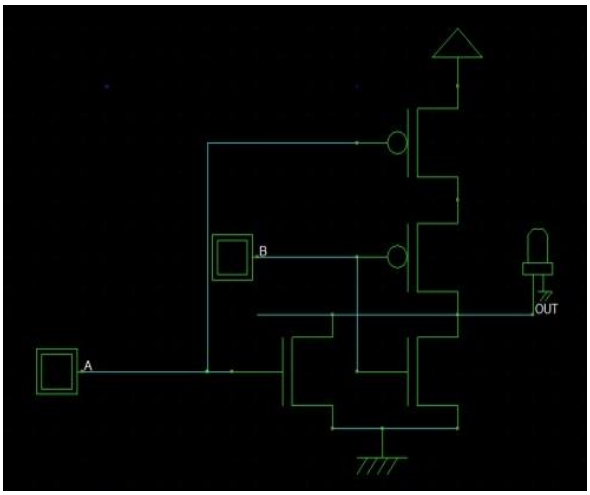

Fig. 2.1

Verifying the logical combinations/inputs,

- A=0, B=0 and OUT=1

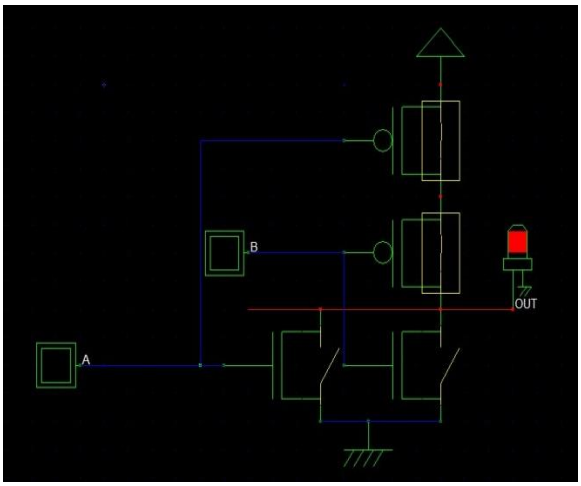

Fig. 2.2

- A=0, B=1 and OUT=0

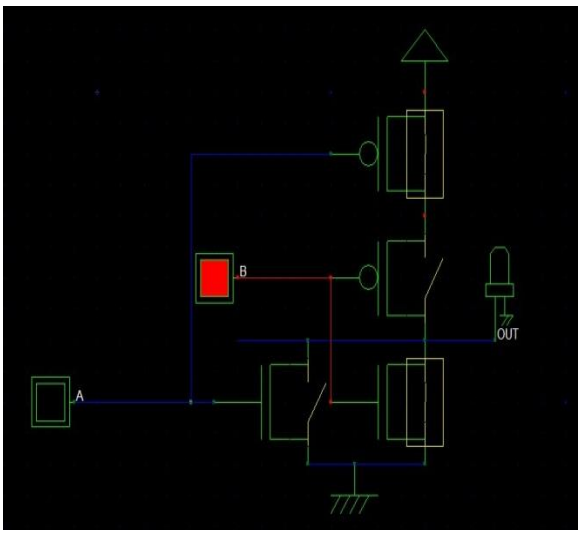

Fig. 2.3

- A=1, B=0 and OUT=0

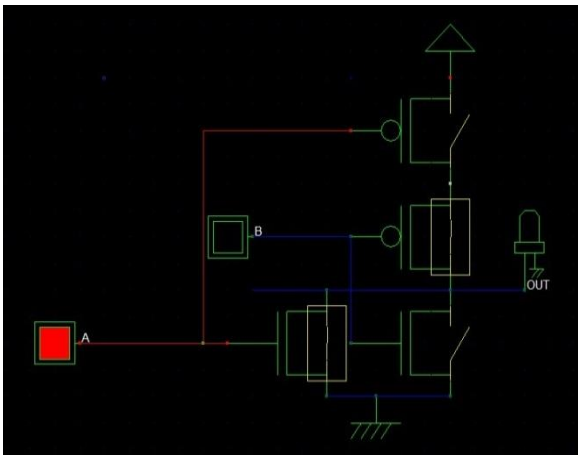

Fig. 2.4

- A=1, B=1 and OUT=0

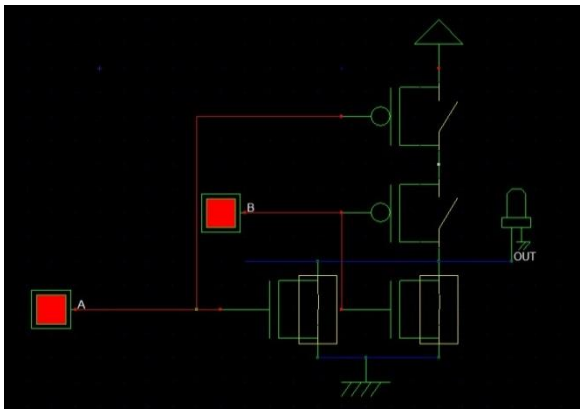

Fig. 2.5

III.PARALLEL COMBINATIONS OF TRANSISTORS IN PULL-UP AND PULL - DOWN NETWORKS FOR NOR LOGIC

Analyzing the NOR logic with parallel implementation in both Pull-up and pull-down networks.

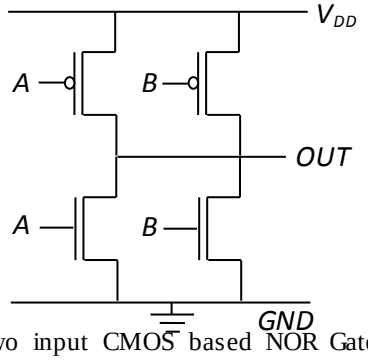

Fig. 3.0 Two input CMOS based NOR Gate using Parallel transistors combination

The conclusiveness obtained after verifying it on DSCH software are:

- Parallel Pull-up and pull-down arrangement.

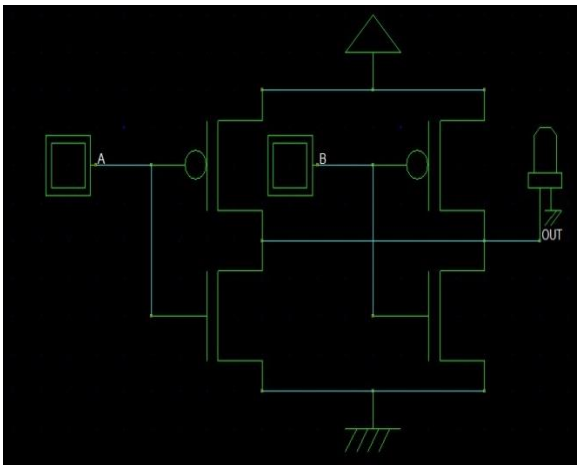

Fig. 3.1

Verifying the logical combinations/inputs,

- A=0, B=0 and OUT=1

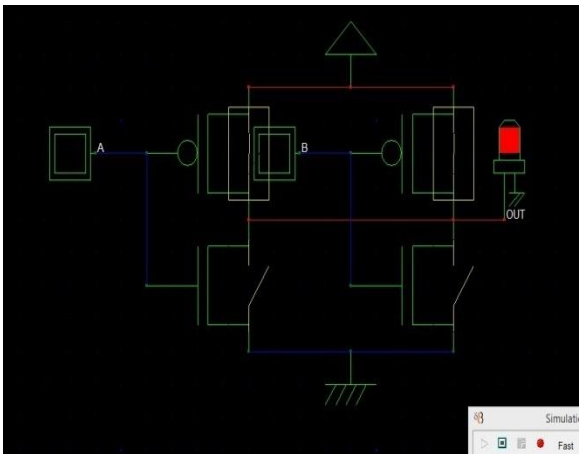

Fig. 3.2

- A=0, B=1 and OUT=0

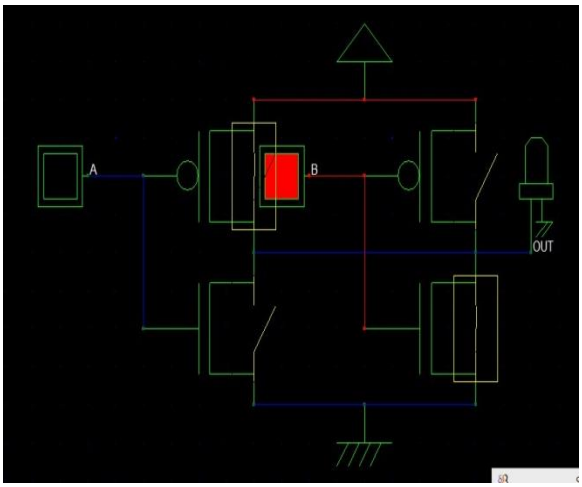

Fig. 3.3

- A=1, B=0 and OUT=0

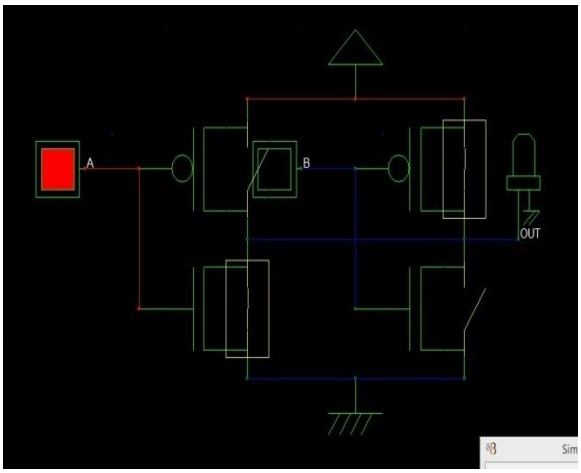

Fig. 3.4

- A=1, B=1 and OUT=0

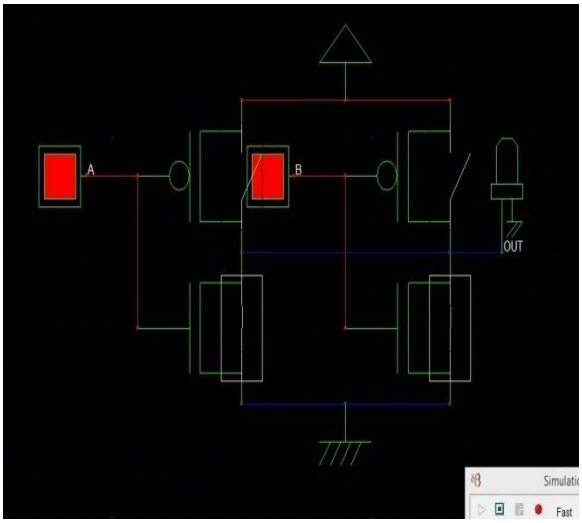

Fig. 3.5

IV. OBSERVATION/ ANAYLSIS ON DSCH CAD

The implementation of the NOR logic as done using DSCH software is been conclusively verifying all the possible logical combinations. The observation obtained is same for the fundamental/ basic CMOS design topology and for the parallel transistors implementation in both pull-up and pull-down networks.

V. FUTURE SCOPE

Such logic implementations may be futuristic for developments of different digital logic circuits and motivate towards the existence of further different network combinations.

VI. CONCLUSION

It can be concluded that a CMOS NOR logic can be implemented by using the Pull-up PMOS transistors in parallel along with Pull-down NMOS transistors in parallel.

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