A Survey and control of multilevel Topologies and Their Modulation technics

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***Abstract*- Recently multilevel inverter technology has widely used in the area of high-power medium-voltage energy control. This paper presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multi cell with separate dc sources. Recent topologies like hybrid inverter are also discussed. This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulse width modulation, multilevel selective harmonic elimination, and space-vector modulation. In this paper some inverters are provided with their simulation model. From the simulation models the quality of outputs can be judge which is improved.**

***Index Terms*- Cascaded multilevel inverter; Neutral point clamped multilevel inverter (NPC); Selective harmonic elimination (SHE).**

I. INTRODUCTION

In recent years industry demands for the higher power equipment, which is in the range of the megawatt level. The controlled ac drives in the megawatt range are usually con nected to the medium-voltage network. Now a days the connection of single power semiconductor switch directly to medium- voltage grids is not possible easily. Hence to overcome this drawback new family of multilevel inverters has used as the solution for working with higher voltage levels [1]–[3]. There are three different types of multilevel inverters as follows: diode-clamped (neutral-clamped) [4]; capacitor-clamped (flying capacitors) [1], [5], [6]; and cascaded multicell with separate dc sources [1], [7]–[9]. In addition to this several modulation and control strategies have been developed or adopted for multilevel inverters including the following: multilevel sinusoidal pulse width modulation (PWM), multilevel selective harmonic elimination, and space-vector modulation (SVM).The previous search results show that multilevel inverter circuits have been introduced around for more than 25 years. An early researches appeared in 1975 [9], the cascade inverter was first introduced with a format that connects separately dc-sourced full-bridge cells in series to synthesize a staircase ac output voltage. Through manipulation of the cascade inverter, with diodes blocking the sources, the diode-clamped multilevel inverter was then derived [10]. The diode-clamped inverter was also called the neutral-point clamped (NPC) inverter when it was first used in a three-level inverter in which the mid-voltage level was defined as the neutral point. Because the NPC inverter effectively doubles the device voltage level without requiring precise voltage matching, the circuit topology prevailed in the 1980s. The application of the NPC inverter and its extension to multilevel converter was found in [11]. Although the cascade inverter was invented earlier, its applications did not prevail until the mid–1990s. Due to the great demand of medium-voltage high-power inverters, the cascade inverter has drawn tremendous interest ever since. Today multilevel inverter is extensively used for high power medium voltage inverter. The field applications include use in laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on.

II. NPC-SHE TOPOLOGY

A. *Modeling And Simulation Design Of NPC/SHE Topology*

In the hybrid converter, the main purpose of NPC inverter is to provide active power flow. The high-power medium voltage NPC due to their lower losses and higher voltage blocking capability [12], [13],

[14], imposing a restriction on the switching frequency. In this work, an NPC is considered operating at a low switching frequency (of 250Hz) where in contrast, the H-bridges are rated at a lower voltage and need to be commutated at a higher frequency for an effective active filtering effect. The NPC inverter is, modulated by using Selective Harmonic Elimination (SHE).This method has the advantage of very low switching frequency and hence low switching losses, while eliminating the low order harmonics. The output voltage of NPC converter is synthesized by using SHE modulation and thus the series HBs will be used only to supply reactive power, allowing for operation with floating capacitor DC-links.

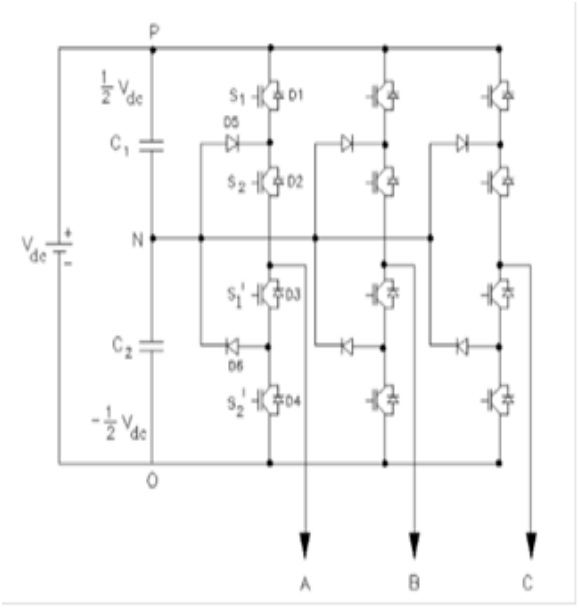

Fig.1.Neutral Point Clamped 3 level multilevel inverter

NPC type Multilevel inverters plays vital role in the field of power electronics and being extensively used in various industrial and commercial applications because it possess low electromagnetic interference and the efficiency is considerably high. NPC Multilevel inverters have become more favoured over the years in electric high power application with the affirmation of less disturbances and the contingency to operate at lower switching frequencies than typical two-level inverters This multilevel inverter will also be compared with two-level inverter in simulations to investigate the advantages of using multilevel inverters. It is observed that NPC multilevel inverter produce only 22% and 32% voltage THD whereas the two-level inverter for the same test produces 115% voltage THD. For other simulation, while practising lower switching frequency, it is observed that when the two-level inverter develops 25W.Switching losses, the experimented multilevel inverters only produce 2.1W and 2.2W switching losses.

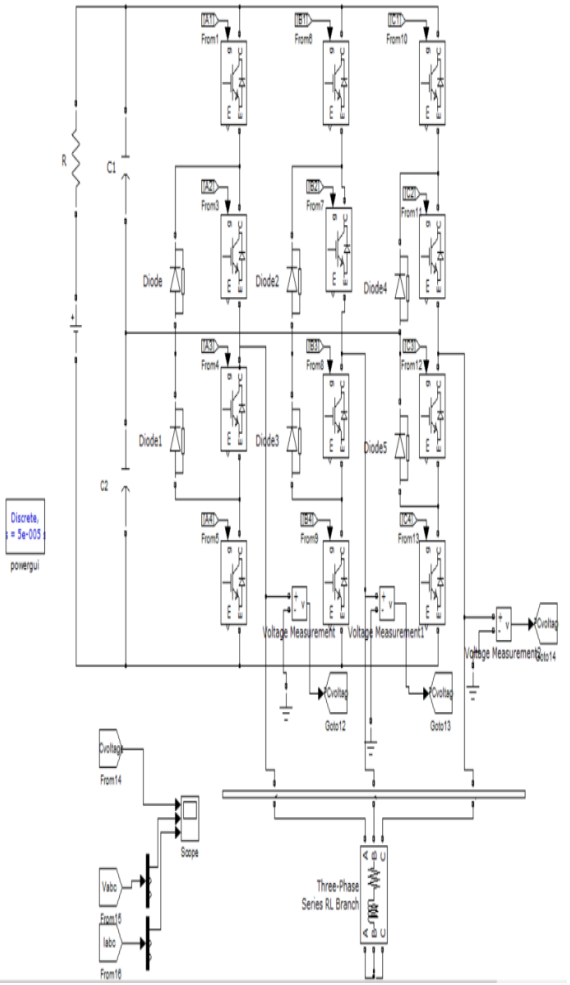

Fig-2 Simulink model for 3 level NPC

The simulation model is shown in the figure below. The implementation of 3 phase Neutral Point Clamped Multilevel inverter in MATLAB software is done. In this model IGBT is used as switching device opt isolator is used to give gate pulse to the thyristor. The output voltage is taken between line to line and phase to phase. The output current and voltage waveform is shown in the figure. A common neutral point is taken outside. The resistance is connected in series with the V_{dc} to obtain constant voltage for the switching. The gate pulse is obtained from closed current loop as shown in fig.2.

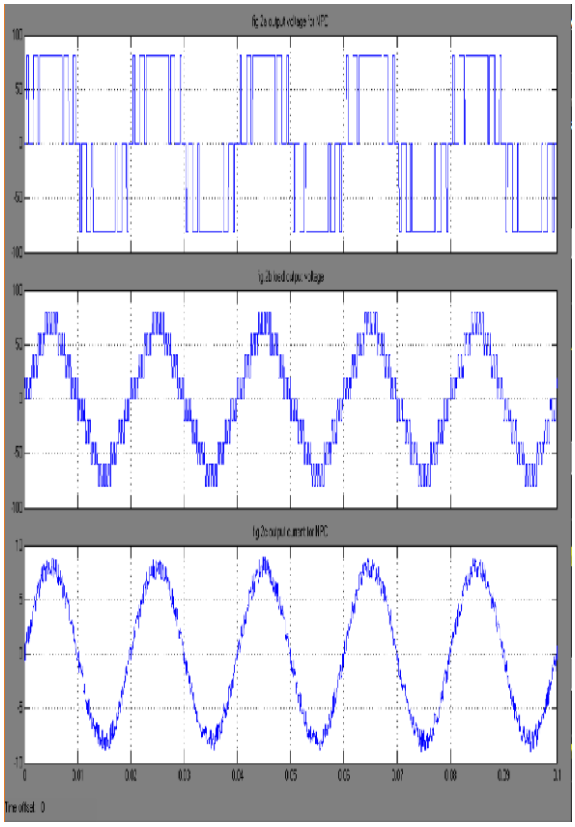

Fig.3.NPC inverter operation at 50Hz with m = 0:8

Experimental results are gained feeding a linear load with values R_L = 10 and L_L = 3mH with the 1kW prototype. The converter is operated with V_{dc} = 180V, while the H-Bridge dc-link voltage reference was set to 30V.For comparison purposes, Fig.3a shows the results for the NPC inverter operating without H-bridge compensation. In this result the NPC inverter is modulated by a 5-angle SHE pattern and m = 0:8. The first waveform corresponds to the NPC inverter output phase voltage $v_{a'N}$ which results in the 9-level load voltage waveform v_{an} of Fig.3b. Finally, Fig.3c shows the resulting output current waveform with its characteristic low frequency distortion.

The Simulink model for closed current loop control for NPC is as shown in fig.4. From this closed loop current control the triggering signals to different IGBT is provided. IN this current control loop the abc to dq transformation model is used to obtain direct axis and quadrature axis control. The phase lock loop is used which guaranties zero phase shift between its both inputs. The output obtained is nonlinear in this case. Hence to make it linear PI controllers is also used.

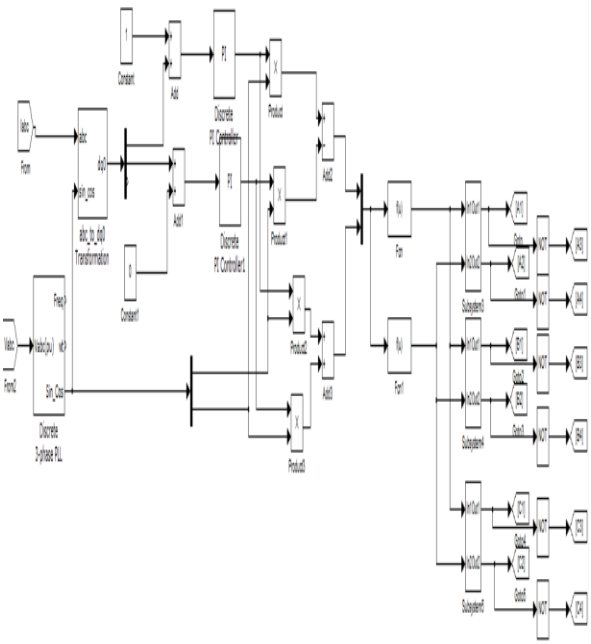

Fig.4.Simulink model for closed current loop for NPC inverter.

III. SELECTIVE HARMONIC ELIMINATION METHOD FOR NPC

The popular selective harmonic elimination method is also called fundamental switching frequency method which is based on the harmonic elimination theory. The multilevel fundamental switching scheme inherently provides the opportunity to eliminate certain lower order harmonics by varying the times at which certain switches are turned ON and turned OFF. A staircase output voltage waveform is generated by switching ON and OFF the switching devices in the multilevel inverters once during one fundamental cycle. This diminishes the switching losses in the devices. In this method, each switch is turned ON and turned OFF once in a switching cycle and switching angles are usually chosen based on specific harmonic elimination or minimization of THD in the output voltage. Two ways to eliminate lower order harmonics are;

i) By increasing the switching frequency of SPWM and SVM in case of two level inverters or in multicarrier based phase shift modulation for multilevel inverters.

ii) By computing the switching angles using SHE techniques.

The first method of eliminating low frequency harmonics is limited by the switching losses and the availability of the voltage steps. SHE techniques comprises the mathematical modeling of output waveform and solving them for switching angles based on the amplitude of the fundamental wave of the output voltage, the order and number of the eliminated harmonics.

Thus, the lower order harmonics are either eliminated or minimized while the higher order harmonics are filtered out in selective harmonic elimination method. Multilevel inverter can produce a quarter wave symmetric stepped voltage waveform synthesized from several DC voltages.

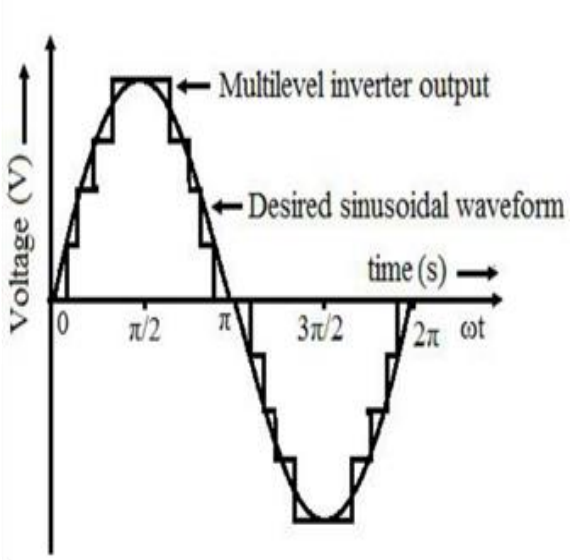

Fig.5. Stepped voltage waveform of multilevel inverter

By applying Fourier series analysis, the output voltage can be expressed as

$V(\omega)=\frac{4}{n\pi}\sum_h[V1\cos(n\theta 1)+V2\cos(n\theta 2)+..+Vh\cos(n\theta h)]$

Sin (n ωt)

Where, n = 1, 3, 5…

'h' is the number of DC sources and V1, V2.. Vh are the level of DC voltages. The switching angles must satisfy the condition $0< \theta 1< \theta 2 <.....< \theta_s < (\pi/2)$. However, if the switching angles do not satisfy the condition, this method no longer exists. To minimize harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to h-1 harmonic contents can be removed from the voltage waveform. In general, the most significant low frequency harmonics are chosen for elimination by properly selecting the triggering or switching angles and high frequency harmonic components can be readily removed by using additional filter circuits.

IV.CASCADED H-BRIDGE INVERTER

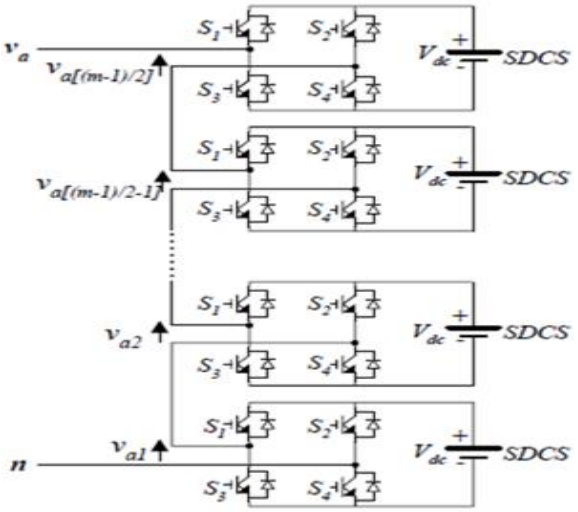

Fig.6. Single-phase structure of a multilevel cascaded H-bridges inverter

A single-phase structure of an m-level cascaded inverter is illustrated in Figure.6.Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources.

The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$. For a stepped waveform such as the one depicted in Figure with s steps, the Fourier Transform for this waveform follows

$V(\omega t) = \frac{4Vdc}{\pi}\sum_n[\cos(n\theta 1) + \cos(n\theta 2) + \cdots + \cos(n\theta n)]\frac{\sin(n\omega t)}{\pi}$, Where n=1, 3, 5, 7…

The magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows: The

conducting angles, θ_1, θ_2, ..., θ_s, can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency.

$H(n) = \frac{4}{\pi n}[\cos(n\theta 1)+\cos(n\theta 2)+\ldots+\cos(n\theta n)]$

Where n=1,3,5,7,……

harmonics, 5th, 7th, 11th, and 13th, harmonics are eliminated. Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications. Three-phase cascaded inverters can be connected in wye, as shown in Figure, or in delta. Peng has demonstrated a prototype multilevel cascaded static var generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system

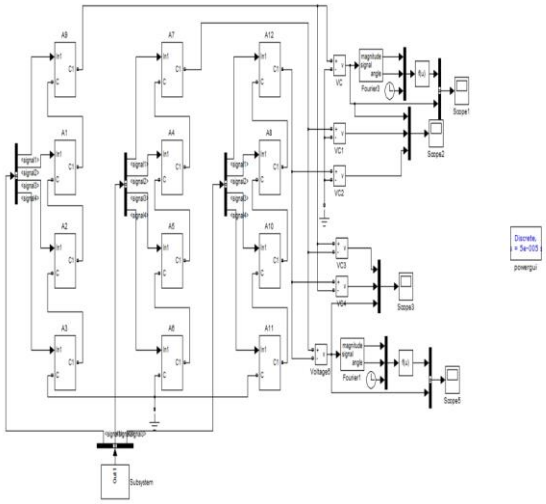

Fig.7. Simulink model for cascaded H-bridge

The simulation model is shown in the fig.7. for H-bridge The implementation of cascaded H-bridge Multilevel inverter in MATLAB software is done. In this model GTO with RC

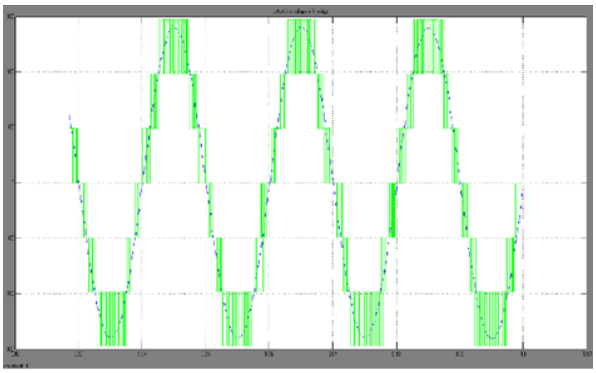

Fig.8. Output waveform for the line voltage

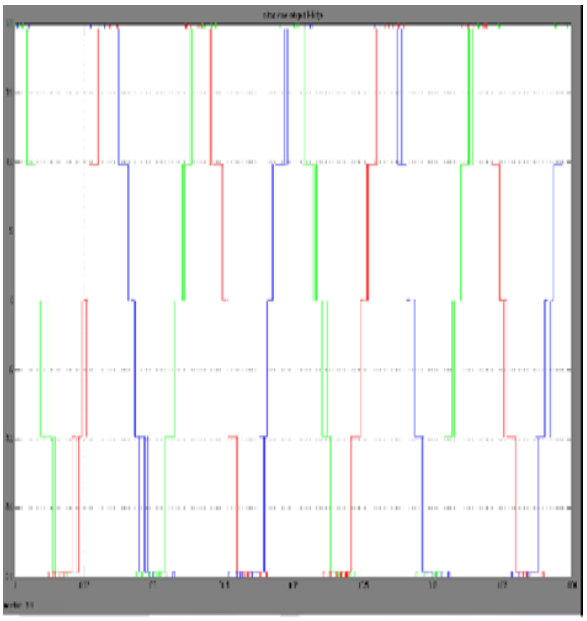

Fig.9. Output waveform for the phase voltage

Snubber circuit is used as switching device. For each phase four separate DC source is used. The output phase voltages and line voltages are measured on corresponding scopes.

IV HYBRID TOPOLOGY

A. Power Circuit

The proposed hybrid topology is made by a traditional three-phase, three-level NPC inverter, connected with a single phase H-bridge inverter in series with each output phase [12]–[13]. The power circuit is illustrated in Fig.10,with only the H-bridge of phase a shown in detail. To make sure as an inverter, the DC source for the NPC converter is provided by two series connected diode bridge rectifiers, connected in a twelve-pulse configuration.

The H-bridge DC-links are not connected to an external DC power supply, and they consist only of floating capacitors kept at a constant voltage by the control strategy. The implemented converter, shown in Fig.10, can be analyzed from two different points of view. The first interpretation is as a single hybrid multilevel inverter with a nine level phase voltage, obtained by the cascade connection of a three level NPC leg and an H-bridge per-phase. The second interpretation is as an NPC converter with a series active filter that compensates for the harmonic content produced by the low switching NPC stage.

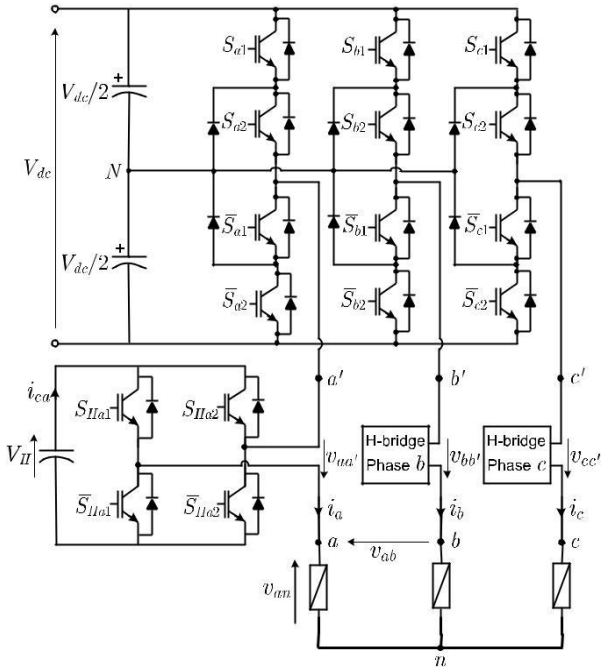

Fig.10.Hybrid topology power circuit.

The connection of the series H-bridge results in more levels being added on the output voltage waveform of the converter v_{aN} . In particular, if the value of V_H is smaller than $V_{dc}/4$, no redundant switching states are created and the output voltage waveform of the converter will have the maximum number of levels (nine), generating similar waveforms to those achieved by cascade H-bridge inverters with unequal dc sources [1], [15]. The increased number of output levels leads to a reduction in both the magnitude of voltage and the output voltage waveform and the harmonic content of the overall output voltage v_{aN}, enhancing the power quality of the hybrid converter. There is one solution to make V_H equal to a sixth of the NPC total dc-link voltage, i.e. $V_H = V_{dc}/6$, so that equally spaced output voltage levels would be created.we know that the NPC converter is modulated using the synchronous SHE method, the H-bridge should be modulated to compensate for the distortion created by the modulation of the NPC. This is done at a higher frequency using carrier based unipolar PWM. When deciding the value for the dc-link voltage of the H-bridges V_H , a sufficiently large value should be selected to obtain appropriate compensation of the remaining distortion, while at the same time the value of V_H should be kept as low as possible in order to minimize the additional switching losses.

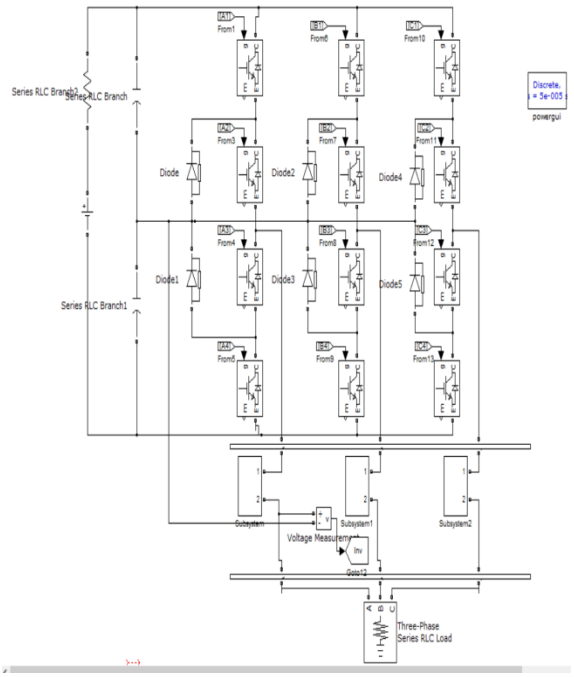

Fig.11. Simulink model for Hybrid topology

Figure 11 presents simulation results for the hybrid topology and control .It consists a combination of the 3 levels NPC inverter and H-bridge inveter. The resulting waveform of this simulation model is shown in fig 12.

In comparison to the previous results, the full hybrid topology results are shown in Fig. 12.a) shows the three-level NPC output voltage, v_a0_N , generated under the same conditions, while Fig. 12.b) shows the output voltage of the respective H-Bridge $v_{aa}0$ with the higher switching frequency compared with the NPC output. Some distortion can be created due to the semiconductors drop, which will not be consider for higher voltage applications. The H-Bridge DC-link voltage is shown in Fig. 12.c), which is controlled to be the desired voltage of $V_H = 0{:}167\ V_{dc}$ Also, it can be noted that in Fig.12. e) that 33 different voltage levels are applied to the load voltage, causing less distortion in the output inverter waveforms than in the NPC output waveforms of Fig.3 . This is seen clearly in the current waveform in Fig. 12.f), with a highly sinusoidal shape compared with the output current waveform without the H-Bridges harmonic compensation. is clear that current waveform improvement has been achieved with the hybrid inverter. Hence, comparing the results of Fig.3. with those of Fig.12f., it is clear that current waveform improvement has been achieved with the hybrid inverter.

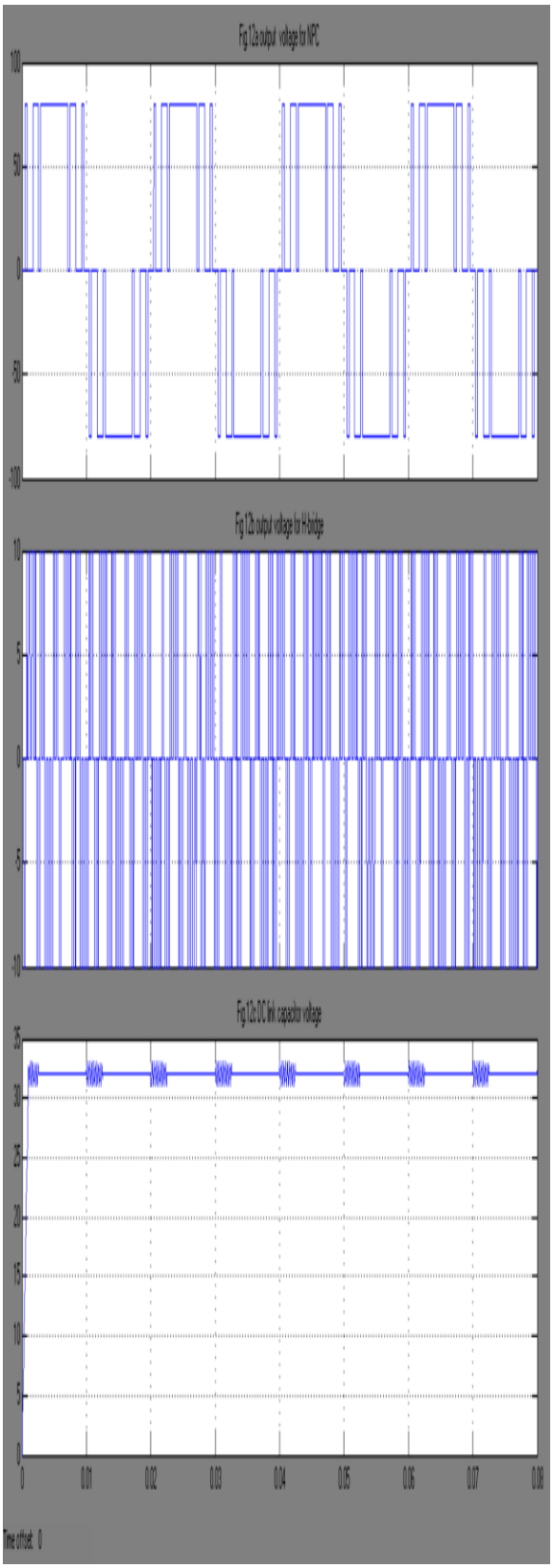

Fig.12-a) NPC output voltage b) H-bridge output voltage c) H-bridge dc-link voltage

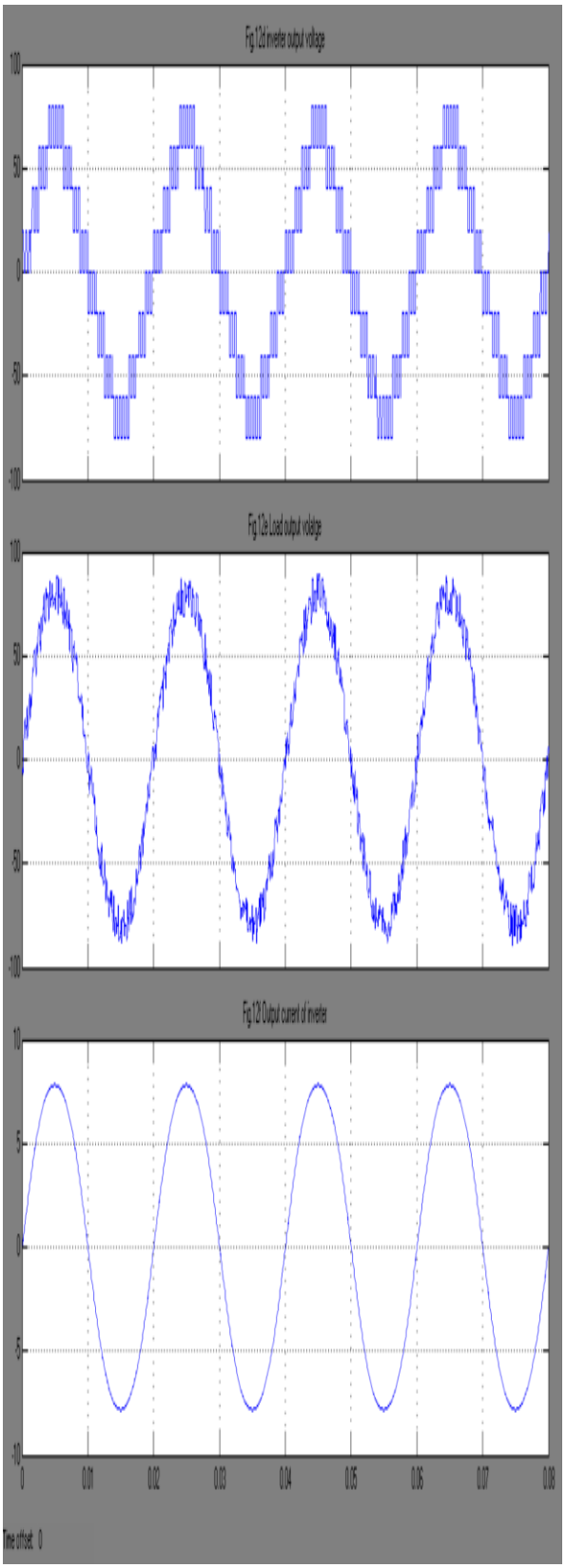

Fig.12 d) Inverter output voltage e) load output voltage f) output current.

V.SINUSOIDAL PULSE WIDTH MODULATION

Sinusoidal PWM method is also known as the triangulation, sub harmonic, sub oscillation method, Carrier Based Pulse Width Modulation (CB-PWM) is very popular in industrial applications (Mohamed Dahidah & Vassilios Agelidis 2008). The SPWM scheme is illustrated in Figure 4.3. In this, V_c is the peak value of the triangular carrier wave and V_r is the reference, or modulating signal. For realizing SPWM, a high frequency triangular carrier wave is compared with a sinusoidal reference of the desired frequency. The intersection of sinusoidal reference and triangular waves determines the switching instants and commutation of the modulated pulse.

Carrier based modulation for more than two level inverters require more carrier signals. For N_L -level inverter, minimum (N_L -1) carrier signals are needed. Each carrier signal is responsible for a pair of switches. Every leg has two switches, one switch is controlled directly by the comparator signal and the other is controlled by its inverting signal. Multiple carrier signals in multilevel inverters create various possibilities of mutual locations of those signals.

VI. CONCLUSION

This paper presents the brief summary of multilevel inverter circuit topologies, control strategies and their simulation models. This paper also focuses on the different modulation technics used for multilevel inverter. Now a day a lot of commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel inverter-related technologies is occurring. This paper cannot cover or reference all the related work, but the fundamental principle of different multilevel inverters has been introduced systematically. The intention of the authors was simply to provide groundwork to readers interested in looking back on the evolution of multilevel inverter technologies, and to consider where to go from here. This paper also shows that how recent multilevel inverter output is better than previous through matlab simulation.

REFERENCES

[1] J. S. Lai and F. Z. Peng, "Multilevel converters–A new breed of power converters," IEEE Trans. Ind. Applicat., vol. 32, pp. 509–517, May/June 1996.

[2] L. Tolbert, F.-Z. Peng, and T. Habetler, "Multilevel converters for large electric drives," IEEE Trans. Ind. Applicat., vol. 35, pp. 36–44, Jan./Feb. 1999.

[3] R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. Sulistijo, B. Woo, and P. Enjeti, "Multilevel converters — A survey," in Proc. European Power Electronics Conf. (EPE'99), Lausanne, Switzerland, 1999, CD-ROM.

[4] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," IEEE Trans. Ind. Applicat., vol. IA-17, pp. 518–523, Sept./Oct. 1981.

[5] T. A. Meynard and H. Foch, "Multi-level choppers for high voltage applications," Eur. Power Electron. Drives J., vol. 2, no. 1, p. 41, Mar. 1992.

[6] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of multilevel inverters for static var compensation," in Conf. Rec. IEEE-IAS Annu. Meeting, Oct. 1994, pp. 921 928.

[7] P. Hammond, "A new approach to enhance power quality for medium voltage ac drives," IEEE Trans. Ind. Applicat., vol. 33, pp. 202–208, Jan./Feb. 1997.

[8] E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerge, "A new medium voltage PWM inverter topology for adjustable speed drives," in Conf. Rec. IEEE-IAS Annu. Meeting, St. Louis, MO, Oct. 1998, pp. 1416–1423.

[9] R. H. Baker and L. H. Bannister, "Electric power converter," U.S. Patent 3 867 643, Feb. 1975.

[10] R. H. Baker, "Switching circuit," U.S. Patent 4 210 826, July 1980.

[11] "Bridge converter circuit," U.S. Patent 4 270 163, May 1981.

[12] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," IEEE Trans. Ind. Appl., vol. 41, no. 2, pp. 655–664, Mar./Apr. 2005.

[13] T. Gopalarathnam, M. Manjrekar and P. Steimer, "Investigations on a unified controller for a practical hybrid multilevel power converter," in Proc. IEEE APEC, 2002, pp. 1024 –1030. ISIE, 2008, pp. 2329–2335.

[14] S. Bernet, R. Teichmann, A. Zuckerberger and P. Steimer, "Comparison of high-power igbt's and hard-driven gto's for high-power inverters," IEEE Trans. Ind. Appl., vol. 35, no. 2, pp. 487–495, Mar./Apr. 1999.

[15] C. Rech and J. R. Pinheiro, "Hybrid multilevel converters: Unified analysis and design considerations," IEEE Trans. Ind. Electron., vol. 54, no. 2, pp. 1092–1104, Apr. 2007.