FPGA Based Traffic Sign Detection with High Resolution Camera

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***Abstract*- Traffic sign detection plays an important role in a number of practical applications, such as intelligent driver assistance and roadway inventory management. In order to process the large amount of data from either real-time videos or large off-line databases, a high-throughput traffic sign detection system is required. When processing high-definition (1080p) video, it achieves the throughput of 126 frames/s and the energy efficiency of 0.041 J/frame. To efficiently utilize the hardware resources and maximize the detection speed .An FPGA-based accelerator for traffic sign detection using cascade classifiers. In this work, we propose an FPGA-based traffic sign detection based on cascade classifiers. To maximize the throughput and power efficiency. We propose following ideas 1) rearranged numerical operations; 2) shared image storage;**

I. INTRODUCTION

The single image with 320×480 pixels are processed to reduce the frame size and to reduce the power consumed. The image with less frame size can be converted by using the FPGA accelerator with fast detection. Real Time applications are usually constrained by cost and energy and have limited computational power. The huge amount of data prevents us from applying complex algorithm to get the result of interest in a timely manner.

In this process we use rearranged numerical operations for high throughput image processing, the need to access a huge amount of data poses enormous challenges on memory bandwidth. To address this issue, we propose a feature extraction scheme with rearranged numerical operations in order to reduce the amount of memory access. In addition, the proposed approach greatly reduces the overall computational cost by combining similar numerical operations together. With limited on – chip static random access memory, it is difficult, if not possible to transfer and store a large amount of image data within on-chip SRAM. To address this challenge, the image should be converted into gray scale image.

II. SYSTEM ARCHITECTURE

FIELD PROGRAMMABLE GATE ARRAY:

FPGA is an integrated circuit which is designed to be configured by a designer or customer after manufacturing. The hardware description language (HDL) is generally used to specify the FPGA configuration. Any computable problems can be solved by an FPGA. Because of their parallel nature they are significantly faster in some of the applications.

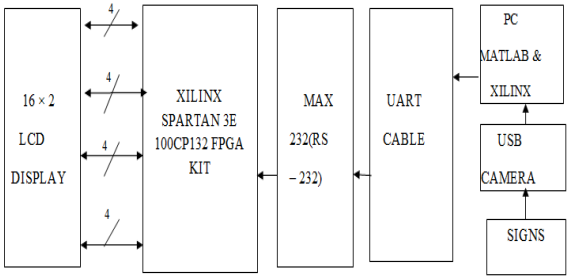
EXISTING SYSTEM

The existing system might be the traffic sign detection system which is used in the embedded systems. In the embedded systems it is very difficult to change the hardware and software configurations. The scalability of the embedded systems might be a huge problem faced by this existing system. Another problem is that the memory or computing capability is very low.

PROPSED SYSTEM

In this proposed system FPGA has been used in order to improve performance of the system as well as the accuracy of the system than the PIC controller used in the embedded systems. The function of reusability has been used in the FPGA in which the prototype which is implemented contains faults which can be easily reconfigured by generating the HDL code and bit streams. Memory capabilities have been improved in FPGA when compared with the other systems.

III. ARCHITECTURE



DESCRIPTION

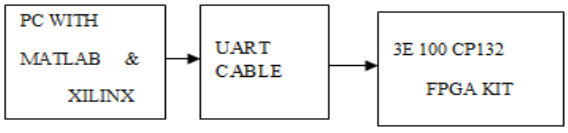
The block diagram represents the function of the traffic sign detection using high resolution camera.

In the first block the signs represent the traffic signs which are present at the side of the roads. The USB camera is used in order to capture the traffic signs. These traffic signs cannot be read by the system as a design, therefore the mat lab software can be used to convert the signs into binary values (0's and 1's). Then the Xilinx software can be used to display the result in the LCD display. The UART cable can be used to send the data's into the system. The MAX 232(RS-232) can be used to process the data's. Now the XILINX SPARTAN 3E 100 CP132 FPGA kit can be used to display the sign in the LCD display. The LCD display consists of 16 pins which are divided into 4 units each consisting of 4 pins. The LCD unit displays the final result.

IV. DETECTION UNIT

The images in the traffic sign detection can be detected by the USB camera which consists of a resolution of 320* 480 with 12 mega pixels. The image which is captured is fed into the MATLAB software and this captured image is processed through grey scale images which will reduce the size of the pixel and improves the computational process.

PROCESSING UNIT



The process of traffic sign detection consists of a UART transmitter and UART receiver. Throughput with minimum frames per second is achieved by the XILINX which provides high bandwidth. For asynchronous serial communication in which data format and to increase the transmission speed the UART computer hardware device is used. in order to convert the logical signals of the UART to form external signaling levels, separate interface devices are used.

V. MATERIALS AND SOFTWARES

A. LCD DISPLAY

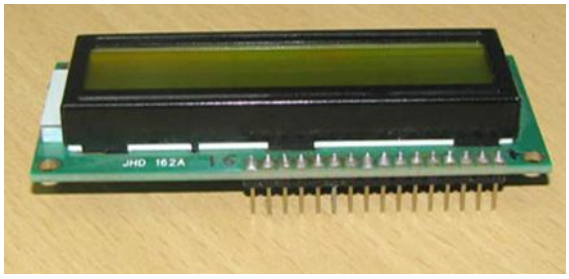


FIG.1 LCD DISPLAY

It is a module used for wide range of displaying applications. It is very basic module commonly used in circuits and as a display device. It is preferred over seven segments and multi segment LED. LCD can easily computable and are very economical. It has no limitation displaying special and custom characters. The characters are displayed in 5*7 pixel matrix in 16*2 LCD. A command can be given to LCD for various operations controlling display clearing screen and setting cursor position. The data registers stores the data that to be displayed on the LCD.

B.FPGA XILINX SPARTAN 3E-100CP 132

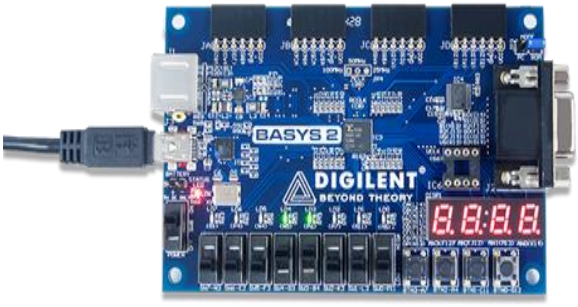


FIG.2 FPGA XILINX SPARTAN 3E - 100 CP13

The FPGA Spartan family is specially designed to meet the high volume cost perceptive electronic

application. It includes 25 devices offering sensitives ranging from 51000 to 5.1 million system gates. It was Spartan 3 platform was industries first 90 nm FPGA which delivers more functionality and bandwidth then previous systems. It provides superior alternative to mask programmed ASICS it avoid high initial cost, the lengthy development cycle and the inbuilt rigidity of conversional ASICS. It provides additional benefits of non-volatility and high amount of on board client flash.

C. RS – 232 DEVELOPEMENT BOARD

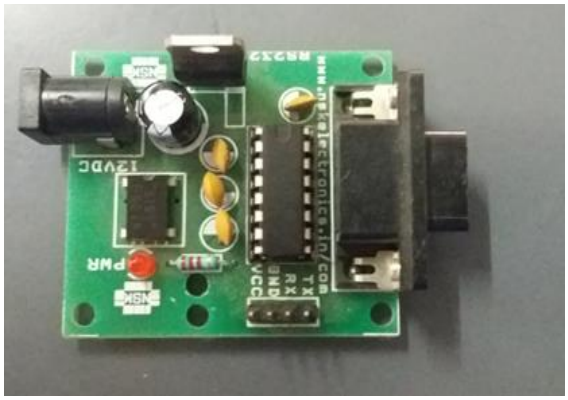


FIG.3 RS-232 DEVELOPMENT BOARD

An RS-232 serial port was once a standard feature of a personal computer, used for connections to modems, printers, mice, data storage, uninterruptible power supplies, and other peripheral devices. However, RS-232, when compared to other serial interfaces such as RS-422, RS-485 and Ethernet, is hampered by low transmission speed, short maximum cable length, large voltage swing, large standard connectors, no multipoint capability and limited multidrop capability. In modern personal computers, USB has displaced RS-232 from most of its peripheral interface roles. Many computers no longer come equipped with rs-232 ports (although some motherboards come equipped with a COM port header that allows the user to install a bracket with a DE-9 port) and must use either an external USB-to-RS-232 converter or an internal expansion card with one or more serial ports to connect to RS-232 peripherals. Nevertheless, thanks to their simplicity and past ubiquity, RS-232 interfaces are still used - particularly in industrial machines, networking equipment, and scientific instruments where a short-range, point-to-point, low-speed wired data connection is adequate.

D. MATLAB R2014a

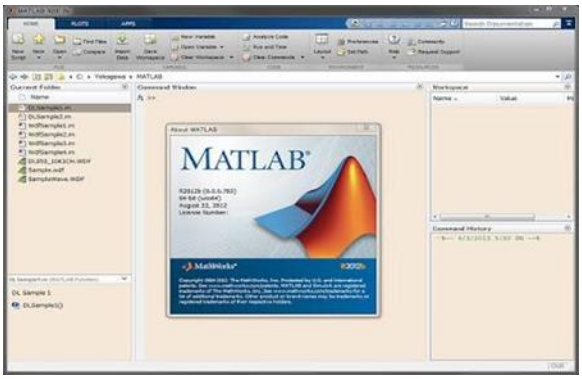


FIG4.MATLAB SOFTWARE

MATLAB (matrix laboratory) is a multi-paradigm numerical computing environment. A proprietary programming language developed by Math works, MATLAB allows matrix manipulations, plotting of functions and data , implementation of algorithms, creation of user interfacing with programs written in other languages, including C,C++,Java, Fortran and python. Although MATLAB is intended primarily for numerical computing, an optional tool box uses the MUPAD symbolic engine, allowing access to symbolic computing abilities. An additional package, Simulink, adds graphical multi-domain simulation and model based design for dynamic and embedded system.

E.XILINX

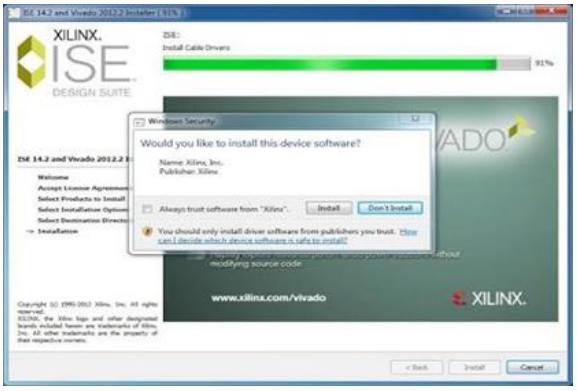


FIG5.XILINX SOFTWARE

Xilinx ISE means Xilinx Integrated Software Environment (ISE). This Xilinx design software suite allows you to take your design from design entry through Xilinx device programming. The ISE Project Navigator manages and processes your design through several steps in the ISE design flow. These

steps are Design Entry, Synthesis, Implementation, Simulation/Verification, and Device Configuration.

VI. RESULT & DISCUSION

After the completion of image detection and recognition process, the recorded images are scanned and compared with the preloaded traffic signs. It is compared by pixel by pixel in each frame and the frame that matches the preloaded traffic sign is identified and displayed by using a LED display, in which the name of the symbol is shown in alphabet wordings in the seven segment display through which we can identify traffic sign before some distance as a safety precaution to avoid accidents in roadway inventory.

VII. CONCLUSION

The traffic sign recognition and detection is designed using FPGA XILINX kit in order to achieve high throughput and low power consumption, which is integrate with some novel ideas in the proposed system design that includes rearranging numerical operations, sharing of image storage and grey scale imaging. The proposed design is instigated and appraised with XILINX SPARTAN 3E-100CP132 and RS-232 development board. The design achieves high throughput of 150 frames per second and energy proficiency of 0.043 j/frames, when the system process high definition image of 480 x 640 resolution. The system is compared with the existing embedded system that used in traffic sign detection, which is inferior in terms of processing speed and computational performance. For future developing process we can involve more rearranged numerical solutions and video decoding systems for even better performance of the assistance of roadway inventory

REFERENCE

[1] S. Lafuente-Arroyo, P. Gil-Jimenez, R. Maldonado-Bascon, F. Lopez-Ferreras, and S. Maldonado-Bascon, "Traffic sign shape classification evaluation I: SVM using distance to borders," in Proc. IEEE Intell. Vehicles Symp., Jun. 2005, pp. 557–562.

[2] de la Escalera, L. E. Moreno, M. A. Salichs, and J. M. Armingol, "Road traffic sign detection and classification," IEEE Trans. Ind. Electron., vol. 44, no. 6, pp. 848–859, Dec. 1997.

[3] P. Sermanet and Y. LeCun, "Traffic sign recognition with multiscale convolutional networks," in Proc. Int. Joint Conf. Neural Netw., Jul./Aug. 2011, pp. 2809–2813.

[4] J. Zhao, X. Huang, and Y. Massoud, "An efficient real-time FPGA implementation for object detection," in Proc. IEEE Int. New Circuits Syst. Conf., Jun. 2014, pp. 313–316.

[5] M. Müller et al., "Design of an automotive traffic sign recognition system targeting a multi-core SoC implementation," in Proc. Design, Autom. Test Eur. Conf. Exhibit., Mar. 2010, pp. 532–537.

[6] J. Zhao, S. Zhu, and X. Huang, "Real-time traffic sign detection using SURF features on FPGA," in Proc. High Perform. Extreme Comput. Conf., Sep. 2013, pp. 1–6.

[7] D. Ciregan, U. Meier, and J. Schmidhuber, "Multi-column deep neural networks for image classification," in Proc. IEEE Conf. Comput. Vis. Pattern Recognit., Jun. 2012, pp. 3642–3649.

[8] X. Baro, S. Escalera, J. Vitria, O. Pujol, and P. Radeva, "Traffic sign recognition using evolutionary adaboost detection and forestECOC classification," IEEE Trans. Intell. Transp. Syst., vol. 10, no. 1, pp. 113–126, Mar. 2009.

[9] P. Viola and M. Jones, "Rapid object detection using a boosted cascade of simple features," in Proc. IEEE Conf. Comput. Vis. Pattern Recognit., vol. 1. Dec. 2001, pp. I-511–I-518.

[10] K. Korekado et al., "A VLSI convolutional neural network for image recognition using merged/mixed analog-digital architecture," J. Intell. Fuzzy Syst., vol. 15, nos. 3–4, pp. 173–179, Dec. 2004.