A Low Power Efficient N-MOS Based 1-Bit Full Adder

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***Abstract*- A Full adder is a basic and most important digital component. To improve the full adder architecture many improvements has been made. Nowadays efficient full adder circuit design is one of the main challenges for VLSI engineers. A full adder circuit is considered as one of the basic building blocks of Digital Signal Processors (DSPs), Arithmetic and Logic Units (ALUs), Application Specific Integrated Circuits (ASICs) and many other digital circuits and systems. In recent times, various types of full adder circuits using different logic design styles have been proposed. In our work, a new NMOS based 1-bit full adder has been proposed which uses Pass Transistor Logic (PTL) technique in its design for improving performance. The result of the post layout simulation is implemented in TANNER TOOL.**

***Index Terms*- N-channel Metal Oxide Semiconductor (N-MOS); Full adder,Pass Transistor Logic (PTL), Power-Delay Product (PDP,Transistor (T).**

I. INTRODUCTION

Addition is one of the common and widely used fundamental arithmetic operations in many VLSI systems. Other similar arithmetic operations are subtraction, multiplication, division, address calculation etc. Using binary adders the full adder is designed and improving 1-bit full adder performance plays an important role in VLSI. Different varieties of full adders exploit completely different logic designs and technologies, which are reported in , and they unremarkably aim at increasing speed and reducing power dissipation.

To improve the performance of adder there we have two methods. One is 'System Level viewpoint' method and second method is critical Style view point'. In system level viewpoint it consists of finding the longest signal path in the ripple adders and reduce the trail so as to scale back the full signal path delay. The longest signal path is where the carry out bit of the most significant bit has to be calculated in most things. The second method is 'Circuit Style Viewpoint' in transistor level, that is, semiconductor device level design skills are supported by designing of high performance full adder. An optimized design is required to prevent any decrease in signal magnitude, provide small delays, consume less power in critical paths and even at low supply voltage maintain consistency while moving headed for smaller designs such as in nanometer range. Driving capability for different loads, outputs without glitches, layout regularity and interconnection quality should also be looked after.

Important parameters in measuring performance of VLSI systems are speed, area, power consumption and cost. Power consumption must be reduced in a VLSI system for two main reasons. Firstly, reduction of power consumption will lead to increased density of function that can be implemented on a single IC. Secondly, in battery operated systems, it is essential to save energy for longer battery life time. These reasons play vital role in modern equipment's due to the explosive growth in portable electronic devices like laptops, medical appliances, portable communication systems, multimedia and nonequivalent pace of improvement of battery technology and may more. Energy efficient high performance circuits are desirable for any electronics gadgets. The supporting hardware should be equally inexpensive and compact. So, design engineers are now concentrating on efficient designs of electronic components to meet the above mentioned critical design issues.

Arithmetic operations are useful in all digital electronic systems like digital signal processing, image processing, video processing, arithmetic and logic units, floating point processor and microprocessors. Binary addition is one of the most useful operations in any arithmetic circuit. Such vast use of this arithmetic operation has created interest among the researchers to propose several kinds of new designs for the implementation of 1-bit full adder circuit in recent years.

II. PREVIOUS WORK

The N-MOS based low power 1 bit full adder has been designed using PTL technique. . The adder shown.

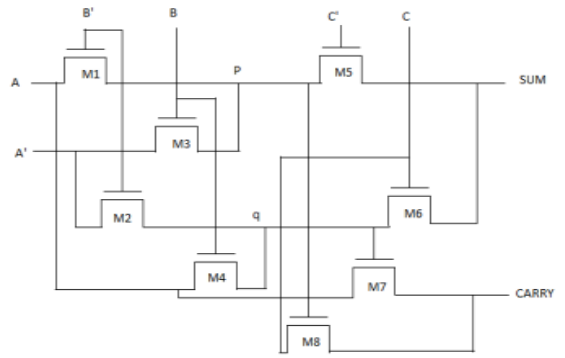

Fig1. 8T full adder

Here Sum = A⊕ B ⊕ C

And Carry = AB + BC + CA

= AB + BC (A+A´) + CA (B+B´)

= AB + ABC + A´BC + AB´C

= AB (1+C) + (AB´ + A´B) C

= AB + (A⊕ B) C

Circuit explanation: The first transistor M1 is generating output AB´ while M3 is generating A´B. The two outputs together generate (A⊕ B) at point p. Outputs of M2 and M4 are A´B´ and AB respectively. They produce (AB) after meeting at point q. The logic at the outputs of M5 and M6 are (A ⊕ B) C´ and (AB) C. They are generating the Sum output in the following manner:

Sum = (A ⊕ B) C´ + (A⊕ B)´ C = A⊕ B ⊕ C

Similarly, the output logics of M7 and M8, (AB) A and (A B) C, together generate Carry output as:

Carry = (AB) A + (A B) C

= (AB + A´B´) A + (A B) C

= AB + (A B) C

The logic values at the output levels for different input combinations of this circuit are listed in Table.

A	B	C	M 1	M 2	M 3	M 4	M 5	M 6	M 7	M 8	Sum	Carry
0	0	0	0	1	0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	1	0	0	1	0
0	1	0	0	0	1	0	1	0	0	0	1	0
0	1	1	0	0	1	0	0	0	0	1	0	1
1	0	0	1	0	0	0	1	0	0	0	1	0
1	0	1	1	0	0	0	0	0	0	1	0	1
1	1	0	0	0	0	1	0	0	1	0	0	1
1	1	1	0	0	0	1	0	1	1	0	1	1

Fig2.Truth table

III. PROPOSED WORK

A basic full adder has three inputs and two outputs which are sum and carry. Full adder cell is designed with CPL and Multiplexing Control Input technique for both sum and carry operations. The Sum and Carry operations are based on the equations 1 & 2 mentioned below:

Sum = A⊕B⊕C (1)

Carry = (A⊕B) C + AB (2)

Sum equation contains XOR gates whose design using CPL logic is desired for low power system.

Full adder circuit can be implemented with different combinations of XOR/XNOR modules and two multiplexer but this approach has not been used in current work as proposed XNOR/XOR cell shows high power consumption than single XNOR gate. The single bit full adder using six transistors has been implemented and shown in Figure.

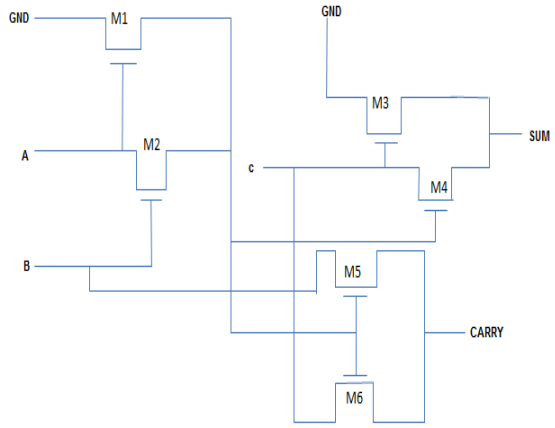

Fig3. 6T Full Adder

NMOS and PMOS transistors have been taken with gate length of 0.65µm. Simulations have been performed using SPICE based on TSMC 0.35µm CMOS technology with supply voltage of 1V. Proposed full adder has been compared with earlier reported circuits and reported circuit shows reduced power consumption with less number of transistors.

A	B	C	M1	M 2	M 3	M 4	M 5	M6	SUM	CARRY
0	0	0	0	1	0	0	0	0	0	0
0	0	1	0	1	0	0	0	1	1	0
0	1	0	0	0	1	0	1	0	1	0
0	1	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	1	0	1	0
1	0	1	1	0	0	0	0	0	0	1
1	1	0	0	0	0	1	0	0	0	1
1	1	1	0	0	0	1	0	1	1	1

Fig4.Truth table

The proposed low power full adder consists of both PMOS & NMOS transistors. The focus is to eliminate the power hungry inverters. The NMOS transistors that require inversion of gate input are replaced by PMOS transistors. The existing & proposed architectures are implemented using Full Custom ASIC design methodologies. Both the existing & proposed full adder architectures are simulated using Tanner tool.

Since the change occurs in the architectural design of the device, below are the advantages of low power:

- No area or performance penalty
- Minimum verification effort
- High scalability

IV.POWER REDUCTION USING GATING TRANSISTORS

The power reduction must be achieved without comprising performance which makes it hard to reduce leakage current during normal operation of mobile. We perform analysis and simulation of various parameters such as standby leakage power, active power, ground bounce noise and propagation delay using Cadence Spectra 80nm standard CMOS technology. Implementation of adder cells to reduce power consumption and to increase the speed has proved as an efficient solution for power reduction. Moreover, realization of adders with different approaches using CMOS technology widens the area of power reduction . Performance of the adder cells can be evaluated by measuring the factors such as leakage power, active power, ground bounce noise in context to voltage and transistor scaling. The power gating technique uses high threshold voltage sleep transistor which cut-off a circuit block when the block is not switching . Here the sleep transistor is connected between actual ground rail and virtual ground. This insertion of sleep transistor divides the power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off during inactive period. The sizing of sleep transistor is an important design factor. This technique is also known as MTCMOS or Multi-Threshold CMOS and reduces standby or leakage power.

Power gating affects design architecture more than clock gating. It increases time delays as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes. Shutting down the blocks can be achieved either by software or hardware. Power gating uses low-leakage PMOS or NMOS as sleep transistors. As told earlier, the CMOS circuit is the base adder and all simulation results comparison has been done with it. It consists of 28 transistors incorporating PMOS pull up and NMOS pull down networks to produce desired outputs. Here the sizing of transistors plays a vital role. Here, the transistor ratio of PMOS to NMOS has been kept 2 for an inverter and on considering the remaining blocks as equivalent inverters also follows the same ratios. When it is simulated in 80nm process, it provided very poor results in context to leakage power. Thus the adder circuit was modified with proper sizing using power gating technique.

The power gating technique is shown to reduce the leakage power by placing a sleep transistor between actual ground rail and circuit ground (virtual ground). Here low leakage NMOS is used as a sleep transistor. Estimation of the ground bounce noise is done when circuit is connected to the sleep transistor. The width and length of smallest transistor has been kept 120nm and 100nm respectively for 80nm CMOS technology. The W/L ratio for NMOS is kept as 1.2 whereas for PMOS its 3.8 which are 3.1 times that of NMOS. The sizing of each block is based on the assumptions that each block is equivalent to inverter and same inverter ratio is maintained for each block. Since sub threshold current is directly proportional to W/L ratio of transistor, the sizing reduces the standby leakage current to a very great extent.

V. ACTIVE AND STANDBY LEAKAGE POWER

The dissipation of power which occurs during the active mode of the circuit is active power. This active power consists of dynamic power as well as the static power. It is measured by giving input vectors to the circuit, then calculating the average power dissipation and comparing the result with the base adder i.e. conventional 1-bit CMOS full adder. International Ground Bounce is the voltage oscillation between ground pin on a component package and the ground reference level on the component die. Essentially it is

caused by a current surge passing through the lead inductance of the package. The effect is most visible when all outputs switch simultaneously. In saturation region an instantaneous charge current passes through the sleep transistor, during power mode transition.

VI. EXPERIMENTAL RESULTS

The CMOS solution is about 20% slower than the CPL version, but has a much smaller transistor count and dissipates less than 1/3 the power. A CPL version with downsized transistors still consumes twice as much power and is slower than CMOS. The CMOS adder has 41% fewer transistors and 29% fewer circuit nodes than the CPL version. The reasons for the greater power dissipation of the CPL adder are basically the larger switched capacitance (more transistors, dual-rail wiring), larger short-circuit currents (differential swing-restoration circuitry), and a higher average switching activity than was observed in the CMOS version. On the other hand, the CMOS adder takes advantage of the efficient implementation of the simple AOI/OAI-gates used for carry-propagation and of the single-rail interconnects. Note that the inaccuracies from wiring estimation can be regarded as considerably smaller than the observed differences in circuit performance.
Table shows the power dissipation of various types of full Adder circuits.

SL. No	Adder Configurations	Power Consumption	No of Transistor
1	TGA20T	1255.54	20
2	16T adder	591.07	16
3	10T SERF	531.29	10
4	22T hybrid adder	1836.4	22
5	22T HPSC	1533.9	22
6	8T full adder	581.542	08
7	6T full adder	1.4995002	06

Fig5. Comparison of Power Consumption and Number of Required Transistors with Earlier Reported Circuits

The configuration details on the different types of full adder and is adder configuration with power efficiency rate difference.

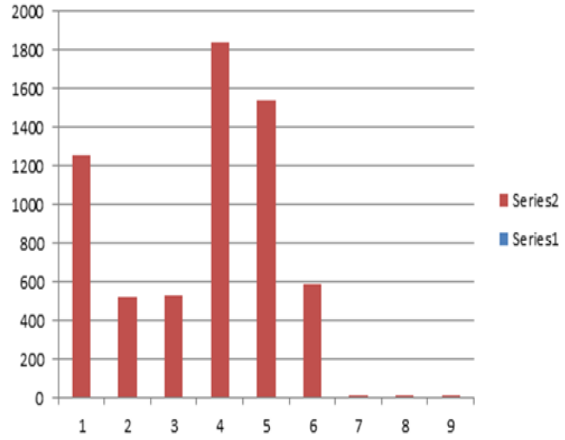

Fig6. Power dissipation (μW) of different type of full adders

Although the leakage power dissipation of our circuits is low at the range of voltages, which is used for simulation, it can be a little considerable at lower supply voltages. However, as our designs have low Dynamic power consumption, the average power consumption still remains low

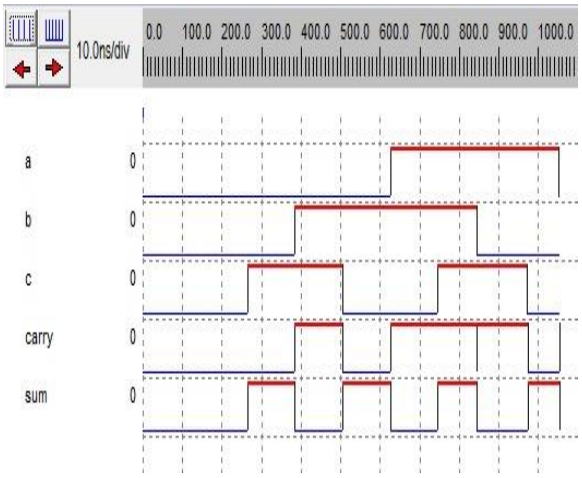

Fig7.Full Adder Wave Form

VII. CONCLUSION

In 1 bit full adder circuit is proposed and it is designed with only N-MOS based pass transistor logic style. The proposed circuit has been simulated using CMOS process technology. The layout of the same has been generated using Tanner tool version 13.0. The post layout simulation result of the proposed circuit has been compared with earlier reported circuits and result analysis shows that the proposed full adder circuit consumes less power and less silicon area as compared to other full adder circuits. Other advanced PTL techniques may be

used. The power consumption in the proposed circuit is 1.95002e-012.The performance degradation at higher load capacitance is a major concern of this proposed circuit and needs to be eliminated in future

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